



12500 TI Boulevard, MS 8640, Dallas, Texas 75243

Revision A is to update the Package Outline drawing for DGQ package and remove wire diameter change for Group 2 device as highlighted below. We apologize for any inconvenience this may have caused.

PCN Number:	20251015000.1		PCN Date:	September 03, 2026	
Title:	Qualify MLA as an additional Assembly site for select devices				
Customer Contact:	Change Management team		Dept:	Quality Services	
Change Type:					
☒ Assembly Site	☐ Design	☐ Wafer Bump Material			
☒ Assembly Process	☐ Data Sheet	☐ Wafer Bump Process			
☒ Assembly Materials	☐ Part number change	☐ Wafer Fab Site			
☒ Mechanical Specification	☐ Test Site	☐ Wafer Fab Material			
☒ Packing/Shipping/Labeling	☐ Test Process	☐ Wafer Fab Process			
PCN Details					
Description of Change:					
Texas Instruments is pleased to announce the qualification of TI Malaysia (MLA) as an additional Assembly site for the list of devices shown below. Material differences between sites are as follows.					
Group 1 Device					
	ASESH	MLA			
Wire diam/type	1.3mil Au	1.3mil Cu			
Mount compound	EY1000063	4211470			
Mold compound	EN2000515	4211880			
Lead finish	NiPdAuAg	NiPdAu			
Package outline	DGQ0010E	DGQ0010 DGQ0010K			
Group 2 Device					
	TAI	MLA			
Wire diam/type	0.96mil Cu	0.8mil Cu			
Marking difference	TI logo, with G4	TI letter, no G4			
Reason for Change:					
Continuity of supply.					
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):					
None.					
Impact on Environmental Ratings					
Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.					
RoHS	REACH	Green Status	IEC 62474		
☒ No Change	☒ No Change	☒ No Change	☒ No Change		

Changes to product identification resulting from this PCN:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
ASESH	ASH	CHN	Shanghai
TI Taiwan	TAI	TWN	Chung Ho, New Taipei City
TI Malaysia	MLA	MYS	Kuala Lumpur

Sample product shipping label (not actual product label)

**Group 1 Product Affected:**

TPS92515DGQR	TPS92515DGQT	TPS92515HVDGQR	TPS92515HVDGQT
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Group 2 Product Affected:

UCC5350MCDWVR	UCC5390ECDWVR
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Group 1 Qualification Report
Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)
Approve Date 31-March-2025

Product Attributes

Attributes	Qual Device: TPS92515QDGQRQ1	QBS Package Reference: SN65HVD1040AQDRQ1	QBS Process Reference: LM5165QDRCRQ1	QBS Package Reference: TPA6211BTDGNRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 2
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 105
Product Function	Power Management	Interface	-	Signal Chain
Wafer Fab Supplier	RFAB	DL-LIN	RFAB	MH8
Assembly Site	MLA	MLA	CLARK-AT	MLA
Package Group	VSSOP	SOIC	QFN	VSSOP
Package Designator	DGQ	D	DRC	DGN
Pin Count	10	8	10	8

QBS: Qual By Similarity, also known as Generic Data

Qual Device TPS92515QDGQRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: TPS92515QDQGRQ1	QBS Package Reference: SN65HVD A1040AQDRQ1	QBS Process Reference: LM5165QDRCRQ1	QBS Package Reference: TPA6211BTDGNRQ1
Test Group A - Accelerated Environment Stress Tests											
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	-	3/828/0	-	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	3/0/0	-	3/0/0	3/0/0
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C	96 Hours	-	3/231/0	-	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	-	3/231/0	3/231/1 ¹
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	3/231/0	-	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	110C/85%RH	264 Hours	-	-	3/231/0	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-	-	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-55C/125C	1000 Cycles	-	-	-	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65/150C	500 Cycles	-	3/231/0	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-	3/231/0	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	-	-	-
TC-SAM	A4	-	3	3	Post TC SAM	<50% delamination	-	-	-	-	3/36/0
PTC	A5	JEDEC JESD22-A105	1	45	PTC	-40/125C	1000 Cycles	-	-	1/45/0	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	3/135/0	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	500 Hours	-	-	-	1/45/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	3/135/0	-	3/135/0	-
Test Group B - Accelerated Lifetime Simulation Tests											
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	3/231/0	3/231/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-
Test Group C - Package Assembly Integrity Tests											
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0	3/90/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	1/15/0	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	1/15/0	1/15/0	1/15/0

PD	C4	JEDEC JESD22- B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	3/30/0	3/30/0	3/30/0
Test Group D - Die Fabrication Reliability Tests											
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Tddb	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests											
ESD	E2	AEC Q100- 002	1	3	ESD HBM	-	2000 Volts	-	-	-	1/3/0
ESD	E3	AEC Q100- 011	1	3	ESD CDM	-	500 Volts	-	-	-	1/3/0
LU	E4	AEC Q100- 004	1	3	Latch-Up	Per AEC Q100-004	-	-	-	-	1/6/0
ED	E5	AEC Q100- 009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	-	1/30/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2402-087

[1]-Mechanical damage to the top of the package resulting in a die crack was likely caused by the automated handler due to the unit not seated correctly.

Group 2 Qualification Report

Automotive Qualification Summary

(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Approve Date 28-March-2025

Product Attributes

Attributes	Qual Device: SN5350MCQDWVRQ1	QBS Process, Product Reference: UCC5350MCQDRQ1	QBS Process Reference: ISO5851QDWQ1	QBS Package, Product Reference: ISO6763QDWRQ1	QBS Process, Product Reference: ISO5452DWR
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Power Management	Interface,Power Management	Interface	Interface	Power Management
Wafer Fab Supplier	DP1DM5, DP1DM5	DP1DM5, DP1DM5	MH8, DP1DM5, DP1DM5	RFAB, RFAB	DP1DM5, DP1DM5, MH8
Assembly Site	MLA	MLA	TAI	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	DWV	D	DW	DW	DW
Pin Count	8	8	16	16	16

QBS: Qual By Similarity, also known as Generic Data
Qual Device SN5350MCQDWVRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN5350MCQDWVRQ1	QBS Process, Product Reference: UCC5350MCQDRQ1	QBS Process Reference: ISO5851QDWQ1	QBS Package, Product Reference: ISO6763QDWRQ1	QBS Process, Product Reference: ISO5452DWR
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	1/0/0	3/0/0	3/0/0	1/0/0
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	1/77/0	3/231/0	3/231/0	1/77/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	1/77/0	1/77/0	3/231/0	1/77/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	-	1/77/0	1/77/0	3/231/0	1/77/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	1/77/0	-	3/135/0	1/45/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	1/45/0	-	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	-	3/231/0	-	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	-	3/2400/0	-	-
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	1/30/0	1/30/0	3/90/0	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	1/30/0	1/30/0	3/90/0	-

PD	C4	JEDEC JESD22- B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	1/10/0	1/10/0	-	-
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDb	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ESD	E2	AEC Q100- 002	1	3	ESD HBM	-	2000 Volts	-	1/3/0	1/3/0	-	-
ESD	E3	AEC Q100- 011	1	3	ESD CDM	-	500 Volts	-	1/3/0	1/3/0	-	-
LU	E4	AEC Q100- 004	1	3	Latch-Up	Per AEC Q100-004	-	-	1/6/0	1/6/0	-	-
ED	E5	AEC Q100- 009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	-	1/30/0	1/30/0	3/90/0	1/30/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

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The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

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Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED

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Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2409-068

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in qualifying its changes. For devices to be categorized as a 'product qualification family' for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also known at TI as Qualification by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled "QBS Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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