12500 TI Boulevard, MS 8640, Dallas, Texas 75243

PCN# 20240725001.2
Qualification of MLA as an additional Assembly & Test site for select devices
Change Notification / Sample Request

Date: July 26, 2024
To: MOUSER PCN

Dear Customer:

This is an announcement of a change to a device that is currently offered by Texas Instruments. The details of this change are on the following pages.

Texas Instruments requires acknowledgement of receipt of this notification within **30** days of the date of this notice. Lack of acknowledgement of this notice within 30 days constitutes acceptance and approval of this change. If samples or additional data are required, requests must be received within **30 days** of this notification.

The changes discussed within this PCN will not take effect any earlier than the proposed first ship date on Page 3 of this notification, unless customer agreement has been reached on an earlier implementation of the change.

This notice does not change the end-of-life status of any product. Should product affected be on a previously issued product withdrawal/discontinuance notice, this notification does not extend the life of that product or change the life time buy offering/discontinuance plan.

For questions regarding this notice or to provide acknowledgement of this PCN, you may contact your local Field Sales Representative or the change management team.

For sample requests or sample related questions, contact your local Field Sales Representative.

Sincerely,

Change Management Team
SC Business Services

20240725001.2
Attachment: 1

Products Affected:

The devices listed on this page are a subset of the complete list of affected devices. According to our records**,** you have recently purchased these devices**.** The corresponding customer part number is also listed, if available.

DEVICE	CUSTOMER PART NUMBER
DAC8551AQDGKRQ1	NULL
INA301A1QDGKRQ1	NULL
INA301A1QDGKTQ1	NULL
INA301A2QDGKTQ1	NULL
INA301A3QDGKTQ1	NULL
LM3485Q1MM/NOPB	NULL
LM3489QMM/NOPB	NULL
LM3489QMMX/NOPB	NULL
LMP8278QMM/NOPB	NULL
LMV762QMM/NOPB	NULL
LMV772QMM/NOPB	NULL
OPA1642AQDGKRQ1	NULL
OPA180QDGKRQ1	NULL
OPA188AQDGKRQ1	NULL
OPA192QDGKRQ1	NULL
OPA197QDGKRQ1	NULL
OPA2172QDGKQ1	NULL
OPA2172QDGKRQ1	NULL
OPA2317QDGKRQ1	NULL
OPA2320AQDGKRQ1	NULL
OPA2322AQDGKRQ1	NULL
OPA2333AQDGKRQ1	NULL
OPA2354AQDGKRQ1	NULL
TLV197QDGKRQ1	NULL
TLV2172QDGKRQ1	NULL
TLV2402QDGKRQ1	NULL
TLV2442QDGKRQ1	NULL

Technical details of this Product Change follow on the next page(s).

PCN Number:	20240725001.2	**PCN Date:**	July 26, 2024
Title:	Qualification of MLA as an additional Assembly & Test site for select devices		
Customer Contact:	Change Management team	**Dept:**	Quality Services
Proposed 1st Ship Date:	January 22, 2025	**Sample Requests accepted until:**	August 25, 2024

***Sample requests received after** August 25, 2024 **will not be supported.**

Change Type:

☒	Assembly Site	☐	Design	☐	Wafer Bump Material
☒	Assembly Process	☐	Data Sheet	☐	Wafer Bump Process
☒	Assembly Materials	☐	Part number change	☐	Wafer Fab Site
☐	Mechanical Specification	☒	Test Site	☐	Wafer Fab Material
☒	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing the qualification of MLA as an additional Assembly & Test site for set of devices listed below. Material differences between sites as follows:

Group 1 Device:

	ASESH	HNA	TIEMA	UTL2	MLA
Wire diam/type	1.0mil Au	1.0mil Au	1.0mil Au	1.0mil Au	1.0mil Cu, 0.96mil Au
Mount compound	EY1000063	400180	8075531	PZ0013	4147858
Mold compound	EN2000515	450179	8096859	CZ0094	4211880
Wafer thickness	203um	191um	165.1um/ 215.9um	203um	190um
Lead finish	NiPdAu	NiPdAu	Matte Sn	NiPdAu	NiPdAu
Device marking	Pin 1 dot, backside marking*	Pin 1 dimple	Pin 1 dimple	Pin 1 dimple	TI letter, pin 1 dot, Mold cavity ID, no backside marking
MSL level	2	2	1	3	1

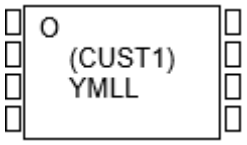
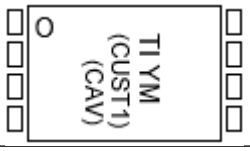
* - Not all devices have TI logo/backside marking included in the symbolization, but for the ones that do, the proposed change applies in MLA.

Group 2 Device:

	ASESH	MLA
Wire diam/type	1.0mil Au	1.0mil Cu, 0.96mil Au
Mount compound	EY1000063	4147858
Mold compound	EN2000515	4226323
Lead finish	NiPdAu	NiPdAu
Wafer thickness	203um	190um
Device marking	Pin1 dot, backside marking	TI letter, Mold cavity ID, pin 1 dimple, no backside marking
MSL level	2	1

Group 3 Device:

	ASESH	MLA
Wire diam/type	1.0mil Au	1.0mil Cu
Mount compound	EY1000063	4147858

Mold compound	EN2000515	4211880
Lead finish	NiPdAu	NiPdAu
Wafer thickness	203um	190um
Device marking		
MSL level	2	1

Test coverage, insertions, conditions will remain consistent with current testing and verified with test MQ.

Reason for Change:

Supply continuity
1) To align with world technology trends and use wiring with enhanced mechanical and electrical properties
2) Maximize flexibility within our Assembly/Test production sites.
3) Cu is easier to obtain and stock

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Impact on Environmental Ratings

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
ASESH	ASH	CHN	Shanghai
HFTF	HFT	CHN	Hefei
TIEMA	CU6	MYS	Melaka
UTL2	NSE	THA	Bangkok
MLA	MLA	MYS	Kuala Lumpur

Sample product shipping label (not actual product label)

Group 1 Product Affected:

LM3485Q1MM/NOPB	LMV762QMM/NOPB	REF3433QDGKRQ1	OPA2172QDGKQ1
LM3489QMM/NOPB	LMV762QMMX/E7002900	REF3440QDGKRQ1	OPA2172QDGKRQ1
LM3489QMMX/NOPB	LMV762QMMX/NOPB	REF3450QDGKRQ1	OPA2322AQDGKRQ1
LMP8278DGKZRQ1	LMV772QMM/NOPB	TLV2402QDGKRQ1	OPA2333AQDGKRQ1
LMP8278QMM/NOPB	LMV772QMMX/E7002761	TLV2442QDGKRQ1	TLV197QDGKRQ1
LMP8278QMME/NOPB	OPA1642AQDGKRQ1	DAC8551AQDGKRQ1	TLV2172QDGKRQ1
LMP8278QMMX/E7002899	OPA2354AQDGKRQ1	OPA180QDGKRQ1	OPA2317QDGKRQ1
LMP8278QMMX/NOPB	REF3425QDGKRQ1	OPA188AQDGKRQ1	
LMV762BQMMX	REF3430QDGKRQ1	OPA197QDGKRQ1	

Group 2 Product Affected:

OPA192QDGKRQ1	OPA2320AQDGKRQ1	OPA2320AQDGKRTW

Group 3 Product Affected:

INA301A1QDGKRQ1	INA301A2QDGKRQ1	INA301A3QDGKRQ1
INA301A1QDGKTQ1	INA301A2QDGKTQ1	INA301A3QDGKTQ1

Qualification Results
Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Approve Date 03-May-2024

Product Attributes

Attributes	Qual Device: LMP8278DGKZRQ1	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1	QBS Process Reference: LMV842QMA/NOPB
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Logic	Logic	Logic	Signal Chain
Wafer Fab Supplier	MAINEFAB	RFAB	RFAB	RFAB	MAINEFAB
Assembly Site	MLA	MLA	MLA	MLA	TIEMA
Package Group	VSSOP	VSSOP	VSSOP	VSSOP	SOIC
Package Designator	DGK	DGS	DGS	DGS	D
Pin Count	8	20	20	20	8

QBS: Qual By Similarity - See Note which applies to Qual Device and all affected products in PCN
Qual Device LMP8278DGKZRQ1 is qualified at MSL1 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: LMP8278DGKZRQ1	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1	QBS Process Reference: LMV842QMA/NOPB
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/Pass	1/Pass	1/Pass	1/Pass	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	Note 1	1/77/0	1/77/0	1/77/0	-

AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	1/77/0	1/77/0	1/77/0	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	1/77/0	1/77/0	1/77/0	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	1/5/0	1/5/0	1/5/0	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	Note 1	1/45/0	1/45/0	1/45/0	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	Note 2	1/77/0	-	-	3/231/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	Note 3	-	-	-	3/2400/0
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	1/15/0	-	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	-	-	-	-
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0 Note 4	-	-	-	-

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
Note 1: HAST and HSTL Package QBS is same Mold, Die attach and Wire package attributes and the manufacturing site is qualified with 3 lots.
Note 2: HTOL Process QBS is same silicon process technology family qualified with 3 lots.
Note 3: ELFR Process QBS is same wafer process technology qualified with 3 lots and generic data allowed per AEC Q100-008.
Note 4: One lot is allowed per AEC-Q100: A1.5.1 Multiple Sites - When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

Qualification Results
Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)
Approve Date 24-June-2024

Product Attributes

Attributes	Qual Device: LMV772QMMX/E7002761	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1	QBS Process Reference: DS90LV019TMX
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Logic	Logic	Logic	Signal Chain
Wafer Fab Supplier	MAINEFAB	RFAB	RFAB	RFAB	MAINEFAB
Assembly Site	MLA	MLA	MLA	MLA	TIEMA
Package Group	VSSOP	VSSOP	VSSOP	VSSOP	SOIC
Package Designator	DGK	DGS	DGS	DGS	D
Pin Count	8	20	20	20	14

QBS: Qual By Similarity - See Note which applies to Qual Device and all affected products in PCN
Qual Device LMV772QMMX/E7002761 is qualified at MSL1 260C

Qualification Results
Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: LMV772QMMX/E7002761	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1	QBS Process Reference: DS90LV019TMX
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/Pass	1/Pass	1/Pass	1/Pass	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	Note 1	1/77/0	1/77/0	1/77/0	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	1/77/0	1/77/0	1/77/0	-
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-	-	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	1/77/0	1/77/0	1/77/0	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	3/15/0	1/5/0	-	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	Note 2	1/45/0	1/45/0	1/45/0	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	Note 3	1/77/0	-	-	3/231/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	Note 4	-	-	-	3/2400/0
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-

SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	Note 5	1/15/0	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	Note 5	1/15/0	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	-	-	-	-
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0 Note 6	-	-	-	-

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

Note 1: HAST Package QBS is same Mold, Die attach and Wire package attributes and the manufacturing site is qualified with 3 lots.
Note 2: HTSL Package QBS is same Mold, Die attach and Wire package attributes and the manufacturing site is qualified with 3 lots.
Note 3: HTOL Process QBS is same silicon process technology family qualified with 3 lots.
Note 4: ELFR Process QBS is same wafer process technology qualified with 3 lots and generic data allowed per AEC Q100-008.
Note 5: PB and PB Free Solderability Package QBS is same lead finish and the manufacturing site is qualified with 1 lot.
Note 6: One lot is allowed per AEC-Q100: A1.5.1 Multiple Sites - When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.
Note 7: HBM, CDM, LU are Not Applicable for Assembly Site Transfer per AEC-Q100, Rev J Table 3

Qualification Results
Automotive Qualification Summary
(As per AEC-Q100 Rev. J and JEDEC Guidelines)
Approve Date 03-May-2024

Product Attributes

Attributes	Qual Device: OPA2197QDGKRQ1	QBS Process Reference: INA301A2QDGKRQ1	QBS Process Reference: INA301A1QDGKRQ1	QBS Process Reference: INA301A3QDGKRQ1	QBS Package Reference: PCM1794AQDBRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain
Wafer Fab Supplier	AIZU	AIZU	AIZU	AIZU	TSMC-WF3
Assembly Site	MLA	ASESHAT	ASESHAT	ASESHAT	MLA
Package Group	VSSOP	VSSOP	VSSOP	VSSOP	SSOP
Package Designator	DGK	DGK	DGK	DGK	DB
Pin Count	8	8	8	8	28

QBS: Qual By Similarity - See Note which applies to Qual Device and all affected products in PCN
Qual Device OPA2197QDGKRQ1 is qualified at MSL1 260C

Qualification Results
Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: OPA2197QDGKRQ1	QBS Process Reference: INA301A2QDGKRQ1	QBS Process Reference: INA301A1QDGKRQ1	QBS Process Reference: INA301A3QDGKRQ1	QBS Package Reference: PCM1794AQDBRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/Pass	-	-	-	3/Pass
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	Note 1	-	-	-	3/231/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-	-	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-	-	-	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	-	-	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	1/45/0	-	-	-	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	408 Hours	Note 2	1/77/0	1/77/0	1/77/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	150C	24 Hours	Note 3	1/800/0	1/800/0	1/800/0	-
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	1/15/0	-	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	-	-	-	-
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements

TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0 Note 4	1/30/0	1/30/0	1/30/0	3/90/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles
Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40C to +150C
Grade 1 (or Q): -40C to +125C
Grade 2 (or T): -40C to +105C
Grade 3 (or I) : -40C to +85C
E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
Quality and Environmental data is available at TI's external Web site: http://www.ti.com/
Note 1: HAST Package QBS is same Mold, Die attach and Wire package attributes and the manufacturing site is qualified with 3 lots.
Note 2: HTOL Process QBS is same silicon process technology family qualified with 3 lots.
Note 3: ELFR Process QBS is same wafer process technology qualified with 3 lots and generic data allowed per AEC Q100-008.
Note 4: One lot is allowed per AEC-Q100: A1.5.1 Multiple Sites - When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

Qualification Results
Automotive Qualification Summary
(As per AEC and JEDEC Guidelines)
Q006 VSSOP at MLA
Approve Date 01-May-2024

Product Attributes

Attributes	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125
Product Function	Logic	Logic	Logic
Wafer Fab Supplier	RFAB	RFAB	RFAB
Assembly Site	MLA	MLA	MLA
Package Group	VSSOP	VSSOP	VSSOP
Package Designator	DGS	DGS	DGS
Pin Count	20	20	20

Qual Device SN74LV244AQDGSRQ1 is qualified at MSL1 260C
Qual Device SN74LV273AQDGSRQ1 is qualified at MSL1 260C
Qual Device SN74LV541AQDGSRQ1 is qualified at MSL1 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: SN74LV244AQDGSRQ1	Qual Device:: SN74LV273AQDGSRQ1	Qual Device: SN74LV541AQDGSRQ1
Test Group A - Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	1/Pass	1/Pass	1/Pass
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	1/22/0	1/22/0	1/22/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	1/22/0	1/22/0	1/22/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	1/77/0	1/77/0	1/77/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	1/77/0	1/77/0	1/77/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	1/22/0	1/22/0	1/22/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	1/77/0	1/77/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	1/22/0	1/22/0	1/22/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	1/3/0	1/3/0	1/3/0

TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	1/77/0	1/77/0	1/77/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	1/22/0	1/22/0	1/22/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	1/45/0	1/45/0	1/45/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	1/45/0	1/45/0	1/45/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
Test Group C - Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0

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ZVEI ID: SEM-PA-07, SEM-PA-08, SEM-PA-11, SEM-PA-13, SEM-PA-18, SEM-PS-02, SEM-PS-04, SEM-TF-01

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