



12500 TI Boulevard, MS 8640, Dallas, Texas 75243

**PCN#20240618001.2**

**Qualification of RFAB using qualified Process Technology, Die Revision, Datasheet  
and Assembly BOM options for select devices  
Change Notification / Sample Request**

**Date:** June 19, 2024

**To:** MOUSER PCN

Dear Customer:

This is an announcement of a change to a device that is currently offered by Texas Instruments. The details of this change are on the following pages.

Texas Instruments requires acknowledgement of receipt of this notification within **30** days of the date of this notice. Lack of acknowledgement of this notice within 30 days constitutes acceptance and approval of this change. If samples or additional data are required, requests must be received within **30 days** of this notification.

The changes discussed within this PCN will not take effect any earlier than the proposed first ship date on Page 3 of this notification, unless customer agreement has been reached on an earlier implementation of the change.

This notice does not change the end-of-life status of any product. Should product affected be on a previously issued product withdrawal/discontinuance notice, this notification does not extend the life of that product or change the life time buy offering/discontinuance plan.

For questions regarding this notice or to provide acknowledgement of this PCN, you may contact your local Field Sales Representative or the change management team.

For sample requests or sample related questions, contact your local Field Sales Representative.

Sincerely,

Change Management Team  
SC Business Services

**20240618001.2**  
**Attachment: 1**

**Products Affected:**

The devices listed on this page are a subset of the complete list of affected devices. According to our records, you have recently purchased these devices. The corresponding customer part number is also listed, if available.

DEVICE	CUSTOMER PART NUMBER
UCC21520AQDWRQ1	NULL
UCC21520QDWRQ1	NULL

Technical details of this Product Change follow on the next page(s).

<b>PCN Number:</b>	20240618001.2	<b>PCN Date:</b>	June 19, 2024
<b>Title:</b>	Qualification of new Die Revision in RFAB using qualified Process Technology, Die Revision, Datasheet and Assembly BOM options for select devices		
<b>Customer Contact:</b>	Change Management Team	<b>Dept:</b>	Quality Services
<b>Proposed 1<sup>st</sup> Ship Date:</b>	December 16, 2024	<b>Sample requests accepted until:</b>	July 19, 2024*

\*Sample requests received after July 19, 2024 will not be supported.

Change Request Received after July 20, 2021 will not be supported:

Change Type:					
<input type="checkbox"/>	Assembly Site	<input checked="" type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Material
<input checked="" type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet	<input type="checkbox"/>	Wafer Bump Process
<input checked="" type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input checked="" type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site	<input checked="" type="checkbox"/>	Wafer Fab Material
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process	<input checked="" type="checkbox"/>	Wafer Fab Process

## PCN Details

### Description of Change:

Texas Instruments is pleased to announce the addition of RFAB using the LBC8LV-ISO.2 qualified process technology and additional Assembly BOM options for the devices listed below.

Current Fab Site			Additional Fab site		
Current Fab Site	Process	Wafer Diameter	Additional Fab site	Process	Wafer Diameter
MIHO8/DMOS5	LBC8LV-ISO.1	200mm	RFAB	LBC8LV-ISO.2	300mm

The die was also changed as a result of the process change.

Construction differences are as follows:

	Current	New
Bond wire diam/type	0.96mil Au, 1.0mil Cu	0.8mil Cu
Wafer thickness	15mils	10.5mils

This particular PCN is related to TI's transition of dual-channel isolated gate drivers in wide body package (16DW) to a newly-designed circuit and to TI's most efficient manufacturing processes and technology. The newly-designed circuit includes improvements to robustness in common automotive and industrial applications. Changes in the datasheet are summarized in the table below and the new datasheet is available at [www.ti.com/product/UCC21520-Q1](http://www.ti.com/product/UCC21520-Q1). TI additionally offers a transition guide to ensure complete understanding of system considerations which is available upon request in the SDP (supporting data package). The changes to the manufacturing processes and technology underscore our commitment to product longevity and supply continuity.

Qual details are provided in the Qual Data Section.

The datasheets will be changing as a result of the above mentioned changes. The datasheet change details can be reviewed in the datasheet revision history. The links to the revised datasheets are available in the table below.



**UCC21520-Q1**

SLUSCQ2E – OCTOBER 2017 – REVISED JUNE 2024

## Changes from Revision D (June 2020) to Revision E (June 2024) Page

• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Deleted 5ns maximum delay matching from Features section.....	1
• Changed Typ propagation delay from 19ns to 33ns.....	1
• Changed 10ns minmum pulse width to 20ns.....	1
• Changed operating temperature range to junction temeperature range.....	1
• Changed CMTI specification from 100V/ns to 125V/ns.....	1
• Changed surge immunity value from 12.8kV to 10kV.....	1
• Deleted "Rejects input pulses and noise transients shorter than 5ns".....	1
• Deleted HBM and CDM ESD classification levels in Features.....	1
• Updated safety certifications to latest standards.....	1
• Updated Description section to match new spec values.....	1
• Updated DT pin description to recommend $\leq 1\text{nF}$ capacitor on DT pin.....	3
• Changed DT pin Min resistor recommendations from $500\Omega$ to $2\text{k}\Omega$ .....	3
• Updated ESD spec from HBM = $\pm 4000$ and CDM = $\pm 1500$ to HBM = $\pm 2000$ and CDM = $\pm 1000$ to match ESD industry standards.....	4
• Deleted ambient temperature spec.....	4
• Changed Max junction temp to $150^\circ\text{C}$ .....	4
• Updated values from $R_{\theta\text{JA}} = 67.3^\circ\text{C/W}$ , $R_{\theta\text{JC}}(\text{top}) = 34.4^\circ\text{C/W}$ , $R_{\theta\text{JB}} = 32.1^\circ\text{C/W}$ , $\psi_{\text{JT}} = 18^\circ\text{C/W}$ , $\psi_{\text{JB}} = 31.6^\circ\text{C/W}$ to $R_{\theta\text{JA}} = 69.8^\circ\text{C/W}$ , $R_{\theta\text{JC}}(\text{top}) = 33.1^\circ\text{C/W}$ , $R_{\theta\text{JB}} = 36.9^\circ\text{C/W}$ , $\psi_{\text{JT}} = 22.2^\circ\text{C/W}$ , $\psi_{\text{JB}} = 36^\circ\text{C/W}$ .....	4
• Updated values from $\text{PD} = 1.05\text{W}$ , $\text{PDI} = 0.05\text{W}$ , $\text{PDA/PDB} = 0.5\text{W}$ to $\text{PD} = 950\text{mW}$ , $\text{PDI} = 50\text{mW}$ , $\text{PDA/PDB} = 450\text{mW}$ .....	5
• Updated values from $\text{DTI} = >21\text{mm}$ , $\text{VIOSM} = 8000\text{VPK}$ to $\text{DTI} = >17\text{mm}$ , $\text{VIOSM} = 10000\text{VPK}$ and added $\text{VIMP} = 7692\text{VPK}$ .....	6
• Deleted safety related certifications section.....	6
• Updated values from $\text{IS} = 75\text{mA}/36\text{mA}$ , $\text{PS} = 50\text{mW}/900\text{mW}/900\text{mW}/1850\text{mW}$ to $\text{IS} = 58\text{mA}/34\text{mA}$ , $\text{PS} = 50\text{mW}/870\text{mW}/870\text{mW}/1790\text{mW}$ .....	7
• Updated $\text{IVDDA}/\text{IVddb}$ quiescent current spec Max value from $1.8\text{mA}$ to $2.5\text{mA}$ .....	7
• Updated $\text{IVCCI}$ operating current Typ value from $2.0\text{mA}$ to $3.0\text{mA}$ and added Max value $3.5\text{mA}$ .....	7
• Added $\text{IVDDA}/\text{IVddb}$ operating current Max = $4.2\text{mA}$ .....	7
• Updated values from Rising threshold Min = $8.3\text{V}$ , Typ = $8.7\text{V}$ , Max = $9.2\text{V}$ to Min = $7.7\text{V}$ , Typ = $8.5\text{V}$ , Max = $8.9\text{V}$ .....	7
• Updated values from Falling threshold Min = $7.8\text{V}$ , Typ = $8.2\text{V}$ , Max = $8.7\text{V}$ to Min = $7.2\text{V}$ , Typ = $7.9\text{V}$ , Max = $8.4\text{V}$ .....	7
• Updated 8-V UVLO hysteresis typ = $0.5\text{V}$ to $0.6\text{V}$ .....	7
• Updated Input high threshold Min value from $1.6\text{V}$ to $1.2\text{V}$ .....	7
• Deadtime parameter broken to a its own table and added more parameters.....	8
• Changed propagation delay $\text{TPDHL}$ and $\text{TPDLH}$ from Typ = $19\text{ns}$ , Max = $30\text{ns}$ to Typ = $33\text{ns}$ , Max = $45\text{ns}$ and adding Min = $26\text{ns}$ .....	8
• Changed propagation delay matching from Max = $5\text{ns}$ to Max = $6.5\text{ns}$ from $\text{TJ} = -40^\circ\text{C}$ to $-10^\circ\text{C}$ and Max = $5\text{ns}$ from $\text{TJ} = -10^\circ\text{C}$ to $150^\circ\text{C}$ .....	8
• Added $\text{VCCI}$ power up delay.....	8
• Updated $\text{VDDA}/\text{Vddb}$ power-up delay from Max = $100\mu\text{s}$ to $10\mu\text{s}$ .....	8
• Updated CMTI from Min = $100\text{V/ns}$ to $125\text{V/ns}$ .....	8
• Updated insulation curves to match updated characteristics.....	9
• Updated typical characteristics figures.....	10
• Updated Power-up UVLO Delay to OUTPUT section to match device electrical characteristics.....	15
• Changed the Functional Block Diagram to add deglitch filter block.....	17
• Added paragraph on minimum pulse width to Output Stage section.....	21
• Updated DT Pin Connected to a Programming Resistor Between DT and GND Pins section to recommend $<1\text{nF}$ capacitor on DT pin.....	23
• Updated typical schematic DT pin capacitor recommendation.....	25
• Updated Dead Time Setting Guidelines section to recommend $<1\text{nF}$ capacitor on DT pin.....	32

Product Folder	Current Datasheet Number	New Datasheet Number	Link to full datasheet
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UCC21520-Q1	SLUSCQ2D	SLUSCQ2E	<a href="http://www.ti.com/product/ucc21520-q1">http://www.ti.com/product/ucc21520-q1</a>
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### Reason for Change:

#### Continuity of Supply

These changes are to transition TI's dual-channel isolated gate drivers in wide body package (16DW) to TI's most efficient manufacturing processes and technology, underscoring our

commitment to product longevity and supply continuity. Additionally, the newly-designed circuit includes improvements to robustness in common automotive and industrial applications, underscoring our commitment to continuous improvements in both product quality and end system robustness.

**Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):**

None

**Impact on Environmental Ratings**

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

**RoHS**

☒ No Change

**REACH**

☒ No Change

**Green Status**

☒ No Change

**IEC 62474**

☒ No Change

**Changes to product identification resulting from this PCN:**

**Fab Site**

**Information:**

Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
MIHO8	MH8	JPN	Ibaraki
DMOS5	DM5	USA	Dallas
<b>RFAB</b>	<b>RFB</b>	<b>USA</b>	<b>Richardson</b>


**Die Rev:**

**Current**

**New**

Die Rev [2P]	Die Rev [2P]
<b>B</b>	<b>A</b>

Sample product shipping label (not actual product label)

 **TEXAS INSTRUMENTS**  
MADE IN: Malaysia  
2DC: 2Q:  
MSL 2 /260C/1 YEAR SEAL DT  
MSL 1 /235C/UNLIM 03/29/04  
OPT:  
ITEM: 39  
LBL: 5A (L)T0:1750



(1P) SN74LS07NSR  
(Q) 2000 (D) 0336  
(31T) LOT: 3959047MLA  
(4W) TKY (1T) 7523483SI2  
(P)  
(2P) REV: (V) 0033317  
(20L) CSO: SHE (21L) CCO:USA  
(22L) ASO: MLA (23L) ACO: MYS

**Product Affected**

UCC21520AQDWRQ1	UCC21520QDWRQ1
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# Qualification Report

## Automotive Qualification Summary (As per AEC-Q100 Rev. J and JEDEC Guidelines) Approve Date 18-June-2024

### Product Attributes

Attributes	Qual Device: <u>UCC21520QDWRQ1</u>	QBS Process Reference: <u>UCC23513QDWYQ1</u>	QBS Product Reference: <u>UCC21551CQDWKRQ1</u>	QBS Package Reference: <u>ISO6763QDWRQ1</u>
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Power Management	Power Management	Power Management	Interface
Wafer Fab Supplier	RFAB, RFAB, RFAB	RFAB, RFAB	RFAB, RFAB, RFAB	RFAB, RFAB
Assembly Site	MLA	TAI	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC
Package Designator	DW	DWY	DWK	DW
Pin Count	16	6	14	16

QBS: Qual By Similarity

Qual Device UCC21520QDWRQ1 is qualified at MSL3 260C

### Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <u>UCC21520QDWRQ1</u>	QBS Process Reference: <u>UCC23513QDWYQ1</u>	QBS Product Reference: <u>UCC21551CQDWKRQ1</u>	QBS Package Reference: <u>ISO6763QDWRQ1</u>
Test Group A - Accelerated Environment Stress Tests											
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	-	-	-	No Fails
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	-	No Fails	-	No Fails	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	1/77/0	-	1/77/0	3/231/0
AC/UHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	-	1/77/0	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	-	1/77/0	3/231/0
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	-	1/5/0	-
TC-SAM	A4	-	3	3	Post TC SAM	<50% delamination	-	1/12/0	-	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	1/45/0	3/135/0
Test Group B - Accelerated Lifetime Simulation Tests											
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	-	3/231/0	1/77/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-
Test Group C - Package Assembly Integrity Tests											



Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: UCC21520QDWRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Product Reference: UCC21551CQDWKRQ1	QBS Package Reference: ISO6763QDWRQ1
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	3/90/0	1/30/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	3/90/0	1/30/0	3/90/0
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	1/15/0	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	1/15/0	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	1/10/0	3/30/0	1/10/0	-

#### Test Group D - Die Fabrication Reliability Tests

EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDb	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements

#### Test Group E - Electrical Verification Tests

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: UCC21520QDWRQ1	QBS Process Reference: UCC23513QDWYQ1	QBS Product Reference: UCC21551CQDWKRQ1	QBS Package Reference: ISO6763QDWRQ1
ESD	E2	AEC Q100-002	1	3	ESD HBM	-	2000 Volts	1/3/0	1/3/0	1/3/0	-
ESD	E3	AEC Q100-011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	1/3/0	-
LU	E4	AEC Q100-004	1	6	Latch-Up	Per AEC Q100-004	-	1/3/0	1/6/0	1/6/0	-
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	3/90/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

#### Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

#### E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

**Automotive Qualification Summary**  
**(As per AEC-Q100, Q006 and JEDEC Guidelines)**  
 Approve Date 19-OCTOBER -2023

**Product Attributes**

Attributes	Qual Device: ISO6763QDWRQ1	Qual Device: UCC21540QDWKRQ1	QBS Package Reference: PUCC21550ADWKR
Automotive Grade Level	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125
Wafer Fab Supplier	RFAB, RFAB	MH8, MH8, MH8	DMOS6, DMOS6, MH8
Assembly Site	MLA	TAI	TAI
Package Group	SOIC	SOIC	SOIC
Package Designator	DW	DWK	DWK
Pin Count	16	14	14

**Qualification Results**

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO6763QDWRQ1	Qual Device: UCC21540QDWKRQ1	QBS Reference: PUCC21550ADWKR
Test Group A - Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL2 260C	-	3/597/0	1/199/0	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL3 260C	-	-	-	3/693/0
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	3/66/0	1/22/0	3/66/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	3/66/0	1/22/0	3/66/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	3/231/0	1/77/0	3/231/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	3/3/0	1/1/0	-
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	3/210/0	1/70/0	3/210/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	3/66/0	1/22/0	3/66/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	3/3/0	1/1/0	3/3/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	3/9/0	1/3/0	3/9/0



Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO6763QDWRQ1	Qual Device: UCC21540QDWKRQ1	QBS Reference: PUCC21550ADWKR
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-55C/150C	1000 Cycles	-	-	3/231/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	1/77/0	-
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	3/66/0	1/22/0	3/66/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	3/3/0	1/1/0	-
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-55C/150C	2000 Cycles	-	-	3/210/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	3/210/0	1/70/0	-
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	3/66/0	1/22/0	3/66/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	3/3/0	1/1/0	3/3/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	3/9/0	1/3/0	3/9/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	3/135/0	1/45/0	-
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	175C	500 Hours	-	-	3/231/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	3/3/0	1/1/0	3/3/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	3/132/0	1/44/0	-
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	175C	1000 Hours	-	-	3/228/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	3/3/0	1/1/0	3/3/0
Test Group C - Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0

QBS: Qual By Similarity

Qual Device ISO6763QDWRQ1 is qualified at MSL2 260C

Qual Device UCC21540QDWKRQ1 is qualified at MSL3 260C

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

**Ambient Operating Temperature by Automotive Grade Level:**

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

**E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):**

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

ZVEI ID: SEM-DE-03, SEM-DE-01, SEM-DE-02, SEM-PW-02, SEM-PW-09, SEM-PW-13, SEM-PW-03, SEM-PA-08

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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