12500 TI Boulevard, MS 8640, Dallas, Texas 75243

Notification Number:	20260731001.0	Notification Issued	August 11, 2026
Datasheet for AM243x, AM62Px, AM273x, AM62Ax, and AM275x			

Change Type(s)	Data Sheet/Electrical Specification
ZVEI ID	SEM-DS-02

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

Changes from December 22, 2025 to June 3, 2026 (from Revision H (DECEMBER 2025) to Revision I (June 2026)) **Page**

- **Global:** Added ANI package option support to the device....1
- (Features): Added details for the new ANI package option....1
- (Device Comparison): Added a note clarifying that features availability may vary by package....7
- (Power-On Hours): Removed note referencing an application report....104
- (Speed Grade Maximum Frequency): Added ANI package option to the table....107
- (Thermal Resistance Characteristics): Added ANI package option to the table....118
- (MCU_OSC0 Switching Characteristics - Crystal Mode): Added ANI package option to the table....136
- (GPMC): Widened range of output load capacitance. Specified separate ranges for 133MHz Synchronous Mode and All other modes....160
- (GPMC and NOR Flash Timing Requirements — Synchronous Mode): Simplified MODE column to include only div_by_1_mode and not_div_by_1_mode. Changed column headers from GPMC_FCLK = 100MHz/ 133MHz to 32-bit data bus (up to 100MHz)/16-bit data bus (up to 133MHz). Simplified several parameter descriptions. Updated pin names to match Pin Attributes table. Updated the table notes. 160
- (GPMC and NOR Flash Switching Characteristics – Synchronous Mode): Removed the MODE column. Combined the GPMC_FCLK=100MHz and GPMC_FCLK=133MHz columns. Reduced F2 and F3 clk-csn maximum output delays. Changed the timing variable in parameters F3 and F11 to "D". Removed 2 of the F7 rows. Removed the "J" timing variable from the F15 and F17 parameters. Added byte enables for 32-bit data bus to F6, F7, F17, F19. Simplified several parameter descriptions. Updated pin names to match Pin Attributes table. Updated the table notes....160
- (GPMC and NOR Flash Timing Requirements – Asynchronous Mode): Removed the MODE column and the table note that described register configuration for div_by_1_mode. Added the correct table note for parameter FA21 169
- (GPMC and NOR Flash Switching Characteristics – Asynchronous Mode): Removed the MODE column and redundant rows. Also removed the table note that described register configuration for div_by_1_mode. Moved links to table notes directly next to each letter. 169
- (GPMC and NAND Flash Timing Requirements – Asynchronous Mode): Removed the MODE column and the table note that described register configuration for div_by_1_mode....176
- (GPMC and NAND Flash Switching Characteristics – Asynchronous Mode): Removed the MODE column and the table note that described register configuration for div_by_1_mode. Added table notes and associated reference links for timing variables A, B, C, D, E, F, G, H, I, K, L, and M....176
- (MCSPI Switching Characteristics – Peripheral Mode): Updated values for parameters SS6 and SS7....187
- (Device Naming Convention): Updated Package Designator row (added ANI package option)....261

Changes from October 24, 2025 to April 22, 2026 (from Revision C (OCTOBER 2025) to Revision D (APRIL 2026)) **Page**

- (Features): Removed Functional Safety-Compliant targeted [Industrial] and IEC 61508 SIL 2 support features....1
- (Description): Removed IEC 61508 SIL 2 support....4
- (Signal Descriptions): Updated PIN TYPE to SIGNAL TYPE column name for all Signal Description tables within this document....46
- (Absolute Maximum Ratings): Updated the reference to the parameter name from "Steady State Max. Voltage at all IO pins" to "Steady-state max voltage at all other IO pins"....79
- (Detailed Description): Removed IEC 61508 SIL 2 support....207
- (Power Supply Designs): Removed IEC 61508 SIL 2 support....217

Changes from June 6, 2025 to July 30, 2026 (from Revision C (June 2025) to Revision D (July 2026)) **Page**

- (Applications): Updated list and links....2
- Absolute Maximum Ratings: Renamed VIN_18CLK to VIOIN_18CLK to align with the power-rail naming used in the Pin Attributes table....51
- Recommended Operating Conditions: Renamed VIN_18CLK to VIOIN_18CLK, VIN_18ADC to VIOIN_18ADC, and VIN_18CSI to VIOIN_18CSI to align with the power-rail naming used in the Pin Attributes table....52
- Buffer Type - Table: Renamed VIN_18CLK to VIOIN_18CLK and VIN_18ADC to VIOIN_18ADC to align with the power-rail naming used in the Pin Attributes table....54
- Added new Electrical Characteristics section and moved the GPADC Parameters table to this section. Added clarification note to the table....56
- Power Supply Sequencing and Reset Timing: Updated device startup sequence description and diagram. Updated tMSS_BOOT_START description. Removed tH_SOP from the Device Wake-up and Power-Down Sequence diagram....57
- External Clock Mode Input Requirements: Updated DC-VIL.max and DC-VIH.min values. Removed DC-VIH.max value. Added table note (1) associated with the VDD power-supply parameter....59
- MIBSPI Peripheral: Updated the name of the SPIGCRx.0 bit to nRESET to match the TRM....64
- Added MCASP timing parameters....82

Changes from June 20, 2025 to April 21, 2026 (from Revision D (JUNE 2025) to Revision E (APRIL 2026)) **Page**

- (Features): Removed Functional Safety-Compliant targeted [Industrial] features and IEC 61508 SIL 2 support....1
- (Related Products): Removed IEC 61508 SIL 2 functional safety support for industrial applications....8
- (Pin Attributes - PADCONFIG149 and PADCONFIG150): Updated PADCONFIG149 and PADCONFIG150 addresses to (0x000F4254) and (0x000F4258) respectively....14
- (Signal Descriptions): Updated PIN TYPE to SIGNAL TYPE column name for all Signal Description tables within this document....46
- (MMC2 Signal Descriptions): Added Note 2 to the MMC2_SDCD and MMC2_SDWP signals....65
- (UART1 Signal Descriptions): Updated the description of UART1_DCDn signal to "Data Carrier Detect (active low)"....72
- (Connectivity Requirements): Updated the Connection Requirements descriptions for CSI0 balls to clarify connectivity expectations when not using all four lanes....75
- (Absolute Maximum Ratings): Updated the reference to the parameter name from "Steady State Max. Voltage at all IO pins" to "Steady-state max voltage at all other IO pins"....79
- (Recommended Operating Conditions for OTP eFuse Programming): Removed the OPP NOM (BOOT) reference from the VDD_CORE parameter description....91
- (Thermal Resistance Characteristics): Added Note....92
- (CPTS): Updated reference name for the TRM section under the timing tables....128
- (ECAP – Timing Requirements and Switching Characteristics): Updated the clock source referenced in table note 1....133
- (EPWM – Timing Requirements and Switching Characteristics): Updated the clock source referenced in table note 1....136
- (EQEP – Timing Requirements): Updated the clock source referenced in table note 1....138
- (GPMC and NOR Flash Timing Requirements — Synchronous Mode): Removed the GPMC_FCLK=100MHz column timing values and the associated not_div_by_1_mode timing values for GPMC_FCLK=133MHz. Simplified several parameter descriptions. Also removed two table notes, one that described register configuration for GPMC_FCLK selection, and another that described register configuration for div_by_1_mode....140
- (GPMC and NOR Flash Switching Characteristics – Synchronous Mode): Removed the GPMC_FCLK=100MHz column timing values and the associated not_div_by_1_mode timing values for GPMC_FCLK=133MHz. Simplified several parameter descriptions. Changed the timing variable in parameters F3 and F11 to "D". Removed the "J" timing variable from the F15 and F17 parameters. Updated the table notes....140
- (GPMC and NOR Flash Timing Requirements – Asynchronous Mode): Removed the MODE column and the table note that described register configuration for div_by_1_mode. Added the correct table note for parameter FA21....148
- (GPMC and NOR Flash Switching Characteristics – Asynchronous Mode): Removed the MODE column and redundant rows. Also removed the table note that described register configuration for div_by_1_mode....148
- (GPMC and NAND Flash Timing Requirements – Asynchronous Mode): Removed the MODE column and the table note that described register configuration for div_by_1_mode....155
- (GPMC and NAND Flash Switching Characteristics – Asynchronous Mode): Removed the MODE column and the table note that described register configuration for div_by_1_mode. Added table notes and associated reference links for timing variables B, C, D, E, F, G, H, I, K, L, and M....155
- (I2C): Changed the supported speeds and exception descriptions so they are organized based on IO buffer type rather than I2C port instance....158
- (MCAN): Updated reference name for the TRM section under the timing tables....160
- (MCASP): Changed the IOSET note that explains timing limitations associated with valid pin combinations....161

- (MCSPI): Changed the IOSET note that explains timing limitations associated with valid pin combinations. 165
- (HS200 Mode): Added "MMC0 Timing Requirements..... 177
- (Detailed Description – A53SS): Added clarification regarding the A53SS features supported by the device..... 211
- (Detailed Description – DMSS): Added reference to the TRM to ensure consistency with the structure and formatting of other sections in the datasheet..... 213
- (Detailed Description – PDMA): Added clarification regarding the PDMA features supported by the device. 213
- (Detailed Description – CPSW3G): Added clarification regarding the CPSW3G features supported by the device..... 215
- (Detailed Description – ECAP): Added clarification regarding the ECAP features supported by the device.. 215
- (Detailed Description – ELM): Added clarification regarding the ELM features supported by the device..... 215
- (Detailed Description – EPWM): Added clarification regarding the EPWM features supported by the device..... 215
- (Detailed Description – EQEP): Added clarification regarding the EQEP features supported by the device. 216
- (Detailed Description – GPIO): Added clarification regarding the GPIO features supported by the device... 216
- (Detailed Description – GTC): Added clarification regarding the GTC features supported by the device..... 217
- (Detailed Description – I2C): Updated the first sentence to ensure consistency with the structure and formatting of other sections in the datasheet and updated the I/O buffer references..... 217
- (Detailed Description – MCAN): Added clarification regarding the MCAN features supported by the device..... 217
- (Detailed Description – McASP): Removed the first sentence to ensure consistency with the structure and formatting of other sections in the document..... 217
- (Detailed Description – MCSPI): Added clarification regarding the MCSPI features supported by the device..... 218
- (Detailed Description – MMCSD): Added clarification regarding the MMCSD features supported by the device..... 218
- (Detailed Descriprion - OSPI): Added clarification regarding the OSPI features supported by the device.....218
- (Detailed Description – Timers): Added clarification regarding the Timers features supported by the device218
- (Detailed Description – UART): Added clarification regarding the UART features supported by the device.. 219
- (Detailed Description – USBSS): Added clarification regarding the USBSS features supported by the device..... 219
- (Tools and Software): Added clarification regarding the SysConfig features..... 233

Changes from July 31, 2025 to April 21, 2026 (from Revision A (July 2025) to Revision B (April 2026)) **Page**

- Features: Updated OSPI XIP support..... 1
- Description: Removed non-Q1 qualified part numbers..... 3
- (Signal Descriptions): Updated PIN TYPE to SIGNAL TYPE column name for all Signal Description tables within this document..... 39
- Recommended Operating Conditions: Removed VDDA18 analog power supply..... 59
- Device Speed Grades: Renamed the section from ‘Operating Performance Points’ to more accurately reflect that the table in this section lists the device’s speed grades..... 59
- MMC0 - eMMC/SDIO Interface: Removed HS400 row in MMC0 DLL Delay Mapping for all eMMC Timing Modes table..... 127
- MMC0 - eMMC/SDIO Interface: Updated table "*MMC0 DLL Delay Mapping for all eMMC Timing Modes*" by splitting it into two separate tables to improve clarity and alignment with interface specifications for SD/SDIO and eMMC interface modes..... 127
- Functional Block Diagram, Section 7.2: Removed the Functional Block Diagram in this section as it duplicates the content already presented in Section 3.1..... 146
- Standard Package Symbolization: Updated figure *Printed Device Reference* 157
- Device Naming Convention: Clarified Base production part number in the table..... 158

The datasheet number will be changing.

Device Family	Change From:	Change To:
AM243x	SPRSP65G	**SPRSP65H**
AM62Px	SPRSP89C	**SPRSP89D**
AM273x	SWRS245C	**SWRS245D**
AM62Ax	SPRSP77D	**SPRSP77E**
AM275x	SPRSPB0A	**SPRSPB0B**

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/AM2434

http://www.ti.com/product/AM62P

http://www.ti.com/product/AM2732

http://www.ti.com/product/AM62A7
http://www.ti.com/product/AM2754-Q1

Reason for Change:	To accurately reflect device characteristics.

Anticipated impact on Form, Fit, Function, Quality or Reliability:	None
Changes to product identification resulting from this PCN:	None

Products Affected:		
AM2432BSEFHIALXR	XAM2434BSFFHIANI	AM2431BSDGHIALVR
AM2434BSEFHIALXR.B	AM2432BKEGHIALXR	AM2431BSDGHIALVR.B
AM2432BKFGHIALXR.B	AM2432BSDFHIALVR	AM2434BSDFHIALXR.B
AM2432BSFFHIALVR	AM2432BSDFHIALXR.B	AM2434BSFFHIALXR
AM2432BSFFHIALVR.B	AM2432BSFFHIALXR.B	AM2432BSDGHIALVR.B
AM2431BSDGHIALXR	AM2431BSDGHIALXR.B	AM2432BSEFHIALXR.B
AM2434BSDFHIALVR.B	AM2434BSDFHIALVR	AM2432BSFFHIALXR
AM2434BSDFHIALXR	AM2434BSDGHIALXR	AM2431BSDFHIALXR
AM2434BSEFHIALXR	AM2434BSDGHIALXR.B	AM2434BSEFHIALVR
AM2434BSFFHIANIR	AM2434BSFFHIALVR.B	AM2434BSEFHIALVR.B
AM2432BSDGHIALXR.B	AM2432BSDGHIALVR	AM2432BKFGHIALXR
AM2432BSEFHIALVR	AM2434BSDGHIALVR.B	AM2432BSDGHIALXR
AM2432BSEFHIALVR.B	AM2432BKEGHIALXR.B	AM2431BKDGHIALXR
AM2431BSDFHIALVR	AM2432BSDFHIALVR.B	AM2431BSDFHIALVR.B
AM2431BSDFHIALXR.B	AM2432BSDFHIALXR	AM2434BSDGHIALVR
AM2434BSFFHIALVR	AM2431BKDGHIALXR.B	AM2434BSFFHIALXR.B
AM62P34CSMSIAMHRQ1	AM62P52BSMSIAMHRQ1	AM62P52CSMSIAMHRQ1
AM62P54BVMSIAMHRQ1	AM62P54BVMSIAMHRQ1.B	AM62P54CVMSIAMHRQ1
XAM62P54CVMHIAMH	XAM62P54CWMSIAMHR	AM2732ADRFGQZCERQ1.B
AM2731CLSFHQNZNRQ1	AM2731CLSFHQNZNRQ1.B	AM2732CDRFHQZCERQ1
AM2731CASFHQNZNRQ1	AM2731CNSFHQNZNRQ1	AM2731CASFHQNZNRQ1.B
AM2732CMSFHQNZNRQ1	XAM2732BDRFHQZCE	AM2732CMSFHQNZNRQ1.B
AM2731CNSFHQNZNRQ1.B	AM2732CDRFHQZCERQ1.A	XAM2732BMSFHQNZN

AM2732CDRFHQZCERQ1.B	AM2732ADRFGQZCERQ1	AM62A12AQMSIANFRQ1
AM62A12AQMSIANFRQ1.B	AM62A12AQMSIAMBRQ1	AM62A74AUMSIANFRQ1
AM62A74AUMSIANFRQ1.B	AM62A32ASMSIAMBRQ1.B	AM62A12AQMSIAMBRQ1.B
AM62A32ASMSIANFRQ1	AM62A34ASMSIANFRQ1.B	AM62A74AVMSIANFRQ1
AM62A34ASMSIAMBRQ1	AM62A74AUMSIAMBRQ1	AM62A32ASMSIAMBRQ1
AM62A34ASMSIAMBRQ1.B	AM62A74AUMSIAMBRQ1.B	AM62A34AMLSIAMBRQ1
AM62A34ASMSIANFRQ1	AM27521AAZIANJRQ1	AM27521ABZIANJRQ1
AM27522ACZIANJRQ1	AM27542ADZIANJRQ1	AM27542AEZIANJRQ1
AM27542AFZIANJRQ1		

In performing change qualifications, Texas Instruments follows integrated circuit industry standards in performing defect mechanism analysis and failure mechanism-based accelerated environmental testing to ensure wafer fab process, assembly process and product quality and reliability. As encouraged by these standards, TI uses both product-specific and generic (family) data in qualifying its changes. For devices to be categorized as a 'product qualification family' for generic data purposes, they must share similar product, wafer fab process and assembly process elements. The applicability of generic data (also known at TI as Qualification by Similarity (QBS)) is determined by the Reliability Engineering function following these industry standards. Generic data is shown in the qualification report in columns titled "QBS Process" (for wafer fab process), "QBS Package" (for assembly process) and "QBS Product" (for product family).

For questions regarding this notice, e-mails can be sent to the contact shown below or your local Field Sales Representative.