12500 TI Boulevard, MS 8640, Dallas, Texas 75243

Notification# 20251015003.0
Datasheet for MSPM0G310x, MSPM0G150x, MSPM0G110x, MSPM0G350x, MSPM0G310x-Q1, MSPM0G350x-Q1
Information Only

Date: October 23, 2025
To: MOUSER PCN

Dear Customer:

This is an information-only announcement of a change to a device that is currently offered by Texas Instruments.

The changes discussed within this notification are for your information only.

Any negotiated alternative change requirements will be provided via the customer's defined process. Customers with previously negotiated, special requirements will be handled separately. Any inquiries should be directed to your local Field Sales Representative.

For questions regarding this notice, contact your local Field Sales Representative or the Change Management team.

Sincerely,

Change Management Team
SC Business Services

20251015003.0
Information Only Datasheet
Attachments

Products Affected:

The devices listed on this page are a subset of the complete list of affected devices. According to our records**,** you have recently purchased these devices**.** The corresponding customer part number is also listed, if available.

DEVICE	CUSTOMER PART NUMBER
MSPM0G3507SPMR	NULL
MSPM0G1507SPTR	NULL
MSPM0G1107TDGS28R	NULL
MSPM0G1507SRGER	NULL
MSPM0G3107SRHBR	NULL
MSPM0G1507SPMR	NULL
MSPM0G3507SRGZR	NULL
MSPM0G1106TRGZR	NULL
MSPM0G3507SPTR	NULL
MSPM0G3507SDGS28R	NULL
MSPM0G3105SDGS28R	NULL
MSPM0G1107TPTR	NULL
MSPM0G1507SRHBR	NULL
MSPM0G1106TRHBR	NULL
MSPM0G3507SRHBR	NULL
MSPM0G3506SDGS28R	NULL
MSPM0G3505SDGS28R	NULL
MSPM0G1507SRGZR	NULL
MSPM0G3106SRHBR	NULL
MSPM0G1506SRGZR	NULL
MSPM0G1505SPMR	NULL
MSPM0G1506SRHBR	NULL
MSPM0G3506SPTR	NULL
MSPM0G3505SPMR	NULL
MSPM0G3506SRGZR	NULL
MSPM0G1107TRHBR	NULL
MSPM0G1505SDGS28R	NULL
MSPM0G1506SDGS28R	NULL
MSPM0G3107SDGS28R	NULL
MSPM0G1505SPTR	NULL
MSPM0G3505SPTR	NULL
MSPM0G1107TRGZR	NULL
MSPM0G1507SDGS28R	NULL
MSPM0G3106SDGS28R	NULL
MSPM0G3506SRHBR	NULL
MSPM0G1105TPTR	NULL
MSPM0G3505SRGZR	NULL
MSPM0G1505SRGZR	NULL
MSPM0G1106TPMR	NULL
MSPM0G3105SRHBR	NULL
MSPM0G1106TPTR	NULL
MSPM0G1505SRGER	NULL
MSPM0G1505SRHBR	NULL
MSPM0G3506SPMR	NULL
MSPM0G1506SPTR	NULL
MSPM0G3505SRHBR	NULL
MSPM0G3106SDGS20R	NULL

MSPM0G3105SDGS20R	NULL
MSPM0G1105TRGZR	NULL
MSPM0G1506SPMR	NULL
MSPM0G1506SRGER	NULL
MSPM0G1107TPMR	NULL
MSPM0G1107TRGER	NULL
MSPM0G3107SDGS20R	NULL

Technical details of this Product Change follow on the next page(s).

PCN Number:	20251015003.0	PCN Date:	October 23, 2025
Title:	Datasheet for MSPM0G310x, MSPM0G150x, MSPM0G110x, MSPM0G350x, MSPM0G310x-Q1, MSPM0G350x-Q1		
Customer Contact:	Change Management team	Dept:	Quality Services
Change Type:	Electrical Specification		

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

Changes from October 1, 2023 to October 30, 2025 (from Revision C (October 2023) to Revision D (October 2025)) **Page**

- Added pitch and package identifier details to package options list..... 1
- Added comlementary output to the advanced timer feature description..... 1
- Added WWDT acronym to the windowed watch dog timer feature description..... 1
- Changed communications feature section formatting for clarity..... 1
- Added "open drain" to 5V IO description..... 1
- Added number of high speed IOs to Flexible I/O Features section..... 1
- Updated Optimized Low-Power Mode section..... 1
- Removed functional safety branding from industrial variant datasheet..... 1
- Added "R" to OPNs to designate distribution format..... 6
- Moved Digital Features by IO Type table to beginning of Pin Attributes section..... 9

- Added pin type information to the beginning of the Signal Description section....12
- Added footnote to absolute maximum ratings section for diode current injection limitation on PA21 GPIO pin....20
- Added I_VDD/I_VSS missing footnote to absolute maximum ratings for lower current at VDD=1.62V....20
- Updated LFOSC start-up time specification from 1.7ms to 1ms....20
- Updated Digital IO VOL specification for HSIO to correctly reference temperature condition to match with other IO types for this spec....20
- Updated Digital IO Electrical specifications and Switching specifications sections with added footnote for series current limiting resistor when using HDIO in DRV=1 drive strength setting....20
- Added Digital IO switching specifications line item for port output frequency for HDIO operation with DRV=1 drive strength setting....20
- Added condition for comparator electrical specifications section on I_comp specification HCYCLE register setting....20
- Updated power-on reset voltage level specifications....23
- Updated BOR COLD specification section....23
- Changed the VBOR0- falling from 1.56 to 1.55....23
- Added SLEEP0 wakeup time....25
- Changed "fSYSOSC additional undershoot accuracy during tsettle" min from -11 to -16....26
- Changed SYSPLLCLK0/1from 1MHz to 2.5MHz....27
- Changed SYSPLL RMS cycle-to-cycle jitter from 24ps to 60ps....27
- Changed the SYSPLL typical start up time from 14us to 7us, and the maximum start up time from 24us to 18us....27
- Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz....32
- 32Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz....32
- Changed I_VBST from 0.7uA to 0.8uA....32
- Added "f_in = 10KHz" test condition....32
- Changed V_SupplyMon max from 1% to 1.5%....32
- Changed offset error from +/-2mV to +/-3.5mV....34
- Changed gain error from +/-3LSB to +/-4LSB....34
- Changed temperature sensor settling time from 10us to 12.5us....35
- Removed +/- from output load current and only made it +4mA....36
- Added temperature senor and VREF to Operating Conditions table....42
- Updated table with accurate details....42
- Changed the temperature sensor calibration condition from 1.4V to 3.3V with the correct register configuration setting....52
- Updated the description of the timer features....56
- Updated the *Superset Input/Output Diagram* figure....58
- Added PART and VARIANT to USERID table for YCJ packages....60

Changes from March 1, 2025 to October 3, 2025 (from Revision D (March 2025) to Revision E (October 2025)) **Page**

- Added comlementary output to the advanced timer feature description....1
- Added WWDT acronym to the windowed watch dog timer feature description....1
- Added pitch and package identifier details to package options list....1
- Changed communications feature section formatting for clarity....1
- Added "open drain" to 5V IO description....1
- Added "GPAMP" to list of analog peripherals with internal connections....1
- Added number of high speed IOs to Flexible I/O Features section....1
- Updated Optimized Low-Power Mode section....1
- Removed functional safety branding from industrial variant datasheet....1
- Updated device comparison information for YCJ packages....6

- Changed VSSOP width from 3mm to 4.9mm to account for leads....6
- Added package pitch information....6
- Removed wildcard from part number....6
- Updated comparison table values....6
- Added "R" to OPNs to designate distribution format....6
- Added DSBGA package pin attributes....13
- Moved Digital Features by IO Type to beginning of Pin Attributes section....13
- Added WCSP package signal descriptions....17
- Added pin type information to the beginning of the Signal Description section....17
- Added footnote to absolute maximum ratings section for diode current injection limitation on PA21 GPIO pin....30
- Added I_VDD/I_VSS missing footnote to absolute maximum ratings for lower current at VDD=1.62V....30
- Updated LFOSC start-up time specification from 1.7ms to 1ms....30
- Updated Digital IO VOL specification for HSIO to correctly reference temperature condition to match with other IO types for this spec....30
- Updated Digital IO Electrical specifications and Switching specifications sections with added footnote for series current limiting resistor when using HDIO in DRV=1 drive strength setting....30
- Added Digital IO switching specifications line item for port output frequency for HDIO operation with DRV=1 drive strength setting....30
- Added condition for comparator electrical specifications section on I_comp specification HCYCLE register setting....30
- Updated power-on reset voltage level specifications....34
- Updated BOR COLD specification section....34
- Changed the VBOR0- falling from 1.56 to 1.55....34
- Added SLEEP0 wakeup time....36
- Changed "fSYSOSC additional undershoot accuracy during tsettle" min from -11 to -16....37
- Changed SYSPLLCLK0/1from 1MHz to 2.5MHz....38
- Changed SYSPLLCLK0/1from 1MHz to 2.5MHz....38
- Changed SYSPLL RMS cycle-to-cycle jitter from 24ps to 60ps....38
- Changed period jitter from 15.5ps to 45ps....38
- Changed the SYSPLL typical start up time from 14us to 7us, and the maximum start up time from 24us to 18us....38
- Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz....43
- 32Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz....43
- Changed I_VBST from 0.7uA to 0.8uA....43
- Changed ADC operating current from 1.5mA to 1.75mA....43
- Added "f_in = 10KHz" test condition....43
- Changed V_SupplyMon max from 1% to 1.5%....43
- Changed offset error from +/-2mV to +/-3.5mV....45
- Changed gain error from +/-3LSB to +/-4LSB....45
- Changed temperature sensor settling time from 10us to 12.5us....46
- Added COMP + VREF current consumption in low power mode....47
- Changed COMP low power mode current consumption from 0.84uA to 0.85uA....47
- Changed COMP IDD from 102uA to 120uA....47
- Split parameter section of comparator current consumption section....47
- Changed COMP+VREF low power mode IDD spec from 2.5uA to 3.5uA....47
- Added DAC code test condition....47
- Changed DAC IDD from 300uA to 400uA....47
- Added V_o = 0.3V to VDD-0.3V test condition....48
- Removed +/- from output load current and only made it +4mA....49
- Changed non- inverting gain error (Gain=32) from (-2.6% to +2.6%) to (-3.2% to +2%)....52
- Changed inverting gain error (Gain=-31) from (-2.7% to +2.7%) to (-3.3% to +2.1%)....52

Changes from October 1, 2023 to October 30, 2025 (from Revision C (October 2023) to Revision D (October 2025)) **Page**

- Added pitch and package identifier details to package options list.... 1
- Added comlementary output to the advanced timer feature description.... 1
- Added WWDT acronym to the windowed watch dog timer feature description.... 1
- Changed communications feature section formatting for clarity.... 1
- Added "open drain" to 5V IO description.... 1
- Added number of high speed IOs to Flexible I/O Features section.... 1
- Updated Optimized Low-Power Mode section.... 1
- Removed functional safety branding from industrial variant datasheet.... 1
- Updated Device Comparison table to include YCJ package.... 6
- Added "R" to OPNs to designate distribution format.... 6

- Added WCSP pin out drawings.... 7
- Added DSBGA package pin attributes.... 13
- Moved Digital Features by IO Type to beginning of Pin Attributes section.... 13
- Added WCSP package signal descriptions.... 17
- Added pin type information to the beginning of the Signal Description section.... 17
- Added footnote to absolute maximum ratings section for diode current injection limitation on PA21 GPIO pin.... 29
- Added I_VDD/I_VSS missing footnote to absolute maximum ratings for lower current at VDD=1.62V.... 29
- Updated LFOSC start-up time specification from 1.7ms to 1ms 29
- Updated Digital IO VOL specification for HSIO to correctly reference temperature condition to match with other IO types for this spec.... 29
- Updated Digital IO Electrical specifications and Switching specifications sections with added footnote for series current limiting resistor when using HDIO in DRV=1 drive strength setting.... 29
- Added Digital IO switching specifications line item for port output frequency for HDIO operation with DRV=1 drive strength setting.... 29
- Added condition for comparator electrical specifications section on I_comp specification HCYCLE register setting.... 29
- Updated power-on reset voltage level specifications.... 33
- Updated BOR COLD specification section.... 33
- Changed the VBOR0- falling from 1.56 to 1.55.... 33
- Added SLEEP0 wakeup time.... 35
- Changed "fSYSOSC additional undershoot accuracy during tsettle" min from -11 to -16.... 36
- Changed SYSPLLCLK0/1from 1MHz to 2.5MHz.... 37
- Changed SYSPLL RMS cycle-to-cycle jitter from 24ps to 60ps.... 37
- Changed the SYSPLL typical start up time from 14us to 7us, and the maximum start up time from 24us to 18us.... 37
- Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz.... 42
- 32Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz.... 42
- Changed I_VBST from 0.7uA to 0.8uA.... 42
- Added "f_in = 10KHz" test condition.... 42
- Changed V_SupplyMon max from 1% to 1.5%.... 42
- Changed offset error from +/-2mV to +/-3.5mV.... 44
- Changed gain error from +/-3LSB to +/-4LSB.... 44
- Changed temperature sensor settling time from 10us to 12.5us.... 45
- Removed +/- from output load current and only made it +4mA.... 46
- Added temperature sensor and VREF to Operating Conditions table.... 51
- Changed the temperature sensor calibration condition from 1.4V to 3.3V with the correct register configuration setting.... 60
- Added block diagram of VREF module.... 60
- Updated the description of the timer features.... 63
- Updated the *Superset Input/Output Diagram* figure.... 65
- Added PART and VARIANT to USERID table for YCJ packages.... 67
- Added YCJ package.... 74

Changes from October 1, 2023 to October 3, 2025 (from Revision B (October 2023) to Revision C (October 2025)) **Page**

- Added package pitch information 6
- Removed wildcard from part number 6
- Updated comparison table values 6
- Added "R" to OPNs to designate distribution format 6
- Moved Digital Features by IO Type table to beginning of Pin Attributes section 11
- Added pin type information to the beginning of the Signal Description section 14
- Added footnote to absolute maximum ratings section for diode current injection limitation on PA21 GPIO pin 25
- Added I_VDD/I_VSS missing footnote to absolute maximum ratings for lower current at VDD=1.62V 25
- Updated LFOSC start-up time specification from 1.7ms to 1ms 25
- Updated Digital IO VOL specification for HSIO to correctly reference temperature condition to match with other IO types for this spec 25
- Updated Digital IO Electrical specifications and Switching specifications sections with added footnote for series current limiting resistor when using HDIO in DRV=1 drive strength setting 25
- Added Digital IO switching specifications line item for port output frequency for HDIO operation with DRV=1 drive strength setting 25
- Added condition for comparator electrical specifications section on I_comp specification HCYCLE register setting 25
- Updated power-on reset voltage level specifications 29
- Updated BOR COLD specification section 29
- Changed the VBOR0- falling from 1.56 to 1.55 29
- Added SLEEP0 wakeup time 32
- Changed "fSYSOSC additional undershoot accuracy during tsettle" min from -11 to -16 33
- Changed SYSPLLCLK0/1from 1MHz to 2.5MHz 36
- Changed SYSPLL RMS cycle-to-cycle jitter from 24ps to 60ps 36
- Changed the SYSPLL typical start up time from 14us to 7us, and the maximum start up time from 24us to 18us 36
- Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz 43
- 32Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz 43
- Changed I_VBST from 0.7uA to 0.8uA 43
- Added "f_in = 10KHz" test condition 43
- Changed V_SupplyMon max from 1% to 1.5% 43
- Changed offset error from +/-2mV to +/-3.5mV 45
- Changed gain error from +/-3LSB to +/-4LSB 45
- Changed temperature sensor settling time from 10us to 12.5us 46
- Added COMP + VREF current consumption in low power mode 47
- Changed COMP low power mode current consumption from 0.84uA to 0.85uA 47
- Changed COMP IDD from 102uA to 120uA 47
- Split parameter section of comparator current consumption section 47
- Changed COMP+VREF low power mode IDD spec from 2.5uA to 3.5uA 47
- Added DAC code test condition 48
- Changed DAC IDD from 300uA to 400uA 48
- Added V_o = 0.3V to VDD-0.3V test condition 49
- Removed +/- from output load current and only made it +4mA 50
- Changed non- inverting gain error (Gain=32) from (-2.6% to +2.6%) to (-3.2% to +2%) 53
- Changed inverting gain error (Gain=-31) from (-2.7% to +2.7%) to (-3.3% to +2.1%) 53
- Updated table with accurate details 60
- Changed the temperature sensor calibration condition from 1.4V to 3.3V with the correct register configuration setting 70
- Updated the description of the timer features 77
- Updated the *Device Analog Connection* figure 79
- Updated the *Superset Input/Output Diagram* figure 81
- Updated the description of the device nomenclature 85

Changes from May 31, 2024 to September 30, 2025 (from Revision (May 2024) to Revision (September 2025)) **Page**

- Added pitch and package identifier details to package options list.... 1
- Added comlementary output to the advanced timer feature description.... 1
- Added WWDT acronym to the windowed watch dog timer feature description.... 1
- Changed communications feature section formatting for clarity.... 1
- Added "open drain" to 5V IO description.... 1
- Added number of high speed IOs to Flexible I/O Features section.... 1
- Updated Optimized Low-Power Mode section.... 1
- Updated functional safety branding to indicate ASIL B compliance.... 1
- Updated Features page to match supply current characteristics electrical specifications 1
- Added "R" to OPNs to designate distribution format.... 6

- Moved Digital Features by IO Type table to beginning of Pin Attributes section.... 12
- Added pin type information to the beginning of the Signal Description section.... 15
- Added footnote to absolute maximum ratings section for diode current injection limitation on PA21 GPIO pin.... 25
- Added I_VDD/I_VSS missing footnote to absolute maximum ratings for lower current at VDD=1.62V.... 25
- Updated LFOSC start-up time specification from 1.7ms to 1ms 25
- Updated Digital IO VOL specification for HSIO to correctly reference temperature condition to match with other IO types for this spec.... 25
- Updated Digital IO Electrical specifications and Switching specifications sections with added footnote for series current limiting resistor when using HDIO in DRV=1 drive strength setting.... 25
- Added Digital IO switching specifications line item for port output frequency for HDIO operation with DRV=1 drive strength setting.... 25
- Added condition for comparator electrical specifications section on I_comp specification HCYCLE register setting.... 25
- Updated power-on reset voltage level specifications.... 29
- Updated BOR COLD specification section.... 29
- Changed the VBOR0- falling from 1.56 to 1.55.... 29
- Added SLEEP0 wakeup time.... 31
- Changed "fSYSOSC additional undershoot accuracy during tsettle" min from -11 to -16.... 32
- Changed SYSPLLCLK0/1from 1MHz to 2.5MHz.... 33
- Changed SYSPLL RMS cycle-to-cycle jitter from 24ps to 60ps.... 33
- Changed the SYSPLL typical start up time from 14us to 7us, and the maximum start up time from 24us to 18us.... 33
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- Changed gain error from +/-3LSB to +/-4LSB.... 40
- Changed temperature sensor settling time from 10us to 12.5us.... 41
- Removed +/- from output load current and only made it +4mA.... 42
- Added temperature senor and VREF to Operating Conditions table.... 48
- Updated table with accurate details.... 48
- Changed the temperature sensor calibration condition from 1.4V to 3.3V with the correct register configuration setting.... 58
- Added PART and VARIANT to USERID table for YCJ packages.... 66

Changes from May 31, 2024 to September 30, 2025 (from Revision (May 2024) to Revision (September 2025)) **Page**

- Added comlementary output to the advanced timer feature description..... 1
- Added WWDT acronym to the windowed watch dog timer feature description..... 1
- Added pitch and package identifier details to package options list..... 1
- Changed communications feature section formatting for clarity..... 1
- Added "open drain" to 5V IO description..... 1
- Added "GPAMP" to list of analog peripherals with internal connections..... 1
- Added number of high speed IOs to Flexible I/O Features section..... 1

- Updated Optimized Low-Power Mode section.....1
- Updated functional safety branding to indicate ASIL B compliance.....1
- Updated Features page to match supply current characteristics electrical specifications 1
- Changed VSSOP width from 3mm to 4.9mm to account for leads.....7
- Added package pitch information.....7
- Removed wildcard from part number.....7
- Updated comparison table values.....7
- Added "R" to OPNs to designate distribution format.....7
- Moved Digital Features by IO Type table to beginning of Pin Attributes section.....13
- Added pin type information to the beginning of the Signal Description section.....16
- Added footnote to absolute maximum ratings section for diode current injection limitation on PA21 GPIO pin.....27
- Added I_VDD/I_VSS missing footnote to absolute maximum ratings for lower current at VDD=1.62V.....27
- Updated LFOSC start-up time specification from 1.7ms to 1ms 27
- Updated Digital IO VOL specification for HSIO to correctly reference temperature condition to match with other IO types for this spec.....27
- Updated Digital IO Electrical specifications and Switching specifications sections with added footnote for series current limiting resistor when using HDIO in DRV=1 drive strength setting.....27
- Added Digital IO switching specifications line item for port output frequency for HDIO operation with DRV=1 drive strength setting.....27
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- Updated BOR COLD specification section.....31
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- Changed SYSPLL RMS cycle-to-cycle jitter from 24ps to 60ps.....35
- Changed the SYSPLL typical start up time from 14us to 7us, and the maximum start up time from 24us to 18us.....35
- Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz.....40
- 32Changed VDD ≥ 2.7V, DRV = 1, CL= 20pF specification from 40MHz to 32MHz.....40
- Changed I_VBST from 0.7uA to 0.8uA.....40
- Added "f_in = 10KHz" test condition.....40
- Changed V_SupplyMon max from 1% to 1.5%.....40
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- Added COMP + VREF current consumption in low power mode.....44
- Changed COMP low power mode current consumption from 0.84uA to 0.85uA.....44
- Changed COMP IDD from 102uA to 120uA.....44
- Split parameter section of comparator current consumption section.....44
- Changed COMP+VREF low power mode IDD spec from 2.5uA to 3.5uA.....44
- Added DAC code test condition.....44
- Changed DAC IDD from 300uA to 400uA.....44
- Added V_o = 0.3V to VDD-0.3V test condition.....45
- Removed +/- from output load current and only made it +4mA.....46
- Changed non- inverting gain error (Gain=32) from (-2.6% to +2.6%) to (-3.2% to +2%).....49
- Changed inverting gain error (Gain=-31) from (-2.7% to +2.7%) to (-3.3% to +2.1%).....49
- Updated table with accurate details.....54
- Changed the temperature sensor calibration condition from 1.4V to 3.3V with the correct register configuration setting.....64

The datasheet number will be changing.

Device Family	Change From:	Change To:
MSPM0G310x	SLASF12C	**SLASF12D**

MSPM0G150x	SLASEW9D	**SLASEW9E**
MSPM0G110x	SLASF11C	**SLASF11D**
MSPM0G350x	SLASEX6B	**SLASEX6C**
MSPM0G310x-Q1	SLASF86B	**SLASF86C**
MSPM0G350x-Q1	SLASF88B	**SLASF88C**

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/MSPM0G3107

http://www.ti.com/product/MSPM0G1507

http://www.ti.com/product/MSPM0G1107

http://www.ti.com/product/MSPM0G3507

http://www.ti.com/product/MSPM0G3107-Q1

http://www.ti.com/product/MSPM0G3507-Q1

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact.

Changes to product identification resulting from this PCN:

None.

Product Affected:

MSPM0G1105TPTR	MSPM0G1505SPTR.A	MSPM0G1507SRGZR	MSPM0G3505SRGZR
MSPM0G1105TPTR.A	MSPM0G1505SPTR.B	MSPM0G1507SRGZR.A	MSPM0G3505SRGZR.A

MSPM0G1105TPTR.B	MSPM0G1505SRGER	MSPM0G1507SRGZR.B	MSPM0G3505SRGZR.B
MSPM0G1105TRGZR	MSPM0G1505SRGER.A	MSPM0G1507SRHBR	MSPM0G3505SRHBR
MSPM0G1105TRGZR.A	MSPM0G1505SRGER.B	MSPM0G1507SRHBR.A	MSPM0G3505SRHBR.A
MSPM0G1105TRGZR.B	MSPM0G1505SRGZR	MSPM0G1507SRHBR.B	MSPM0G3505SRHBR.B
MSPM0G1106TPMR	MSPM0G1505SRGZR.A	MSPM0G3105SDGS20R	MSPM0G3506SDGS28R
MSPM0G1106TPMR.A	MSPM0G1505SRGZR.B	MSPM0G3105SDGS20R.A	MSPM0G3506SDGS28R.A
MSPM0G1106TPMR.B	MSPM0G1505SRHBR	MSPM0G3105SDGS20R.B	MSPM0G3506SDGS28R.B
MSPM0G1106TPTR	MSPM0G1505SRHBR.A	MSPM0G3105SDGS28R	MSPM0G3506SPMR
MSPM0G1106TPTR.A	MSPM0G1505SRHBR.B	MSPM0G3105SDGS28R.A	MSPM0G3506SPMR.A
MSPM0G1106TPTR.B	MSPM0G1506SDGS28R	MSPM0G3105SDGS28R.B	MSPM0G3506SPMR.B
MSPM0G1106TRGZR	MSPM0G1506SDGS28R.A	MSPM0G3105SRHBR	MSPM0G3506SPTR
MSPM0G1106TRGZR.A	MSPM0G1506SDGS28R.B	MSPM0G3105SRHBR.A	MSPM0G3506SPTR.A
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MSPM0G1107TPMR	MSPM0G1506SRGER.A	MSPM0G3106SRHBR	MSPM0G3507SDGS28R
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MSPM0G1107TPTR	MSPM0G1506SRGZR.A	MSPM0G3107SDGS20R	MSPM0G3507SPMR
MSPM0G1107TPTR.A	MSPM0G1506SRGZR.B	MSPM0G3107SDGS20R.A	MSPM0G3507SPMR.A
MSPM0G1107TPTR.B	MSPM0G1506SRHBR	MSPM0G3107SDGS20R.B	MSPM0G3507SPMR.B
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A			
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ZVEI ID: SEM-DS-01

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.