12500 TI Boulevard, MS 8640, Dallas, Texas 75243

Notification# 20240923001.0
Datasheet for DS90UH988-Q1, DS90UB984-Q1, DS90UB988-Q1, and DS90UH984-Q1
Information Only

Date: September 25, 2024
To: MOUSER PCN

Dear Customer:

This is an information-only announcement of a change to a device that is currently offered by Texas Instruments.

The changes discussed within this notification are for your information only.

Any negotiated alternative change requirements will be provided via the customer's defined process. Customers with previously negotiated, special requirements will be handled separately. Any inquiries should be directed to your local Field Sales Representative.

For questions regarding this notice, contact your local Field Sales Representative or the Change Management team.

Sincerely,

Change Management Team
SC Business Services

20240923001.0
Information Only Datasheet
Attachments

Products Affected:

The devices listed on this page are a subset of the complete list of affected devices. According to our records**,** you have recently purchased these devices**.** The corresponding customer part number is also listed, if available.

DEVICE	CUSTOMER PART NUMBER
DS90UB984RURTQ1	NULL
DS90UH984RURTQ1	NULL
DS90UH988RURTQ1	NULL

Technical details of this Product Change follow on the next page(s).

PCN Number:	20240923001.0	PCN Date:	September 25, 2024
Title:	Datasheet for DS90UH988-Q1, DS90UB984-Q1, DS90UB988-Q1, and DS90UH984-Q1		
Customer Contact:	Change Management team	Dept:	Quality Services
Change Type:	Electrical Specification		

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

DS90UH988-Q1

SNLS649A – FEBRUARY 2022 – REVISED NOVEMBER 2023

Changes from Revision * (February 2022) to Revision A (November 2023) **Page**

- Updated RIN and DOUT differential and single-ended configuration description in pin function table.... 4
- Updated value of the internal pull-down resistor for the PDB pin.... 4
- Added information about configuring the INTB_IN pin.... 4
- Updated FPD-Link III data path in functional block diagram.... 46
- Updated ispread value for OLDI SSCG.... 57
- Added clarification that single link mode uses RX port 0 only.... 60
- Added port clarification for single link mode.... 60
- Post divider value correction FPD-Link IV RX PLL table.... 60
- Moved Display Timing Generator section.... 61
- Added programming the DTG for FPD-Link III Daisy-Chain section.... 62
- Updated back-channel SSCG script.... 63
- Added temperature ramp section and script.... 67
- Added FPD port polarity swap.... 68
- Updated CF Values for pins VDD11_TX1 and VDD11_D.... 69
- Clarified INTB_IN step 6 set-up sequence.... 71
- Added GPIO configuration guidance to reduce spurious GPIO noise.... 76
- Added FC GPIO configuration instructions.... 76
- Updated Back-Channel GPIO configuration table.... 77
- Added daisy-chain GPIO example script.... 77
- Added DS90Ux944A and DS90Ux688 to backward compatibility table.... 79
- Added 98x in FPD-Link III mode to backward compatibility table.... 79
- Added additional usage guidance for DIGITAL_RESET_ALL while in FPD-Link III RX mode.... 81
- Removed TX_BIST_CTL_FPD3 (0x14) from Main-Link BIST instructions.... 83
- Updated the information on enabling BIST mode from the serializer or the deserializer.... 83
- Integrated into serializer or deserializer 89
- Added RGB_CHKSUM_EN requirement for FPD-Link III mode.... 90
- Added DS90Ux949 supports audio over HDMI or I2S pins.... 93
- Added supported daisy-chain rates of 10.8Gbps, 12.528Gbps, and 13.5Gbps.... 103
- Added DUAL_ALIGN_DE bit to 1 when operating in dual FPD-Link daisy chain mode.... 104
- Added FPD-Link III daisy-chain SSCG frequency deviation guidance.... 105
- Updated CMLOUT script.... 110
- Updated FPD-Link III AEQ default wait time.... 112
- Corrected Fmod under MODE_SEL2 table 113
- Added dual and single FPD-Link RX dependency on Target 1 address.... 115
- Moved I2C access over the main link back channel information to Remote Target Operation section.... 117

Changes from Revision * (December 2022) to Revision A (November 2023) **Page**

- Unreserved registers/bits: main page 0x3B[3:1], main page 0x3D, main page 0x3E, Page_5 0x18, Page_5 0x19, Page_6 0x44[1], Page_8 0x8D, Page_10 0x40[3], Page_10 0xC0[3], Page_18 0xC1, Page_18 0xC2, Page_18 0xC7[1:0], Page_20 0x80-0xEF, APB 0x128[0]..... 126
- Reserved registers/bits: main page 0x54[1], Page_17 0x80[7], Page_17 0x88[7], Page_17 0x90[7], Page_17 0x98[7], Page_17 0xA0[7], Page_17 0xA8[7], Page_17 0xB0[7], Page_17 0xB8[7], Page_17 0xC0[7], Page_17 0xC8[7], Page_17 0xD0[7], Page_17 0xD8[7]..... 126
- Modified eDP AUX voltage, I2C pin names in Coax and STP Typical Applications Diagrams 533
- Added information about strap voltage stable before PDB high..... 538
- Modified t0 PDB Start Threshold in Power Sequencing..... 538

Changes from Revision * (December 2022) to Revision A (November 2023) **Page**

- Updated value of the internal pull-down resistor for the PDB pin..... 4
- Added information about configuring the INTB_IN pin..... 4
- Updated FPD-Link III data path in functional block diagram..... 46
- Updated ispread value for OLDI SSCG..... 57
- Added port clarification for single link mode..... 60
- Moved Display Timing Generator section..... 61
- Added programming the DTG for FPD-Link III Daisy-Chain section..... 62
- Updated CF Values for pins VDD11_TX1 and VDD11_D..... 69
- Added GPIO configuration guidance to reduce spurious GPIO noise..... 76
- Added DS90Ux944A and DS90Ux688 to backward compatibility table..... 79
- Updated the information on enabling BIST mode from the serializer or the deserializer..... 83
- Added RGB_CHKSUM_EN requirement for FPD-Link III mode..... 90
- Added checksum error in the FPD-Link III video stream errors script..... 90
- Moved I2C access over the main link back channel information to Remote Target Operation section..... 117
- Added configuration information on daisy-chain I2C transactions when main link is unlocked..... 117
- Modified registers/bits: main page 0x05[7:6], main page 0x2B, main page 0x2C, main page 0x2F, main page 0x30, main page 0x3B[0], main page 0x3C, main page 0x3F, main page 0x40, main page 0x45[0], main page 0x79-0x7F, main page 0x92[1:0], main page 0xA3, Page_2 0x07[0], Page_3 0x07[0], Page_5 0x1E[7], Page_7 0x5-0xE, Page_7 0x25-0x2E, Page_11 0x02[6:5], Page_11 0x21[3:2], Page_11 0x23[3:2], Page_18 0xC7[2], Page_20 0x32[0], Page_20 0x62[0]..... 126
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- Reserved registers/bits: main page 0x2F[6], main page 0x54[1], Page_17 0x80[7], Page_17 0x88[7], Page_17 0x90[7], Page_17 0x98[7], Page_17 0xA0[7], Page_17 0xA8[7], Page_17 0xB0[7], Page_17 0xB8[7], Page_17 0xC0[7], Page_17 0xC8[7], Page_17 0xD0[7], Page_17 0xD8[7]..... 126
- Modified to match pin names in OLDI and RGB Typical Applications Diagrams 471
- Changed the unit for t3 from ms to us..... 478
- Updated Power Up Requirements And PDB Pin description..... 478
- Modified t0 PDB Start Threshold in Power Sequencing..... 478

Changes from Revision A (December 2022) to Revision B (November 2023) **Page**

- Updated value of the internal pull-down resistor for the PDB pin....3
- Added information about configuring the INTB_IN pin....3
- Modified APB_CTL placement in the APB Read/Write Script....45
- Updated 3.3V AUX connection for eDP/DP....48
- Added port clarification for single link mode....56
- Moved Display Timing Generator section....58
- Added programming the DTG for FPD-Link III Daisy-Chain section....59
- Updated CF Values for pins VDD11_TX1 and VDD11_D....66
- Added GPIO configuration guidance to reduce spurious GPIO noise....73
- Added DS90Ux944A and DS90Ux688 to backward compatibility table....76
- Updated the information on enabling BIST mode from the serializer or the deserializer....80
- Added RGB_CHKSUM_EN requirement for FPD-Link III mode....87
- Moved I2C access over the main link back channel information to Remote Target Operation section....117
- Added configuration information on daisy-chain I2C transactions when main link is unlocked....117
- Modified registers/bits: main page 0x05[7:6], main page 0x2B, main page 0x2C, main page 0x2F, main page 0x30, main page 0x3B[0], main page 0x3C, main page 0x3F, main page 0x40, main page 0x45[0], main page 0x79-0x7F, main page 0x92[1:0], Page_2 0x07[0], Page_3 0x07[0], Page_5 0x1E[7], Page_6 0x44[1], Page_7 0x5-0xE, Page_7 0x25-0x2E, Page_12 0x07[0], Page_20 0x32[0], Page_20 0x62[0], Page_20 0x92[0], Page_20 0xD2[0]....126
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- Modified eDP AUX voltage, I2C pin names in Coax and STP Typical Applications Diagrams....536
- Added Power Supply Recommendations description....540
- Added information about strap voltage stable before PDB high....541
- Modified t0 PDB Start Threshold in Power Sequencing....541

The datasheet number will be changing.

Device Family	Change From:	Change To:
DS90UH988-Q1	SNLS649	**SNLS649A**
DS90UB984-Q1	SNLS607	**SNLS607A**
DS90UB988-Q1	SNLS706	**SNLS706A**
DS90UH984-Q1	SNLS609A	**SNLS609B**

The document is not available on the TI website. Please contact the document owner at k-hawkins@ti.com or visit the MySecure site for a copy of the full datasheet.

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

DS90UH988RURTQ1	DS90UH988RURRQ1	DS90UB984RURTQ1	DS90UB984RURRQ1
DS90UB988RURTQ1	DS90UB988RURRQ1	DS90UH984RURTQ1	DS90UH984RURRQ1

For questions regarding this notice, e-mails can be sent to the Change Management team or your local Field Sales Representative.

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