PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	MDG/24/14455
1.3 Title of PCN	STM32G050x, STM32G051x and STM32G061x 64K - product enhancement - addendum to PCN13483
1.4 Product Category	STM32G050x, STM32G051x, STM32G061x
1.5 Issue date	2024-02-09

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Ricardo Antonio DE SA EARP
2.1.2 Marketing Manager	Veronique BARLATIER
2.1.3 Quality Manager	Pascal NARCHE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Die redesign : Mask or mask set change with new die design like metallization (specifically chip frontside) or bug fix	TSMC FAB14 (Taiwan) ST Crolles (France)

4. Description of change		
	Old	New
4.1 Description	STM32G050x, STM32G051x and STM32G061x 64K - (Die456– cut1.0 revision A) product has limitation as described in Errata Sheets. - ES0544 (Rev 1 - December 16 2020) for STM32G050x6/x8 device - ES0545 (Rev 1 - December 16 2020) for STM32G051x6/x8 device - ES0546 (Rev 1 - December 16 2020) for STM32G061x6/x8 device	STM32G050x, STM32G051x and STM32G061x 64K - (Die456 – cut1.1 revision Z) product enhancement fixes those limitations as described in Errata Sheets. - ES0544 (Rev 2 - April 12 2022) for STM32G050x6/x8 device - ES0545 (Rev 2 - April 12 2022) for STM32G051x6/x8 device - ES0546 (Rev 2 - April 12 2022) for STM32G061x6/x8 device
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	Impact on functionality as indicated in Errata Sheets: ES0544, ES0545 & ES0546	

5. Reason / motivation for change	
5.1 Motivation	Improvements was implemented to increase robustness, performances and quality of our products. PCN13483 sent initially was not received by new customers and REV A will be terminated in April 2024
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Traceability ensured by ST internal tools. Die revision changes from "A" to "Z" on Package Marking

7. Timing / schedule	
7.1 Date of qualification results	2022-11-24
7.2 Intended start of delivery	2022-12-08
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	14455 MDG-MCD-RER2012 V1.5 - STM32G0 - Die 456XXXZ- Reliability evaluation report.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	**Issue Date**	2024-02-09

9. Attachments (additional documentations)
14455 Public product.pdf 14455 MDG-MCD-RER2012 V1.5 - STM32G0 - Die 456XXXZ- Reliability evaluation report.pdf 14455 PCN14455_Additional information.pdf

10. Affected parts		
10. 1 Current		**10.2 New (if applicable)**
10.1.1 Customer Part No	**10.1.2 Supplier Part No**	**10.1.2 Supplier Part No**
	STM32G050C6T6	
	STM32G050C8T6	
	STM32G050F6P6	
	STM32G050K6T6	
	STM32G050K8T6	
	STM32G051C6T6	
	STM32G051C6U6	
	STM32G051C8T3	
	STM32G051C8T6	
	STM32G051C8U6	
	STM32G051F8P6	
	STM32G051F8Y6TR	
	STM32G051G6U6	
	STM32G051G8U3	
	STM32G051G8U6	
	STM32G051K6T6	
	STM32G051K8T6	
	STM32G051K8U6	
	STM32G051K8U7	
	STM32G061C6T6	
	STM32G061C6U6	
	STM32G061C8T6	
	STM32G061C8U6	
	STM32G061F8Y6TR	
	STM32G061G6U6	
	STM32G061G8U6	
	STM32G061K6T6	
	STM32G061K8T6	

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Reliability Evaluation Report

MDG-MCD-RER2012

STM32G0x (456x66)

Reliability Evaluation Purpose **(New Product Qualification)**

General Information	
Commercial Product	STM32G05x/ STM32G06x
Product Line	456X66
Die revision	456XXXZ (Cut1.1)
Product Description	STM32G0x
Package	LQFP7x7 48L, LQFP32 7x7, UFQFPN7x7 48L, UFQFPN5x5 32L, UFQFN 4X4 28L, TSSOP 20, WLCSP20
Silicon Technology	TSMC Fab14 90ULL
Division	MDG-MCD
Reliability Maturity Level	30

Traceability	
Diffusion Plant	TSMC Fab14, Taiwan.
Assembly Plant	ATP1, AMKOR, Philippines. ATT1, AMKOR, Taiwan. JSCC, China.

Reliability Assessment	
Pass	☒
Fail	☐
Investigation required	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	Dec 3th 2020	Muriel GALTIER	MDG-MCD-Q&R Engineer
1.1	Jan 27th 2021	Muriel GALTIER	MDG-MCD-Q&R Engineer
1.2	March 4th 2021	Muriel GALTIER	MDG-MCD-Q&R Engineer
1.3	July 11th 2022	Muriel GALTIER	MDG-GPM-Q&R Engineer
1.4	Nov 21st 2022	Octavia NDJOYE-KOGOU	MDG-GPM-Q&R Engineer
1.5	Jan 25th 2024	Muriel GALTIER Octavia NDJOYE-KOGOU	MDG-GPM-Q&R Engineer

APPROVED BY:

VERSION 1.0

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	04-Dec-2020
Division Quality Manager	Rousset	Pascal NARCHE	04-Dec-2020

VERSION 1.1

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	27-Jan-2021

VERSION 1.2

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	18-Mar-2021

VERSION 1.3

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	11-Jul-2022

VERSION 1.4

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	24-Nov-2022

VERSION 1.5

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	25-Jan-2024

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation performed on STM32G0x - Die 456XXXZ.

Test vehicle is described here below:

Product	Process / Package	Diffusion / Assembly plant
STM32G051C8T6	90ULL, LQFP 7x7 48L	TSMC Fab14, JSCC
STM32G051K8T6	90ULL, LQFP 7x7 32L	TSMC Fab14, JSCC
STM32G051C8U6	90ULL, UFQFPN 7x7 48L	TSMC Fab14, JSCC
STM32G051K8U6	90ULL, UFQFPN 5x5 32L	TSMC Fab14, JSCC
STM32G051G8U6	90ULL, UFQFPN 4x4 28L	TSMC Fab14, JSCC
STM32G051F8P6	90ULL, TSSOP 20	TSMC Fab14, ATP1
STM32G051F8Y6TR	90ULL, WLCSP 20L	TSMC Fab14, ATT1

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

1.2 Reliability Strategy

The STM32G0x - Die 456XXXA, is processed in the 90ULL process from TSMC Fab14 Taiwan plant which is qualified through- Die 415 (RERMCD1112).

Partial Construction Analysis are needed on two packages:

- TSSOP 20 because of new FE node TSMC 90nm in TSSOP line
- UFQFN28 to get data on wire bond profile.

For LQFP32 we can apply similarity rules with LQFP48 so only CDM needed.
For UFQFN48, only CDM needed thanks to:

- Available reliability on same packages with similar die sizes.

For UFQFN32, only CDM needed thanks to available reliability on same packages with similar die sizes.
Package reliability exercise is planned on 1 lot to assess the LQFP7x7 48L.

Package	Reference	Assy Plant location
LQFP 7x7 48L	RERMCD1621	JSCC, China
LQFP 7x7 32L	RERMCD1621	JSCC, China
UFQFPN 7x7 48L	RERMCD1622/RERMCD1808	JSCC, China
UFQFPN 5x5 32L	RERMCD1622/RERMCD1808	JSCC, China
UFQFN 4x4 28L	RERMCD1808	JSCC, China
TSSOP 20	RERMCD1712	ATP1, AMKOR, Philippines

WLCSP 20L	RERMCD1213	ATT1, AMKOR, Taiwan.

According to "RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION" specification (DMS 0061692), the following qualification strategy has been defined:

- Die Qualification:
  - Cut1.0:1 full qualification lot to assess the die in LQFP48 package (valid for all packages)
    Cut1.1: Minor fixes are implemented on this cut. No reliability risk has been identified – Only HTOL (168H), HBM, LU & CDM tests are planned

    The PPM and FIT targets are followed through the MCD monitoring program

Note: ESD HBM & LU is done in LQFP48 (Max pin count)

- Package Qualification:
  The reliability test plan and result summary are presented in the following tables:

Package	Body	Pitch	Package Code	Wire	Assembly	Bonding Option	Trial
LQFP 48	7x7	0.5	5B	Gold	JSCC		1 reliability lot
LQFP 32	5x5	0.5	5V	Gold	JSCC		CDM only
UFQFN 48L	7x7	0.5	A0B9 (MI)	Gold	JSCC		CDM only
UFQFN 32L	5x5	0.5	A0B8 (MG)	Gold	JSCC		CDM only
UFQFN 28L	4x4	0.5	A0B0 (MB)	Gold	JSCC		1 reliability lot + reduced CA
TSSOP 20		0.65	YA	Gold	ATP1		1 reliability lot + reduced CA
WLCSP20	-	0.4	4I (J3)	-	ATT1		1 reliability lot

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, Maturity 30 is granted for the STM32G0x- Die 456 cut 1.1 for LQFP48, WLCSP20, LQFP32, QFN32, QFN48 and TSSOP packages

Refer to Section 3.0 for reliability test results.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

The die 456 - is a derivative from die 466. The main differences are linked add 1x12 bit DAC 2 channels, 2 comparators and 1x16 bit timer 2 (PWM)

For additional information concerning the product behavior, refer to STM32G0x datasheets.

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information	
FAB1	
Wafer fab name / location	TSMC Fab14 / Taiwan
Wafer diameter (inches)	12
Wafer thickness (µm)	775 +/- 25
Silicon process technology	TSMC090 ULL
Number of masks	45
Die finishing front side (passivation) materials/thicknesses (µm)	FSG + NITRIDE 1um
Die area (Stepping die size) (µm)	1966.6, 2421.6
Die pad size (X,Y) (µm)	123, 59
Sawing street width (X,Y) (µm)	80, 80
Metal levels/Materials/Thicknesses (µm)	Rank - Metal composition - Thickness (um) 1 - TaN/Ta/CuSeed/Cu - 0.240 / 2 - TaN/Ta/CuSeed/Cu - 0.310 3 - TaN/Ta/CuSeed/Cu - 0.310 / 4 - TaN/Ta/CuSeed/Cu - 0.310 5 - TaN/Ta/CuSeed/Cu - 0.310 / 6 - TaN/Ta/CuSeed/Cu - 0.850 7 - AlCu - 1.450
Die over coating (material/thickness)	NA
FIT level (Ea=0.7eV, C.L: 60%, 55°C)	2.2 FITs at qualification date
Soft Error Rate - Alpha SER [FIT/Mb] - Neutron SER [FIT/Mb] - Conditions	Alpha SER: 491 FIT/Mb Neutron SER: 445 FIT/Mb Neutron SER is an estimation at sea level of NYC (14n/h/cm²). Alpha result is estimated using a nominal flux of 0.001α/h/cm²
Wafer Level Reliability - Electro-Migration (EM) - Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) - Hot Carrier Injection (HCI) - Negative Bias Thermal Instability (NBTI) - Stress Migration (SM)	Yes
Other Device(s) using same process	STM32L4x, STM32G4x product family, 415, 435, 461, 462, 464, 470, 468, 469, 466, 479

2.2.2 Assembly information

Table 2

Assembly Information	
Package 1 - LQFP 7x7x1.4 48L 5B	
Assembly plant name / location	JSCC, China.
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/- 25
Die sawing method	Laser Groove + Mechanical sawing
Bill of Material elements	
Lead Frame material/supplier	LQFP 48L C9-DSM 184x184 (7x7PKG)/HDS
Die attach material/type(glue/film)/supplier	R008-0005A/Epoxy 3230/Ablestik
Wire bonding material/diameter/supplier	GOLD WIRE /0.8MIL/HERAEUS
Molding compound material/supplier	EME-G631SH/ Sumitomo
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 2 - LQFP 7x7x1.4 32L 5V	
Assembly plant name / location	JSCC, China.
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/- 25
Die sawing method	Laser Groove + Mechanical sawing
Bill of Material elements	
Lead Frame material/supplier	LQFP 32L C9-DSM 184x184 (7x7PKG)/HDS
Die attach material/type(glue/film)/supplier	R008-0005A/Epoxy 3230/Ablestik
Wire bonding material/diameter/supplier	GOLD WIRE /0.8MIL/HERAEUS
Molding compound material/supplier	EME-G631SH/ Sumitomo
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 3 - UFQFPN 7x7x0.5 48L A0B9 (MI)	
Assembly plant name / location	JSCC, China.
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 +/- 10
Die sawing method	Laser Groove + Mechanical sawing
Bill of Material elements	
Lead Frame material	Sn PAD 5.2 MM SQ Groove
Die attach material/type(glue/film)/supplier	EN4900GC /Glue/ Hitachi
Wire bonding material/diameter	GOLD 0.8 MIL
Molding compound material/supplier	RESIN G770/ SUMITOMO
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 4 - UFQFPN 5x5x0.5 32L A0B8 (MG)	
Assembly plant name / location	JSCC, China.

Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 +/- 10
Die sawing method	Laser Groove + Mechanical sawing
Bill of Material elements	
Lead Frame material	Sn PAD 3.1MMSQ GROOVE(4up)
Die attach material/type(glue/film)/supplier	Glue EN4900GC /Hitachi
Wire bonding material/diameter	GOLD 0.8 MIL
Molding compound material/supplier	RESIN G770/ SUMITOMO
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 5 - UFQFN 4x4x0.5 28L A0B0 (MB)	
Assembly plant name / location	JSCC, China.
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 +/- 10
Die sawing method	Laser Groove + Mechanical sawing
Bill of Material elements	
Lead Frame material	QFNs-HD-COL28 4*4
Die attach material/type(glue/film)/supplier	DAF(Film) HR-5104/ HITACHI
Wire bonding material/diameter	GOLD 0.8 MIL
Molding compound material/supplier	Mold COMPOUND EME G770HCD/SUMITOMO
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
Package 6 - TSSOP x0.65 20 YA	
Assembly plant name / location	ATP1, AMKOR, Philippines.
Pitch (mm)	0.65
Die thickness after back-grinding (µm)	275 +/- 25
Die sawing method	Laser Groove + Mechanical sawing
Bill of Material elements	
Lead Frame material /supplier	C194/ HAESUNG DS
Die attach material/type(glue/film)/supplier	ESEC-2100XP /Glue/ HENKEL KOREA LTD
Wire bonding material/diameter/supplier	WIRE GOLD DIAM. 0.8 MIL/ MK ELECTRON
Molding compound material/supplier	TOWA-YPM 1180/ TAKATORI
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Package 7 - WLCSP 20 4I (YA)	
Assembly plant name / location	ATT1, AMKOR, Taiwan.
Pitch (mm)	0.4
Die thickness after back-grinding (µm)	355 +/- 25
Die sawing method	Laser Groove + Mechanical sawing
Bill of Material elements	
PBO material/reference	HD8820
RDL	Copper 6um
UBM	Ti/Cu/Cu
Balls metallurgy/diameter (BGA/CSP)	SAC405/ 230 um
Backside Coating material/supplier/reference	LC2850/ LINTEC
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 1

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	GRAL/Grenoble

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
1	P64U84 Wafer#23	1.0	GQ03428R	705B*456ESXA	LQFP 7x7 48L	Die and Package Reliability assessment.
2	P64U84 Wafer#23	1.0	GQ035208	705V*456ESXA	LQFP 7x7 32L	Package Reliability assessment.
3	P64U84 Wafer#24	1.0	GQ0342BA	70MI*456ESXA	UFQFN 7x7 48L	Package Reliability assessment.
4	P64U84 Wafer#24	1.0	GQ03520A	70MG*456ESXA	UFQFN 5x5 32L	Package Reliability assessment.
5	P64U84 Wafer#25	1.0	GQ03524N	70MB*479ESXA	UFQFN 4x4 28L	Package Reliability assessment.
6	P64U84 Wafer#22	1.0	7B043542	40YA*456ESXA	TSSOP 20	Package Reliability assessment.
7	P64U84 Wafer#15	1.0	A503400M	T04I*479ESXA	WLCSP 20	Package Reliability assessment.
8	9R147498 Wafer#9	1.1	GQ2302AX	705B*456ESXZ	LQFP 7x7 48L	Die Reliability assessment.

3.2 Test plan and results summary

Table 5 - ACCELERATED LIFETIME SIMULATION TESTS CUT1.1
For LQFP 7x7 48L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Ta=125°C Duration= 168H Lot 8 Vcore :1V28 Vdd: 3V6	1	77	77	Lot8: 0/77	
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF 2kV class2	1	3	3	Lot8: 0/3	
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot8: 0/3	
Latch Up	JESD78	130°C	1	3	3	Lot8: 0/3	

Table 6 - ACCELERATED LIFETIME SIMULATION TESTS
For LQFP 7x7 48L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Ta=125°C Duration= 1200H Lot 1 Vcore :1V28 Vdd: 3V6	1	77	77	Lot1: 0/77	
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF 2kV class2	1	3	3	Lot1: 0/3	
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot1: 0/3	
Latch Up	JESD78	130°C	1	3	3	Lot1: 0/3	
EDR	JESD22-A117	10kcy EW @ 125°C then Storage HTB 150°C - Duration 1500H	1	77	77	Lot1: 0/77	
EDR	JESD22-A117	10kcy EW @ 25°C then Storage HTB 150°C - Duration 168h	1	77	77	Lot1: 0/77	
EDR	JESD22-A117	10kcy EW @ -40°C then Storage HTB 150°C - Duration 168H	1	77	77	Lot1: 0/77	
ELFR	JESD22-A108 JESD74	Ta=125°C Duration= 48hrs Vcore :1V28 Vdd : 3V6	1	500	500	Lot1: 0/500	

Table 7 - ACCELERATED ENVIRONMENT STRESS TESTS

For LQFP 7x7 48L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot1: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot1: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot1: 0/77	
UHAST	JESD 22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot1: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 Duration= 1000hrs ☒ After PC	1	77	77	Lot1: 0/77	
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot1: 0/3	

Note: Test method revision reference is the one active at the date of reliability trial execution

For LQFP 7x7 32L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot2:0/3	

Note: Test method revision reference is the one active at the date of reliability trial execution

For UFQFN 7x7 48L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot3: 0/3	

Note: Test method revision reference is the one active at the date of reliability trial execution

For UFQFN 5x5 32L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot4: 0/3	

Note: Test method revision reference is the one active at the date of reliability trial execution

For UFQFN 4x4 28L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot5: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot5: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot5: 0/77	
UHAST	JESD 22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot5: 0/77:	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 Duration= 1000hrs☒ After PC	1	77	77	Lot5: 0/77	
ESD CDM	ANSI/ESDA/ JEDEC JS-002		1	3	3	Lot5: 0/3	

Note: Test method revision reference is the one active at the date of reliability trial execution

For TSSOP 20

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot6: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot6: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot6: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 Duration= 1000hrs ☒ After PC	1	77	77	Lot6: 0/77	
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot6: 0/3	

For WLCSP 20

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot7: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot7: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot7: 0/77	
UHAST	JESD 22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot7: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 Duration = 1000hrs ☒ After PC	1	77	77	Lot7: 0/77	
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot7: 0/3	

Note: Test method revision reference is the one active at the date of reliability trial execution

Table 8 - PACKAGE ASSEMBLY INTEGRITY TESTS

For TSSOP 20

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including -Die shear -Die attach glue fillet	JESD 22B102 JESDB100/ B108	1	20	20	Lot6 : 0/20	

For UFQFN 4x4 28L

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including -Die shear -Die attach glue fillet	JESD 22B102 JESDB100/ B108	1	20	20	Lot5 : 0/20	

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD22-A103	High Temperature Storage Life
JESD22-A104	Temperature cycling
JESD22-A108	Temperature, Bias and Operating Life
JESD22-A110	Temperature Humidity Bake
JESD22-A113	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A117	Endurance and Data retention
JESD22-A118	Unbiased Highly Accelerated temperature & humidity Stress Test
J-STD-020	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices

5 GLOSSARY

HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
ESD HBM	Electrostatic discharge - human body model
ESD - CDM	Electrostatic Discharge - Charged device model
LU	Latch-up
CA	Construction analysis
HTSL	High temperature storage life
PC	Preconditioning
TC	Temperature Cycling
THB	Temperature Humidity Bias
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
DMS	ST Advanced Documentation Controlled system/ Documentation Management system

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Muriel GALTIER	Initial Release	Div. Quality Manager	Rousset	Pascal NARCHE	04-Dec-2020
			Q&R Quality Manager	Grenoble	Dominique GALIANO	04-Dec-2020
1.1	Muriel GALTIER	Intermediate Release	Q&R Quality Manager	Grenoble	Dominique GALIANO	27- Jan-2021
1.2	Muriel GALTIER	Intermediate Release	Q&R Quality Manager	Grenoble	Dominique GALIANO	18-Mar-2021
1.3	Muriel GALTIER	Intermediate Release	Q&R Quality Manager	Grenoble	Dominique GALIANO	11-Jul-2022
1.4	Octavia NDJOYE-KOGOU	Intermediate Release	Q&R Quality Manager	Grenoble	Dominique GALIANO	24-Nov-2022
1.5	Muriel GALTIER Octavia NDJOYE-KOGOU	Final Release	Q&R Quality Manager	Grenoble	Dominique GALIANO	25-Jan-2022

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PRODUCT/PROCESS CHANGE NOTIFICATION PCN14455 – Additional information

STM32G050x, STM32G051x and STM32G061x 64K - product enhancement - addendum to PCN13483

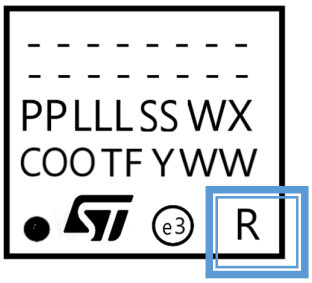
MDG – General Purpose Microcontrollers Division (GPM)

What are the changes?

Changes described in table below:

STM32G050x, **STM32G051x,** **STM32G061x**	Current Cut1.0	New Cut1.1
Die revision Marking **R**	“A”	“Z”

Example: Marking on package UFQFPN 7X7X0.55 48L



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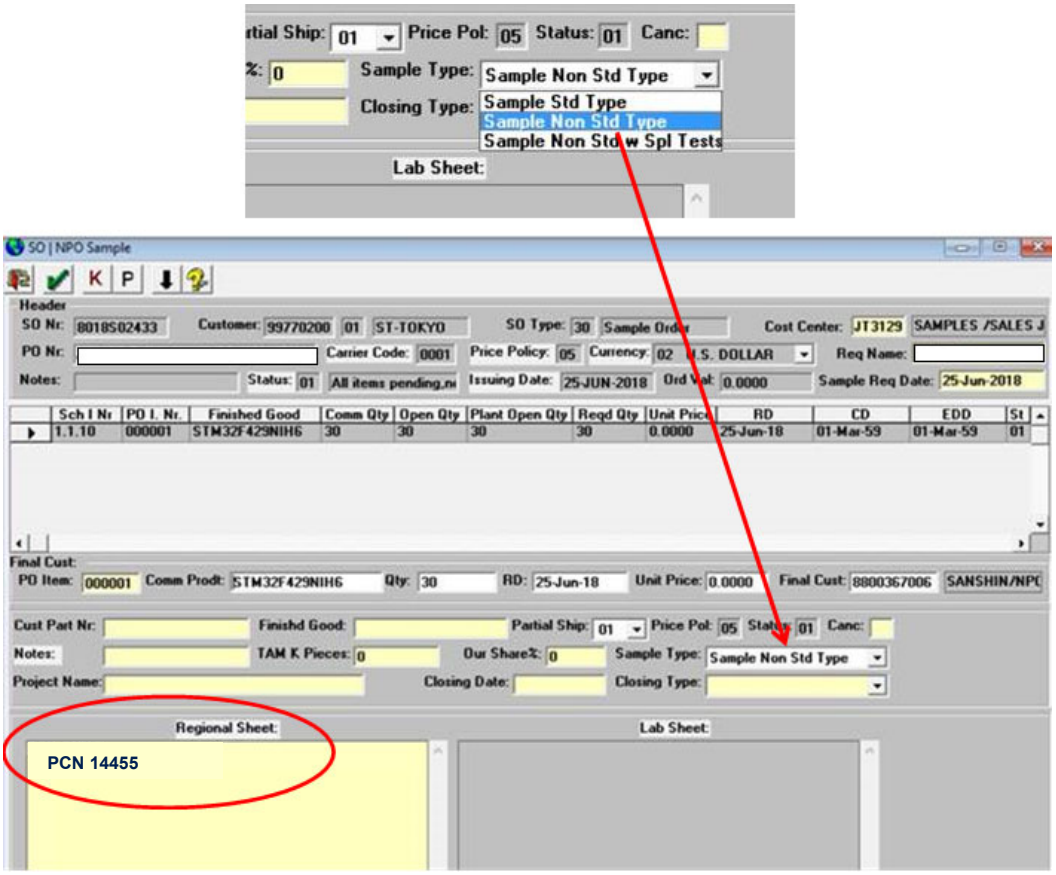
- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "**PCN14455**" into the NPO Electronic Sheet/**Regional Sheet**
- request sample(s) through Notice tool, indicating a single Commercial Product for each request



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PCN Title : STM32G050x, STM32G051x and STM32G061x 64K - product enhancement - addendum to PCN13483

PCN Reference : MDG/24/14455

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STM32G051K6T6	STM32G061C6U6	STM32G051C8T3TR
STM32G051K8U6	STM32G051C8U6TR	STM32G051C8U7
STM32G061G8U6	STM32G051K8T7TR	STM32G051F8P6
STM32G050F6P6	STM32G050C8T6	STM32G050K6T6
STM32G061K8T6	STM32G051C8U3TR	STM32G051F8Y3TR
STM32G061C8U6	STM32G051K8U7TR	STM32G051K8T6
STM32G051G8U6TR	STM32G051F8P3	STM32G051F6P6
STM32G051F8Y6TR	STM32G051K6U7TR	STM32G050K6T6TR
STM32G061K6T6	STM32G051C8U3	STM32G061F8Y6TR
STM32G050K8T6	STM32G061F6P6	STM32G051C6U6
STM32G051G8U3TR	STM32G051K8U7	STM32G051C8U6
STM32G061F8P6	STM32G051K6U7	STM32G051C6T6
STM32G051K6U6	STM32G051C8T3	STM32G061C6T6
STM32G061K6U6	STM32G051G8U3	STM32G051C8U7TR
STM32G051G8U6	STM32G051G6U6	STM32G061G6U6
STM32G050C6T6	STM32G051C8T6	STM32G051F8P3TR
STM32G061K8U6	STM32G061C8T6	

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