PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	MDG/24/14117
1.3 Title of PCN	STM32WBA52xx product enhancement for UFQFPN 7X7 48L & UFQFPN 5X5 32L listed Packages
1.4 Product Category	STM32WBA52CEU6 / STM32WBA52CGU6 for UFQFPN 7X7 48L STM32WBA52KEU6 / STM32WBA52KGU6 for UFQFPN 5X5 32L
1.5 Issue date	2024-02-28

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Ricardo Antonio DE SA EARP
2.1.2 Marketing Manager	Veronique BARLATIER
2.1.3 Quality Manager	Pascal NARCHE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Die redesign : Mask or mask set change with new die design like metallization (specifically chip frontside) or bug fix	TSMC FAB14 (Taiwan)

4. Description of change		
	Old	New
4.1 Description	STM32WBA52xx - (Die492 – cut1.0 revision A) product has limitation as described in Errata Sheet (ES0592 Rev2 / June 2023) - Core Floating-point state can be incorrectly cleared on some exception return faults (2.1.1) - RTC and TAMP Alarm flag may be repeatedly set when the core is stopped in debug (2.8.1) - USART Noise error flag set while ONEBIT is set (2.10.4)	STM32WBA52xx - (Die492 Cut2.0 revision B) product fixes those limitations as described in Errata Sheet (ES0592 Rev3). ES0592 Rev3 shall be available from ST Website (www.st.com) around march 2024.
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	functionality enhancement	

5. Reason / motivation for change	
5.1 Motivation	Improvements was implemented to increase robustness, performances and quality of our products.
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Traceability ensured by ST internal tools. Die revision changes from "A" to "B" on Package Marking

7. Timing / schedule	
7.1 Date of qualification results	2024-02-05
7.2 Intended start of delivery	2024-04-26
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation	
8.1 Description	14117 RER2112_MDG-GPM_STM32WBA5xx-Die492 Reliability Evaluation Report_v2.1.pdf

8.2 Qualification report and qualification results	Available (see attachment)	**Issue Date**	2024-02-28

9. Attachments (additional documentations)
14117 Public product.pdf 14117 RER2112_MDG-GPM_STM32WBA5xx-Die492 Reliability Evaluation Report_v2.1.pdf 14117 PCN14117_Additional information.pdf

10. Affected parts		
10. 1 Current		**10.2 New (if applicable)**
10.1.1 Customer Part No	**10.1.2 Supplier Part No**	**10.1.2 Supplier Part No**
	STM32WBA52CEU6	
	STM32WBA52CGU6	
	STM32WBA52KEU6	
	STM32WBA52KGU6	

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PRODUCT/PROCESS CHANGE NOTIFICATION
PCN14117 – Additional information

STM32WBA52xx product enhancement for UFQFPN 7X7 48L & UFQFPN 5X5 32L listed Packages

MDG – General Purpose Microcontrollers Division (GPM)

What is the change?

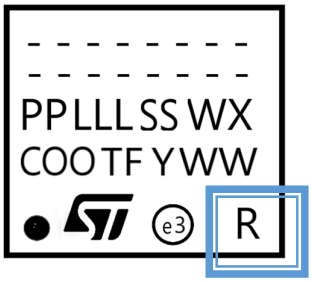
Package stack-up and die revision changes as shown below

	Current condition	New condition
Front-End Diffusion site	TSMC (Taiwan)	
STM32WBA52xx	Cut 1.0	Cut 2.0
Die revision Marking **R**	“A”	“B”

How can the change be seen?

Die revision change is visible on device marking.

Example on package UFQFPN 7X7X0.55 48L as below:



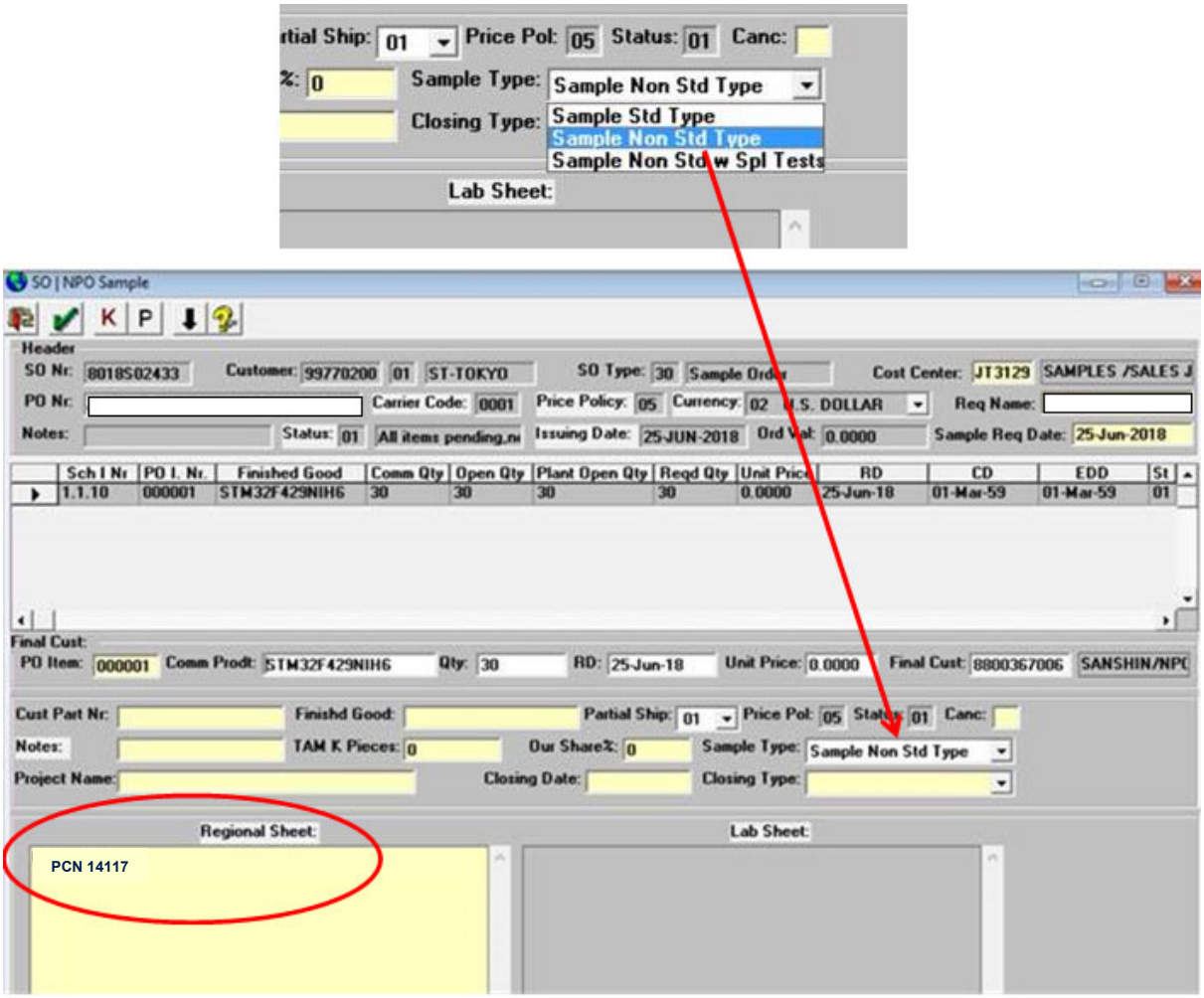
About Die Revision change

The STM32WBA5x product new revision (Die492 cut2.0 revision B) fixes limitations as described in Errata Sheet (ES0592 Rev3)

How to order samples?

For all samples request linked to this PCN, please:

- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "**PCN14117**" into the NPO Electronic Sheet/**Regional Sheet**
- request sample(s) through Notice tool, indicating a single Commercial Product for each request



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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : STM32WBA52xx product enhancement for UFQFPN 7X7 48L & UFQFPN 5X5 32L listed Packages

PCN Reference : MDG/24/14117

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STM32WBA52CGU6	STM32WBA52KGU6	STM32WBA52CEU6TR
STM32WBA52KEU6	STM32WBA52CEU6	

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External
Reliability Evaluation Report
MDG-GPM-RER2112
STM32WBA5xx 1M (492x66)
Reliability Evaluation Purpose **(New product qualification)**

General Information		Traceability	
Commercial Product	STM32WBA50KGU6 STM32WBA52CGU6 STM32WBA52CGU6U STM32WBA52CEU6 STM32WBA52CEU6TR STM32WBA52KGU6 STM32WBA52KEU6 STM32WBA54CGU6 STM32WBA54CGU7 STM32WBA54KGU6 STM32WBA54KGU7 STM32WBA55CEU6 STM32WBA55CGU6U STM32WBA55CGU6 STM32WBA55CGU6TR STM32WBA55CGUTR STM32WBA55CGU7 STM32WBA55UGI6 STM32WBA55UGI6U STM32WBA55UGI7 STM32WBA55UGI7U	**Diffusion Plant**	: TSMC, FAB14, TAIWAN.
Product Line	: 492x66	**Assembly Plant**	: JSCC/ASE
Die revision	: X492XXXA (cut1.0) : X492XXXB (cut2.0)		
Product Description	: STM32WBA5xx		
Package	: UFQFN48-LDO : UFQFN48-SMPS : UFQFN32 : UFBGA59	**Reliability Assessment**	
Silicon Technology	: 40nm eFlash Generic TSMC	**Pass**	☒
Division	: GPM	**Fail**	☐

Reliability Maturity *: 30*	**Investigation required** ☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	12-Jan-2023	Muriel GALTIER	Division Quality & Reliability Engineer
1.1	12-Sept-2023	Muriel GALTIER Cédric CHASTANG	Division Quality & Reliability Engineer BE Quality Engineer
1.2	28-Sept-2023	Muriel GALTIER	Division Quality & Reliability Engineer
2.0	1-Dec-2023	Muriel GALTIER	Division Quality & Reliability Engineer
2.1	1-Feb-2024	Muriel GALTIER Cédric CHASTANG	Division Quality & Reliability Engineer BE Quality Engineer

REV 1.0 APPROVED BY:

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	16 – Jan – 2023
BE Quality Manager	Rousset	Berengere ROUTIER-SCAPPUCCI	17 – Jan – 2023
Division Quality Manager	Rousset	Pascal NARCHE	18 – Jan – 2023

REV 1.1 APPROVED BY:

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	15-Sept -2023
BE Quality Manager	Rousset	Berengere ROUTIER-SCAPPUCCI	14-Sept -2023

REV 1.2 APPROVED BY:

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	28-Sept -2023

REV 2.0 APPROVED BY:

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	04-Dec-2023

REV 2.1 APPROVED BY:

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	05-Feb -2024
BE Quality Manager	Rousset	Berengere ROUTIER-SCAPPUCCI	05-Feb -2024

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation STM32WBA50KGU6, STM32WBA52CGU6, STM32WBA52CGU6U, STM32WBA52CEU6, STM32WBA52CEU6TR, STM32WBA52KGU6, STM32WBA52KEU6, STM32WBA54CGU6, STM32WBA54CGU7, STM32WBA54KGU6, STM32WBA54KGU7, STM32WBA55CEU6, STM32WBA55CGU, STM32WBA55CGUTR, STM32WBA55CGU6U, STM32WBA55CGU6, STM32WBA55CGU7, STM32WBA55CGU6TR, STM32WBA55UGI6, STM32WBA55UGI6U, STM32WBA55UGI7, STM32WBA55UGI7U – Die492xx66.

Test vehicle is described here below:

Product	Process or Package	Diffusion or Assembly plant
STM32WBA54CGU7	CMOS040 eFlash, UFQFN48-LDO	TSMC FAB14, JSCC
STM32WBA55CGU7	CMOS040 eFlash, UFQFN48-SMPS	TSMC FAB14, JSCC
STM32WBA54KGU7	CMOS040 eFlash, UFQFN32	TSMC FAB14, JSCC
STM32WBA52KGU6	CMOS040 eFlash, UFQFN32	TSMC FAB14, JSCC
STM32WBA55UGI7	CMOS040 eFlash, UFBGA59	TSMC FAB14, ASE

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard.

1.2 Reliability Strategy

The STM32WBA5x – (Die 492) – will be processed in the TSMC 40eF which is a qualified technology in GPM group through U5 family, but embedded RF IP not qualified. STM32U585x (die 482):

The STM32WBA5x (Die 492) device is assembled in the following packages already qualified for this product family:

Package	Reference	Assy Plant location	Final Test Plant location
UFQFPN 48L 7x7 0.55	RERMCD1919	JSCC	JSCC

Based on these data, and according to “RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION” specification (DMS 0061692), the following qualification strategy has been defined:

- Die Qualification:

  Full reliability exercise on 3 diffusion lots for Cut1.0 (except for NVM – Only 1 lot)

Full reliability exercise on 1 diffusion lot for Cut2.0 (except for SMPS – reduce to HTOL 168h as no modification between the 2 cuts)

- Package Qualification:

The reliability test plan and result summary are presented in the following tables:

Package	Body	Pitch	Package Code	Wire	Assy	Bounding Option	Trial
UFQFPN-LDO 48L	7x7	0.55	A0B9	Gold	JSCC	-	1 full qual lot including CA
UFQFPN-LDO 48L	7x7	0.55	A0B9	Gold	JSCC	New Bonding	1 full qual lot including CA
UFQFN32	5x5	0.55	A0B8	Gold	JSCC	-	3 full qual lots including CA
UFQFN32	5x5	0.55	A0B8	Gold	JSCC	New Bonding	2 full qual lots including CA
UFQFPN-LDO 48L	7x7	0.55	A0B9	Gold	JSCC	-	CDM cut2.0
UFQFPN-SMPS 48L	7x7	0.55	A0B9	Gold	JSCC	-	CDM cut2.0
UFBGA59	5x5	0.5	B0FS	Gold	ASE	-	1 full qual lot including CA

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, production maturity is granted for the STM32WBA50KGU6, STM32WBA52CGU6, STM32WBA52CGU6U, STM32WBA52CEU6, STM32WBA52CEU6TR, STM32WBA52KGU6, STM32WBA52KEU6, STM32WBA54CGU6, STM32WBA54CGU7, STM32WBA54KGU6, STM32WBA54KGU7, STM32WBA55CEU6, STM32WBA55CGU, STM32WBA55CGUTR, , STM32WBA55CGU6U, STM32WBA55CGU6, STM32WBA55CGU7, STM32WBA55CGU6TR, STM32WBA55UGI6, STM32WBA55UGI6U, STM32WBA55UGI7, STM32WBA55UGI7U on all packages listed above.

Refer to Section 3.0 for reliability test results.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

Die 492 as part of the new family STM32WBA, is diffused in TSMC 40nm ULP eFlash process (as die 482 – U5 family) with RF IP.
The objective is to build a new 2.4 GHz RF ultralow power family start with 1MB at a competitive cost by improving performance (horsepower) with best-in-class low power both static and dynamic modes. The new family provides single core architecture based on the Cortex-M33 (Teal) with security features. This new family is targeting IOT, medical, metering, safety, and any battery-operated applications. With following standards: Bluetooth low energy 5.2, IEEE802.15.4, ANT+, Zigbee 3.0, and Thread.

For additional information concerning the product behavior, refer to STM32WBA5xx datasheet.

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information	
TSMC FAB14/TAIWAN	
Wafer fab name / location	TSMC FAB14/TAIWAN
Wafer diameter (inches)	12
Wafer thickness (µm)	775
Silicon process technology	40nm EFLASH GENERIC TSMC
Number of masks	50
Die finishing front side (passivation) materials/thicknesses	AL, OXIDE NITRIDE
Die finishing back side Materials	RAW SILICON
Die area (Stepping die size)	8.336mm² (X=2779um, Y=2999.6um)
Die pad size	54.9, 54.9 µm
Sawing street width (X,Y) (µm)	80,80
Metal levels/Materials/Thicknesses	Metal 1 Cu 0.125 µm Metal 2 Cu 0.145 µm Metal 3 Cu 0.145 µm Metal 4 Cu 0.145 µm Metal 5 Cu 0.145 µm Metal 6 Cu 0.850 µm Metal 7 Cu 3.500 µm Metal 8 Al 1.500 µm
Die over coating (material/thickness)	NO
FIT level (Ea=0.7eV, C.L: 60%, 55°C)	2 FITs
Soft Error Rate - Alpha SER [FIT/Mb] - Neutron SER [FIT/Mb] - Conditions	RAM (VDD:1v2, 125°C) • ALPHA SER: <156 FIT/Mb • NEUTRON SER: <359 FIT/Mb • SRAM MAX SIZE 8MB FLASH: (VDD:1v2, 125°C) • TOTAL SER: <10 FIT/Mb FLIP-FLOP: (VDD:1v2, 125°C) • ALPHA SER: <417 FIT/MFF • NEUTRON SER: <356 FIT/MFF ALPHA SER 0.001α/cm²/h NEUTRON SER 14n/cm²/h
Wafer Level Reliability - Electro-Migration (EM) - Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) - Hot Carrier Injection (HCI) - Negative Bias Thermal Instability (NBTI) - Stress Migration (SM)	Yes
Other Device(s) using same process	481; 455; 482

2.2.2 Assembly information

Table 2

Assembly Information	
Package 1– UFQFPN 7X7X0.55 48L	
Assembly plant name / location	STATSCHIPPAC(JSCC), CHINA
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150±25
Die sawing method	LASER GROOVING + MECHANICAL SAWING
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	HD LF FOR UQFN7x7 48L Sn 5.2mmSq Groove
Lead frame finishing (material/thickness)	Pure Tin (e3) – Tolerance 7 to 20 µm
Die attach material/type(glue/film)/supplier	EN4900GC (GLUE)/Hitachi
Wire bonding material/diameter	Gold/0.8mils
Molding compound material/supplier/reference	RESIN SUMITOMO EME-G770
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3
Assembly Information	
Package 2 – UFQFPN 5X5X0.55 32L	
Assembly plant name / location	STATSCHIPPAC(JSCC), CHINA
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150±25
Die sawing method	LASER GROOVING + MECHANICAL SAWING
Bill of Material elements	
Lead frame/Substrate material/supplier/reference	HD LF FOR UQFN 5x5 32L Sn PAD 3.9 SQ No Groove
Lead frame finishing (material/thickness)	Pure Tin (e3) – Tolerance 7 to 20 µm
Die attach material/type(glue/film)/supplier	DAF FH9011T / Hitachi
Wire bonding material/diameter	Gold/0.8mils
Molding compound material/supplier/reference	RESIN SUMITOMO G770
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3
Assembly Information	
Package 3 – UFBGA59 5x5x0.6	
Assembly plant name / location	ASEKH, TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	70um +/- 10um
Die sawing method	LASER GROOVING+ MECHANICAL SAWING
Bill of Material elements	
Substrate material/supplier/reference	UFBGA 5x5x0.6 59 P0.5 ASE A29309-A
Balls metallurgy/diameter (BGA)	200 DIAM SN96.5 AG3.5%
Die attach material/type(glue/film)/supplier	D/A Tape ABLESTICK ATB-125
Wire bonding material/diameter	Wire gold 0.8mils
Molding compound material/supplier/reference	KYOCERA G1250AAS ULA

Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	ST Grenoble (France) / Shenzhen BE Lab / Muar BE lab

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
1	P67M01/1	1.0	9R14749611/ GQ21827T	74MI*492ESXA	UFQFPN 7X7X0.55 48L LDO	Die Reliability
2	P67M02/19	1.0	9R14254612/ GQ22025T	74MI*492ESXA	UFQFPN 7X7X0.55 48L LDO	Die / Package Reliability
3	P67M03/14	1.0	9R14279811/ GQ22025Y	74MI*492ESXA	UFQFPN 7X7X0.55 48L LDO	Die Reliability
4	P67M03/17	1.0	9R14279816/ GQ2432GG	80MI*492ESXA	UFQFPN 7X7X0.55 48L LDO	Package reliability assessment for new bonding including CA
5	P67M02/20	1.0	9R14254616/ GQ221281	71MG*492ESXA	UFQFN32 5X5X0.55	Package Reliability
6	P67M02/20	1.0	9R14254618/ GQ22226G	71MG*492ESXA	UFQFN32 5X5X0.55	Package Reliability
7	P67M02/22	1.0	9R1425461A/ GQ2332A3	71MG*492ESXA	UFQFN32 5X5X0.55	Package Reliability
8	P67M02/10	1.0	9R148248/GQ 3092BC	82MG*492ESXA	UFQFN32 5X5X0.55	Package reliability assessment for new bonding (including CA focus bonding)

9	P67M02/13	1.0	9R1482481H0000/ GQ3292AK	82MG*492ESXA	UFQFN32 5X5X0.55	CA sawing assessment (New DAF)
10	P67M01 / 1	1.0	9R14749612/ GQ21827S	72MI*492ESXA	UFQFPN 7X7X0.55 48L SMPS	Die Reliability
11	P67M02 / 19	1.0	9R14254614/ GQ22123Z	72MI*492ESXA	UFQFPN 7X7X0.55 48L SMPS	Die Reliability
12	P67M03 / 14	1.0	9R14279812/ GQ221240	72MI*492ESXA	UFQFPN 7X7X0.55 48L SMPS	Die Reliability
13	P6AF13 / 06	2.0	9R31615816/ GQ3322BZ	74MI*492ESXB	UFQFPN 7X7X0.55 48L LDO	Die / Package Reliability
14	P6AF13 / 08	2.0	9R31716615/ GQ33228P	72MI*492ESXB	UFQFPN 7X7X0.55 48L SMPS	Die / Package Reliability
15	P6AF13 / 03	2.0	GQ336269/9R3171661B	71MG*492ESXB	UFQFN32 5X5X0.55	Package reliability
16	P67M02 / 21	1.0	AA222001/9R142546	E17I*492ESXA	UFBGA59 5x5x0.6 pitch 0.5	Package reliability
17	P6AF13 / 02	2.0	AA336017/3R317166	E17I*492ESXB	UFBGA59 5x5x0.6 pitch 0.5	Package Reliability

3.2 Test plan and results summary

Table 5 – ACCELERATED LIFETIME SIMULATION TESTS

UFQFPN 7X7X0.55 48L LDO

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Ta=125°C Duration= 1200H 3V6	4	77	308	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot 13: 0/77	
ESD HBM	ANSI/ESDA/ JEDEC JS-001	Ta 25°C Min 1KV (Class 1C) Target 2KV (Class 2)	4	3	12	Lot1: 0/3 Lot2: 0/3 Lot3: 0/3 Lot13: 0/3	Pass at 2kV
LatchUp	JESD78	130°C (class2)	4	3	12	Lot1: 0/3 Lot2: 0/3 Lot3: 0/3 Lot13: 0/3	
EDR	JESD22-A117 JESD22-A103	@ 125°C 10k cycles (On 8Mbits on each of the 2 NVM BANKs) 100k cycles (On 2Mbits on each of the 2 NVM BANKs) then Storage HTB 150°C – Duration 1500H	2	77	154	Lot1: 0/77 Lot13: 0/77	
EDR	JESD22-A117 JESD22-A103	@ 25°C 10k cycles (On 8Mbits on each of the 2 NVM BANKs) 100k cycles (On 2Mbits on each of the 2 NVM BANKs) then Storage HTB 150°C – Duration 168h	2	77	154	Lot1: 0/77 Lot13: 0/77	
EDR	JESD22-A117 JESD22-A103	@ -40°C 10k cycles (On 8Mbits on each of the 2 NVM BANKs) 100k cycles (On 2Mbits on each of the 2 NVM BANKs) then Storage HTB 150°C – Duration 168h	2	77	154	Lot1: 0/77 Lot13: 0/77	

ELFR	MIL-STD-883 Method 1005JESD22-A108 JESD74	Ta=125°C Duration= 48hrs 3V6	4	500	2000	Lot1: 0/500 Lot2: 0/500 Lot3: 0/500 Lot13: 0/500	

UFQFPN 7X7X0.55 48L SMPS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Ta=125°C Duration= 1200H 3V6	3	77	231	Lot10: 0/77 Lot11: 0/77 Lot12: 0/77	Stress done on Chip Board
HTOL	JESD22 A108	Ta=125°C Duration= 168H 3V6	1	77	77	Lot14 : 0/77	Stress done on Chip Board

UFQFPN 7X7X0.55 48L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	Ta 25°C Min 250V (class C1) Target 500V (Class C2a)	3	3	9	Lot2: 0/3 Lot13: 0/3 Lot14: 0/3	Pass 500V
PC	0098041 JSTD 020 JESD 22-A113 7191395	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot2: 0/308	
TC	MIL-STD-883 Method 1010 JESD 22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 2: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 2: 0/77	
HTSL	JESD 22-A103	Ta=150° , Duration= 1000hrs ☒ After PC	1	77	77	Lot 2: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 2: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution

UFQFPN 7X7X0.55 48L New Bonding

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	Ta 25°C Min 250V (class C1) Target 500V (Class C2a)	1	3	3	Lot 4: 0/3	Pass 500V
PC	0098041 JSTD 020 JESD 22-A113 7191395	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 4: 0/308	
TC	MIL-STD-883 Method 1010 JESD 22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 4: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 4: 0/77	
HTSL	JESD 22-A103	Ta=150° , Duration= 1000hrs ☒ After PC	1	77	77	Lot 4: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 4: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution

UFQFPN 5X5X0.55 32L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	Ta 25°C Min 250V (class C1) Target 500V (Class C2a)	4	3	12	Lot5: 0/3 Lot6: 0/3 Lot7: 0/3 Lot15: 0/3	Pass 500V
PC	0098041 JSTD 020 JESD 22-A113 7191395	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	3	308	924	Lot5: 0/308 Lot6: 0/308 Lot7: 0/308	
TC	MIL-STD-883 Method 1010 JESD 22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	3	77	231	Lot 5: 0/77 Lot 6 0/77 Lot 7: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	3	77	231	Lot 5: 0/77 Lot 6 0/77 Lot 7: 0/77	
HTSL	JESD 22-A103	Ta=150° , Duration= 1000hrs ☒ After PC	3	77	231	Lot 5: 0/77 Lot 6 0/77 Lot 7: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	3	77	231	Lot 5: 0/77 Lot 6 0/77 Lot 7: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution

UFQFPN 5X5X0.55 32L New Bonding

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	Ta 25°C Min 250V (class C1) Target 500V (Class C2a)	1	3	3	Lot 8: 0/3	Pass 500V
PC	0098041 JSTD 020 JESD 22-A113 7191395	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 8: 0/308	
TC	MIL-STD-883 Method 1010 JESD 22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 8: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 8: 0/77	
HTSL	JESD 22-A103	Ta=150° , Duration= 1000hrs ☒ After PC	1	77	77	Lot 8: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 8: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution

UFBGA59 5X5X0.6 pitch 0.5

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)

ESD CDM	ANSI/ESDA/ JEDEC JS-002	Ta 25°C Min 250V (class C1) Target 500V (Class C2a)	2	3	6	Lot 16: 0/3 Lot 17: 0/3	Pass 500V
PC	0098041 JSTD 020 JESD 22-A113 7191395	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 16: 0/308	
TC	MIL-STD-883 Method 1010 JESD 22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 16: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 16: 0/77	
HTSL	JESD 22-A103	Ta=150°, Duration= 1000hrs ☒ After PC	1	77	77	Lot 16: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 16: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution

Table 7 – PACKAGE ASSEMBLY INTEGRITY TESTS

UFQFPN 7X7X0.55 48L

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including - Wire bond shear -Wire bond pull	Internal ST specs	1	50	50	Lot2: 0/50	Pass SHZ-CA_22_00206

UFQFPN 7X7X0.55 48L New Bonding

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including - Wire bond shear -Wire bond pull	Internal ST specs	1	50	50	Lot4: 0/50	Pass (SHZ-CA_22_00294)

UFQFPN 5X5X0.55 32L

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including - Wire bond shear -Wire bond pull	Internal ST specs	1	50	50	Lot5: 0/50	Pass (SHZ - CA_23_00065)

UFQFPN 5X5X0.55 32L New Bonding

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including - Wire bond shear -Wire bond pull - Wafer sawing (new DAF)	Internal ST specs	2	50	100	Lot8: 0/50 Lot9: 0/50	Pass (SHZ - CA_23_00303) Pass (MUAR_23_00032)

UFBGA59 5X5X0.6 pitch0.5

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)

CA	Construction Analysis including - Wire bond shear -Wire bond pull	Internal ST specs	1	50	50	Lot16: 0/50	Pass (SHZ – CA_23_00288)

- Applicable and reference documents

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A117	Endurance and Data retention
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A101:	Temperature Humidity Bias

4 GLOSSARY *(MANDATORY)*

Reference	Short description
HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up
CA	Construction Analysis
DAF	Die Attach Film

5 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Muriel GALTIER Cédric CHASTANG	Initial release for waiver 29 on UFQFN48-LDO package (include new bonding)	Division Back-End Quality Manager	Rousset	Berengere ROUTIER-SCAPPUCCI	17- Jan - 2023
			Division Quality & Reliability Manager	Grenoble	Dominique GALIANO	16- Jan - 2023
			Division Quality Manager	Rousset	Pascal NARCHE	18- Jan - 2023

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.1	Muriel GALTIER Cédric CHASTANG	Add UFQFN48-SMPS and QFN32	Division Quality & Reliability Manager	Grenoble	Dominique GALIANO	15- Sep - 2023

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.2	Muriel GALTIER	Update on package list	Division Quality & Reliability Manager	Grenoble	Dominique GALIANO	28- Sep - 2023

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
2.0	Muriel GALTIER	Cut 2.0 qualification update for QFN48 packages	Division Quality & Reliability Manager	Grenoble	Dominique GALIANO	4- Dec - 2023
2.1	Muriel GALTIER Cédric CHASTANG	Die qualification on cut 2.0 completed. Add QFN32 and BGA59 for cut2.0	Division Quality & Reliability Manager	Grenoble	Dominique GALIANO	05-02-2014
			Division Back-End Quality Manager	Rousset	Berengere ROUTIER-SCAPPUCCI	05-02-2014

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