PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	MDG/23/13948
1.3 Title of PCN	STM32H563x - product enhancement
1.4 Product Category	STM32H563RIT6 STM32H563VIT6 STM32H563ZIT6
1.5 Issue date	2023-07-04

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Ricardo Antonio DE SA EARP
2.1.2 Marketing Manager	Veronique BARLATIER
2.1.3 Quality Manager	Pascal NARCHE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Die redesign : Mask or mask set change with new die design like metallization (specifically chip frontside) or bug fix	ST Crolles 300 (France)

4. Description of change		
	Old	New
4.1 Description	STM32H563x- (Die484 – cut1.1 revision Z) product enhancement shows limitations as described in first release of the Errata Sheet (ES0561 - Rev 1 - March 2023)	STM32H563x - (Die484 - cut1.3 revision X) product enhancement fixes those limitations as described in Errata Sheet (ES0565 - Rev 3 - June 2023)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	Functionality enhancement	

5. Reason / motivation for change	
5.1 Motivation	Improvements was implemented to increase robustness, performances and quality of our products.
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Traceability ensured by ST internal tools. Die revision changes from "Z" to "X" on Package Marking.

7. Timing / schedule	
7.1 Date of qualification results	2023-09-20
7.2 Intended start of delivery	2023-10-10
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13948 MDG-MCD-RER2111_STM32H5x3x_484-2M.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2023-07-04

9. Attachments (additional documentations)
13948 Public product.pdf 13948 MDG-MCD-RER2111_STM32H5x3x_484-2M.pdf 13948 PCN13948_Additional information.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STM32H563IIK6	
	STM32H563VIT6	
	STM32H563ZIT6	

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Reliability Evaluation Report

MDG-GPM-RER2111

STM32H5xx (484X66)

New product qualification

General Information	
Commercial Product	STM32H5xx
Product Line	: 484X66
Die revision	: 484XXXX (cut1.3)
Product Description	: STM32H5 2MB eSTM40
Package	: UFBGA10x10 176+25L, LQFP20x20 144L, LQFP14x14 100L, LQFP 10x10 64L
Silicon Technology	: CMOS eSTM40 40nm
Division	: MDG-GPM
Reliability Maturity	: *20->W29*

Traceability	
Diffusion Plant	: ST C300 (12'') France
Assembly Plant	: ASE KH, JSCC

Reliability Assessment	
Pass	☒
Fail	☐
Investigation required	☐

Note: this report is a summary of the reliability trials performed in good faith by STMicroelectronics to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).

Version	Date	Author	Function
1.0	05-Dec-2022	P. ADAM	PQR Engineer
2.0	12-Jun-2023	P. ADAM	PQR Engineer

Approved by:
V2.0

Function	Location	Name	Date
Division Q&R Responsible	Grenoble	Dominique GALIANO	13-June-2023
Division Quality Manager	Rousset	Pascal NARCHE	13-June-2023
BE Quality Manager	Rousset	Berengere ROUTIER-SCAPPUCCI	14-June-2023

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present the results of the reliability evaluation performed on STM32H5xx 2MBytes – Die 484XXXX, diffused in ST Crolles 300 (CMOS eSTM40 40 nm)

Test vehicle is described here below:

Product	Process or Package	Diffusion, Assembly plant	Comment
STM32H563IIK6	eSTM40, UFBGA 10x10 176+25L	ST C300, ASE KH	LDO version
STM32H563ZIT6	eSTM40, LQFP 20x20 144L	ST C300, ASE KH	LDO version
STM32H563VIT6	eSTM40, LQFP 14x14 100L	ST C300, ASE KH	LDO version
STM32H563RIT6	eSTM40, LQFP 10x10 64L	ST C300, JSCC	LDO version

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard.

1.2 Conclusion

First reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing for the STM32H5xx – Die 484XXXX, diffused in ST Crolles 300, France, and assembled with the following packages UFBGA 10x10 176+25L, LQFP 20x20 144L, LQFP 14x14 100L at ASEKH and LQFP 10x10 64L at JSCC.

The completion of all reliability tests is forecasted in 2023'Q4. Results will be communicated in another version of this report.

The report will be updated when new reliability results are available with other packages.

Refer to Section 3.0 for reliability test results.

1.3 Reliability Strategy

The STM32H5xx - Die 484XXXX new design with a 100K cycles NVM on 48KBytes, new SRAM, new square pad staggered. The eSTM40 technology is deployed on die 474 with 128KBytes NVM.

STM32H7x (die 480)	RERMCD1401
STM32H503x (die 474)	RERMCD2107

Based on these data, and according to "RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION" specification (DMS 0061692), the following qualification strategy has been defined:

- Die Qualification:

Full reliability exercise on 2 diffusion lots for Cut 1.0 LDO
Full reliability exercise on 1 diffusion lot for Cut 1.1 LDO
Full reliability exercise on 1 diffusion lot for Cut 1.3 LDO

Package	Body	Pitch	Package Code	Wire	Assy	Bounding Option	Trial
UFBGA 176+25L	10x10	0.65	A0E7	Copper	ASE KH	LDO	4 full lots

- Package Qualification:

The STM32H5xx (484X66) device is assembled in the following packages already qualified:

Package	Body	Pitch	Package Code	Wire	Reference	Assy Plant location
UFBGA 176+25L	10x10	0.65	A0E7	CuPd	MCD RER2021	ASE KH
LQFP 144L	20x20	0.5	1A	Gold	MCD RER1815	ASE KH
LQFP 100L	14x14	0.5	1L	Gold	MCD RER1815	ASE KH
LQFP 64L	10x10	0.5	5W	Gold	MCD RER1621 MCD RER1606	JSCC

The reliability test plan summary is presented in the following table:

Package	Body	Pitch	Package Code	Wire	Assy	Bounding Option	Trial
UFBGA 176+25L	10x10	0.65	A0E7	CuPd	ASE KH	LDO	2 lots
LQFP 144L	20x20	0.5	1A	Gold	ASE KH	LDO	2 lots
LQFP 100L	14x14	0.5	1L	Gold	ASE KH	LDO	1 lot
LQFP 64L	10x10	0.5	5W	Gold	JSCC	LDO	3 lots

Note: In order to cover all I/O options, some additional ESD HBM & LU trials have been planned for some package options.

2 PRODUCT CHARACTERISTICS

2.1 Generalities

The STM32H5xx device - die 484XXXX - is a security enhanced microcontroller based on ARM® Cortex® M33 32-bit RISC core operating at a frequency of 240MHz with 2Mbytes NVM with ECC support.
For additional information concerning the product behavior, refer to the datasheet.

2.2 Traceability

2.2.1 Wafer fab information

Table 1

Wafer fab information	
FAB1	
Wafer fab name / location	ST Crolles 300 / France
Wafer diameter (inches)	12
Wafer thickness (µm)	775+/-25 UM
Silicon process technology	CMOSE40 ULP
Number of masks	52
Die finishing front side (passivation) materials/thicknesses	PSG (PECVD) (Oxide 500nm) + NITRIDE (SiN 600nm)
Die finishing back side Materials/thicknesses	RAW SILICON
Die area (Stepping die size)	3518x3297 um
Die pad size	55 µm
Sawing street width (X, Y) (µm)	(80.0,80.0) µm
Metal levels/Materials/Thicknesses	7M2T Metal 1 Cu 0.110 µm Metal 2 Cu 0.140 µm Metal 3 Cu 0.140 µm Metal 4 Cu 0.140 µm Metal 5 Cu 0.140 µm Metal 6 Cu 0.860 µm Metal 7 Cu 0.860 µm Metal 8 Ta/TaN/AlCu 1.525 µm
Die over coating (material/thickness)	No
FIT level (Ea=0.7eV, C.L: 60%, 55°C)	FIT not yet available at product level at qualification date
Soft Error Rate - Alpha SER [FIT/Mb] - Neutron SER [FIT/Mb] - Conditions	Alpha SER: 470 Fit/Mb Neutron SER: 900 Fit/Mb conditions: Alpha SER 0.001 α/cm²/h, SER/SEL at 125°C 14 n/cm²/h (>400MeV)
Wafer Level Reliability - Electro-Migration (EM) - Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) - Hot Carrier Injection (HCI) - Negative Bias Thermal Instability (NBTI) - Stress Migration (SM)	Yes
Other Device(s) using same process	STM32H503x 128Kbytes (die 474)

2.2.2 Assembly information

Table 2

Assembly Information	
Package 1 - A0E7, UFBGA176+25L 10x10	
Assembly plant name / location	ASE KH
Pitch (mm)	0.65
Die thickness after back-grinding (µm)	75 +/- 10 um
Die sawing method	Laser grooving + mechanical sawing
Bill of Material elements	
Substrate reference / supplier	A29941 / ASE
Die attach type / supplier	ATB-125 / ABLESTICK
Wire bonding material / diameter	CuPd / 0.8 mils
Balls metallurgy / diameter	SN96.5 AG3.5% / DIAM. 200
Molding reference / supplier	G1250AAS ULA / KYOCERA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Table 3

Assembly Information	
Package 2 - 1A, LQFP144L 20x20	
Assembly plant name / location	ASE KH
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/- 25 um
Die sawing method	Laser grooving + mechanical sawing
Bill of Material elements	
Lead frame reference	LF# A25582 LQ20 144 Pure Tin C7025 6.6sq
Die attach material type / supplier	GLUE EPOXY CRM 1076WA / SUMITOMO
Wire bonding material / diameter	Gold / 0.8 mils
Molding compound material reference / supplier	RESIN EME-G631SH / SUMITOMO
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Table 4

Assembly Information	
Package 3 - 1L, LQFP100L 14x14	
Assembly plant name / location	ASE KH
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/- 25 um
Die sawing method	Laser grooving + mechanical sawing
Bill of Material elements	
Lead frame reference	LF# A25516 LQ14 100L Pure Tin C7025 6.6sq Slot
Die attach material type /supplier	GLUE EPOXY CRM 1076WA / SUMITOMO
Wire bonding material / diameter	Gold / 0.8 mils
Molding compound material reference / supplier	MOLDING RESIN EME-G631SH / SUMITOMO
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

Table 5

Assembly Information	
Package 4 - 5W, LQFP64L 10x10	
Assembly plant name / location	JSCC
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	375 +/- 25 um
Die sawing method	Laser grooving + mechanical sawing
Bill of Material elements	
Lead frame reference / supplier	LQ10 64L 207sq Eff slots STMP LF / JSCC
Die attach material type / supplier	D/A 3230 / Ablestik
Wire bonding material / diameter	Gold / 0.8 MIL
Molding reference / supplier	low alpha G631SHQ / SUMITOMO
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

2.2.3 Reliability testing information

Table 6

Reliability Testing Information	
Reliability laboratory name / location	GRAL / ST Grenoble
	ST Shenzhen

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 7 - Die & Packages Lots

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
1	Q125426 / 10	1.0	AA236032	E0MR*484XXXA	ASE KH Copper UFBGA176+25L LDO	DIE & PKG reliability
2	Q130120 / 10	1.0	AA236030	E0MR*484XXXA	ASE KH Copper UFBGA176+25L LDO	DIE & PKG reliability
3	Q127276 / 19	1.1	AA236031	E0MR*484XXXZ	ASE KH Copper UFBGA176+25L LDO	DIE Reliability
4	Q236268 / 15	1.3	n.a.	D1MR*484ESXX	ASE KH Copper UFBGA176+25L LDO	DIE Reliability
5	Q237555 / 4, 7, 9	1.3	AA315167	21MR*484XXXX	ASE KH Copper UFBGA176+25L LDO	DIE Reliability
6, 7	VQ127276 / 7, 9 VQ213903 / 7, 9	1.0 1.1	AA237201 AA310003	E01A*484ESXA E01A*484ESXZ	ASE KH Gold LQFP144L LDO	PACKAGE Reliability
8	VQ127276 / 7, 9	1.0	AA237200	E01L*484ESXA	ASE KH Gold LQFP100L LDO	PACKAGE Reliability
9, 10, 11	VQ127276 / 13	1.0	GQ2382DA GQ24224X GQ241233	705W*484ESXA	JSCC Gold LQFP64L LDO	PACKAGE Reliability

3.2 Test plan and results summary

ACCELERATED LIFETIME SIMULATION TESTS

Table 8 - UFBGA 10x10 176+25L, ASE KH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	Ta = 125°C, 3V6 Duration = 1200H Duration = 600h	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	Cut 1.0 LDO Cut 1.0 LDO Cut 1.1 LDO (1200h in 2023 July)
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF 2kV class1	2	3	6	Lot 1: 0/3 Lot 4: 0/3 Lot 5: ongoing	Cut 1.0 LDO Cut 1.3 LDO Cut 1.3 LDO in 2023 July
Latch-Up	JESD78	130°C	2	3	6	Lot 1: 0/3 Lot 3: 0/3 Lot 5: 0/3	Cut 1.0 LDO Cut 1.1 LDO Cut 1.3 LDO
EDR	JESD22-A117	100kcy EW @125°C then storage HTB 150°C - Duration 168H	1	77	77	Lot 4: 0/77	Cut1.3 LDO
EDR	JESD22-A117	100kcy EW @ -40°C then storage HTB 25°C - Duration 500H	1	74	74	Lot 4: 0/74	Cut 1.3 LDO
EDR	JESD22-A117	100kcy EW @ 125°C then storage HTB 150°C - Duration 1500H	1	77	77	Lot 5: ongoing	Cut 1.3 LDO in 2023 Sept.
EDR	JESD22-A117	100kcy EW @ 25°C then storage HTB 25°C - Duration 1500H	1	77	77	Lot 5: ongoing	Cut 1.3 LDO in 2023 Sept.
EDR	JESD22-A117	100kcy EW @ -40°C then storage HTB 25°C - Duration 1500H	1	77	77	Lot 5: ongoing	Cut 1.3 LDO in 2023 Sept.
ELFR	JESD22-A108 JESD74	Ta=125°C Duration= 48hrs 3V6	1	500	500	Lot 5: 0/500	Cut 1.3 LDO

ACCELERATED ENVIRONMENT STRESS TESTS

Table 9 – UFBGA 10x10 176+25L, ASE KH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	3	3	9	Lot 1: 0/3 Lot 3: 0/3 Lot 4: 0/3	Cut 1.0 LDO Cut 1.1 LDO Cut 1.3 LDO
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	2	308	616	Lot 1: 0/308 Lot 2: 0/308	Cut 1.0 LDO Cut 1.0 LDO
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	2	77	144	Lot 1: 0/77 Lot 2: 0/77	Cut 1.0 LDO Cut 1.0 LDO
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	2	77	144	Lot 1: 0/77 Lot 2: 0/77	Cut 1.0 LDO Cut 1.0 LDO
HTSL	JESD 22-A103	Ta=150°C, Duration= 500hrs ☒ After PC	2	77	144	Lot 1: 0/77 Lot 2: 0/77	Cut 1.0 LDO Cut 1.0 LDO
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	77	Lot 1: 0/77 Lot 2: 0/77	Cut 1.0 LDO Cut 1.0 LDO

Note: Test method revision reference is the one active at the date of reliability trial execution

Table 10 – LQFP 20x20 144L, ASE KH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	2	3	6	Lot 6: 0/3 Lot 7: 0/3	Cut 1.0 LDO Cut 1.1 LDO
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	2	308	616	Lot 6: 0/308 Lot 7: 0/308	Cut 1.0 LDO Cut 1.1 LDO
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	2	77	144	Lot 6: 0/77 Lot 7: 0/77	Cut 1.0 LDO Cut 1.1 LDO
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	2	77	144	Lot 6: 0/77 Lot 7: 0/77	Cut 1.0 LDO Cut 1.1 LDO
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	2	77	144	Lot 6: 0/77 Lot 7: ongoing	Cut 1.0 LDO Cut 1.1 LDO in 2023 August
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 Duration= 1000hrs ☒ After PC	2	77	144	Lot 6: 0/77 Lot 7: ongoing	Cut 1.0 LDO Cut 1.1 LDO in 2023 August

Note: Test method revision reference is the one active at the date of reliability trial execution

Table 11 – LQFP 14x14 100L, ASE KH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	1	3	3	Lot 8: 0/3	Cut 1.0 LDO
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	308	308	Lot 8: ongoing	Planned in 2023 July
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot 8: to be done	Planned in 2023 July
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot 8: to be done	Planned in 2023 July
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot 8: to be done	Planned in 2023 August
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	1	77	144	Lot 8: to be done	Planned in 2023 August

Note: Test method revision reference is the one active at the date of reliability trial execution

Table 12 – LQFP 10x10 64L, JSCC

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	1	3	3	Lot 9: 0/3	Cut 1.0 LDO
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	3	308	924	Lot 9: 0/308 Lot 10: 0/308 Lot 11: 0/308	Cut 1.0 LDO Cut 1.0 LDO Cut 1.0 LDO
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	3	77	231	Lot 9: 0/77 Lot 10: 0/77 Lot 11: 0/77	Cut 1.0 LDO Cut 1.0 LDO Cut 1.0 LDO
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ☒ After PC	3	77	231	Lot 9: 0/77 Lot 10: 0/77 Lot 11: 0/77	Cut 1.0 LDO Cut 1.0 LDO Cut 1.0 LDO
HTSL	JESD 22-A103	Ta=150°C, Duration= 500hrs ☒ After PC	3	77	231	Lot 9: 0/77 Lot 10: 0/77 Lot 11: 0/77	Cut 1.0 LDO Cut 1.0 LDO Cut 1.0 LDO
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 ☒ After PC	3	77	231	Lot 9: 0/77 Lot 10: 0/77 Lot 11: 0/77	Cut 1.0 LDO Cut 1.0 LDO Cut 1.0 LDO

Note: Test method revision reference is the one active at the date of reliability trial execution

Table 13 – PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including: . Wire bond shear . Wire bond pull	ST internal specifications	1 1 1	50 50 50	50 50 50	Lot 1: 0/50 Lot 6: 0/50 Lot 9: 0/50	UFBGA 176+25L LDO LQFP 144L LDO LQFP 64L LDO

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A117	Endurance and Data retention
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A101:	Temperature Humidity Bias

5 GLOSSARY

Reference	Short description
HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up
CA	Construction Analysis
MSL3	Moisture Sensitivity Level 3

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Philippe ADAM	Initial release	Division Q&R Responsible	Grenoble	Dominique GALIANO	9 – Dec – 2022
			Division Quality Manager	Rousset	Pascal NARCHE	15 – Dec – 2022
			BE Quality Manager	Rousset	Berengere ROUTIER-SCAPPUCCI	9 – Dec – 2022
2.0		Cut1.3 partial result	Division Q&R Responsible	Grenoble	Dominique GALIANO	13-Jun-2023
			Division Quality Manager	Rousset	Pascal NARCHE	13-Jun-2023
			BE Quality Manager	Rousset	Berengere ROUTIER-SCAPPUCCI	14-Jun-2023

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PRODUCT/PROCESS CHANGE NOTIFICATION
PCN13948 – Additional information

STM32H563xx - product enhancement

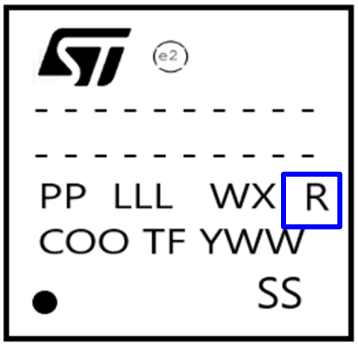
MDG – General Purpose Microcontrollers Division (GPM)

What are the changes?

Changes described in table below:

	Current condition	New condition
Front-End Diffusion site	ST Crolles 300 (France)	
STM32H563RIT6 **STM32H563VIT6** **STM32H563ZIT6**	Cut 1.1	Cut 1.3
Die revision Marking **R**	“Z”	“X”

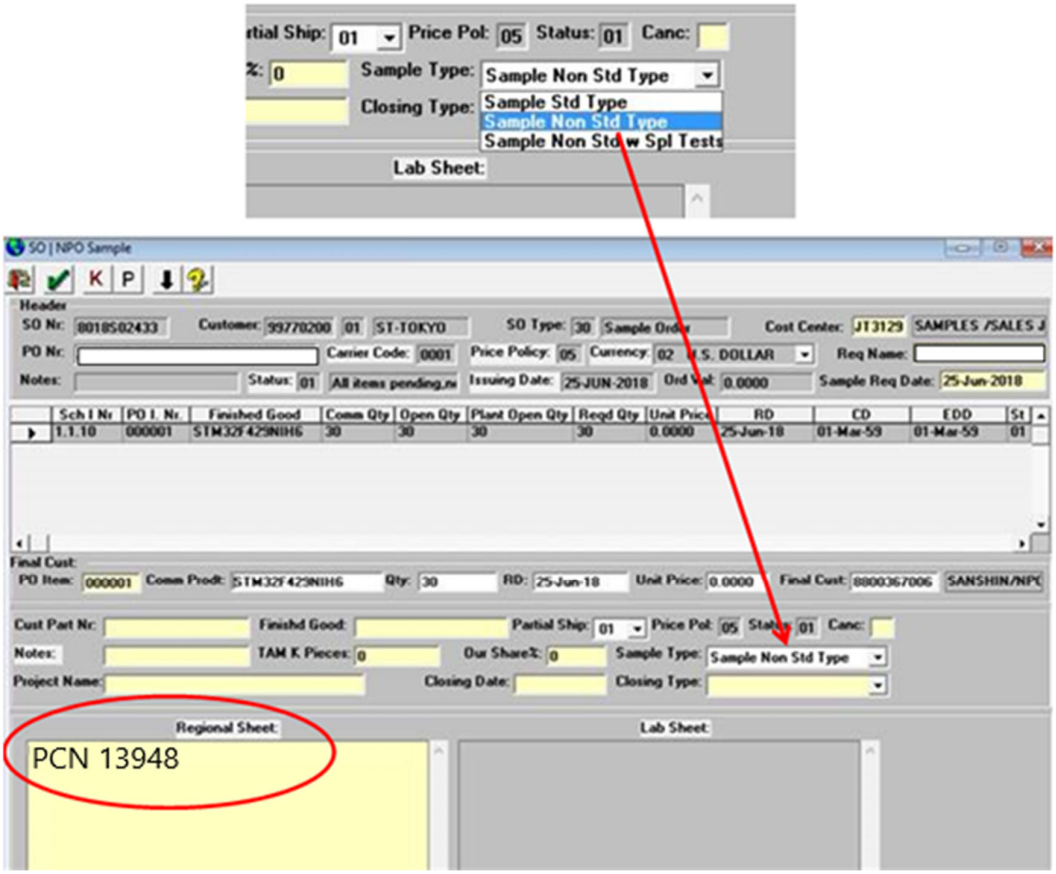
Example: Marking on package LQFP 100 14x14x1.4



How to order samples

For all samples request linked to this PCN, please:

- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "**PCN13948**" into the NPO Electronic Sheet/**Regional Sheet**
- request sample(s) through Notice tool, indicating a single Commercial Product for each request



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PCN Title : STM32H563x - product enhancement

PCN Reference : MDG/23/13948

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STM32H563IIK6	STM32H563VIT6	STM32H563ZIT6

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