PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	MDG/21/12623
1.3 Title of PCN	STM32WLxx products enhancement
1.4 Product Category	STM32WL 256K
1.5 Issue date	2021-07-16

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Ricardo Antonio DE SA EARP
2.1.2 Marketing Manager	Veronique BARLATIER
2.1.3 Quality Manager	Pascal NARCHE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Die redesign : Mask or mask set change with new die design like metallization (specifically chip frontside) or bug fix	TSMC Fab14 (Taiwan)

4. Description of change		
	Old	New
4.1 Description	STM32WLxxx Devices Cut 1.1 (Version Z) is in production with some limitations as documented in : STM32WL55xx, STM32WL54xx current version - ES0500 - Rev 2 - April 2021 (Errata Sheet) - DS13293 - Rev 1 - November 2020 (Datasheet) - RM0453 - Rev 1 - November 2020 (Reference Manual) STM32WLE5xx, STM32WLE4xx current version - ES0506 - Rev 2 - April 2021 (Errata Sheet) - DS13105 - Rev 8 - November 2020 (Datasheet) - RM0461 - Rev 3 - November 2020 (Reference Manual)	STM32WLxxx Cut 1.2 (Version Y) Devices introduces new features (long-packet) and feature enhancements as documented in : STM32WL55xx, STM32WL54xx new documentations - ES0500 - Rev 3 - June 2021 (Errata Sheet) - DS13293 - Rev 2 - June 2021 (Datasheet) - RM0453 - Rev 2 - June 2021 (Reference Manual) STM32WLE5xx, STM32WLE4xx new documentations - ES0506 - Rev 3 - June 2021 (Errata Sheet) - DS13105 - Rev 9 - June 2021 (Datasheet) - RM0461 - Rev 4 - June 2021 (Reference Manual)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	Impact on Function: improvements as indicated in documents listed. Remains fully compatible with existing Embedded Software	

5. Reason / motivation for change	
5.1 Motivation	STM32WL Cut 1.2 (Version Y) new feature introduction (long-packet) versus Cut 1.1 (version Z).
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Traceability ensure by ST internal tools. The die revision changes from "Z" to "Y" is displayed on Marking visible on top side of customer product package.

7. Timing / schedule	
7.1 Date of qualification results	2021-02-05

7.2 Intended start of delivery	2021-05-31
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	12623 MDG MCD RER1813 V1.3 STM32WL 256K Die 497XXXY Reliability Evaluation Report.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	**Issue Date**	2021-07-16

9. Attachments (additional documentations)
12623 Public product.pdf 12623 MDG MCD RER1813 V1.3 STM32WL 256K Die 497XXXY Reliability Evaluation Report.pdf 12623 PCN12623_Additional information.pdf

10. Affected parts		
10. 1 Current		**10.2 New (if applicable)**
10.1.1 Customer Part No	**10.1.2 Supplier Part No**	**10.1.2 Supplier Part No**
	STM32WL55CCU6	
	STM32WL55CCU7	
	STM32WL55JCI6	
	STM32WL55JCI7	
	STM32WLE5C8U6	
	STM32WLE5CBU6	
	STM32WLE5CCU6	
	STM32WLE5CCU7	
	STM32WLE5JBI6	
	STM32WLE5JCI6	
	STM32WLE4JCI6	
	STM32WLE5J8I6	
	STM32WLE5JCI6TR	

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Reliability Evaluation Report

MDG-MCD-RER1813

STM32WL5x/Ex (497x66)

Reliability Evaluation Purpose **(New Product Qualification)**

General Information	
Commercial Product	STM32WL54/L55/LE4/LE5
Product Line	497X66
Die revision	497XXXY (Cut1.2)
Product Description	STM32WL product family
Package	UFBGA 5X5X0.6 73L P 0.5 UFQFPN 7X7X0.55 48L P 0.5 WLCSP 59L DIE 497 P0.4
Silicon Technology	TSMC N90 eFLASH - 6M1U
Division	MDG-MCD
Reliability Maturity Level	20->W29

Traceability	
Diffusion Plant	TSMC Fab14, Taiwan.
Assembly Plant	ASE Taiwan JSCC, China. Amkor ATT1

Reliability Assessment	
Pass	☒
Fail	☐
Investigation required	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	17th Dec 2019	Patrick AUBERT	MDG-MCD-Q&R Engineer
1.1	14th Feb 2020	Patrick AUBERT	MDG-MCD-Q&R Engineer
1.2	15 Apr 2020	Patrick AUBERT	MDG-MCD-Q&R Engineer
1.3	5 Feb. 2021	Patrick AUBERT	MDG-MCD-Q&R Engineer

APPROVED BY:

VERSION 1.0

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	07th Jan 2020
Division Quality Manager	Rousset	Pascal NARCHE	09th Jan 2020

VERSION 1.1

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	14th Feb 2020

VERSION 1.2

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	15th Apr 2020

VERSION 1.3

Function	Location	Name	Date
Division Q&R Manager	Grenoble	Dominique GALIANO	5 Feb. 2021

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The aim of this report is to present results of the reliability evaluation performed on STM32GWL55/WL54/WLE5/WLE4 - Die 497XXXY.

Test vehicle is described here below:

Product	Process / Package	Diffusion / Assembly plant
STM32WL55JCI7	TSMC N90 eFLASH - 6M1U / UFBGA 5X5X0.6 73L P 0.5 UFQFPN48 7x7 48L P0.5	TSMC Fab14 / ASE JSCC

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

1.2 Reliability Strategy

The STM32GWL55/WL54/WLE5/WLE4 - Die 497XXXY, is processed in the 90ULL process from TSMC Fab14 Taiwan plant which is qualified through STM32L4x- 1M - Die 415 (RERMCD1112) and with STM32BLE Die 495 (RERMCD1613) for RF options for our division

Package	Reference	Assy Plant location
UFBGA 5X5X0.6 73L P 0.5 MM|B08E	MCD-RER1901	ASE Taiwan

According to "RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION" specification (DMS 0061692), the following qualification strategy has been defined to assess the die in BGA73 package.

- Die Qualification:
  - Cut 1.0:
    - 1 full qualification lot to assess the die in BGA73 package.
    - 1 full qualification lot to assess the SMPS IP in QFN48 package.
  - Cut 1.1:
    - ESD/LU Trial
    - Flash cycling & retention Trials
    - HTOL 168H

    Note: For all Cuts, ESD HBM & LU is done in BGA73 (Max pin count)
  - Cut 1.2:
    - ESD/LU Trial
    - HTOL 168H

- Package Qualification:
  The reliability test plan and result summary are presented in the following tables:

Package	Body	Pitch	Package Code	Wire	Assembly	Bonding Option	Trial
UFBGA73	5x5	0.5	B08E	Gold	ASE		1 reliability lot
UFQFPN48	7X7	0.5	A0B9	Gold	JSCC		1 reliability lot
WLCSP 59		0.4	B058		ATT		1 reliability lot

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for the STM32GWL55/WL54/WLE5/WLE4 - Die 497XXXY in BGA73 package and UQFPN48 package.

Report will be updated when new reliability results will be available with other packages

Refer to Section 3.0 for reliability test results.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1 Generalities

2.1.1 Main features

- Dual Core (M4 @ 48MHz MO+ @ 48MHz)
- 256KB Flash, 64KB RAM (2x32KB)
- 2xSPI,3xI2C,2xUSART,SPI
- RTC V3.0 / AWU/CSS
- Radio Mod LoRa@,FSK,2(G)FSK,GMSK,MSK
- PCROP + AES 256Kbit + Secure Key storage + PKA
- 3xULP 16bit timer , 1xULP 32bit timer
- Radio IP & SMPS LoRaIP
- 1.8V to 3.6V voltage range(DC/DC,LDO)
- -40°C to +105°C temperature range without radio
- -40°C to +85°C temperature range with the radio

For additional information concerning the product behavior, refer to STM32WL5x/Ex datasheets.

2.2 Traceability

2.2.1 Wafer fab information

Table 1

<table>
<tr><th colspan="2">Wafer fab information</th></tr>
<tr><td>Wafer fab name / location</td><td>TSMC Fab14 / Taiwan</td></tr>
<tr><td>Wafer diameter (inches)</td><td>12</td></tr>
<tr><td>Wafer thickness (µm)</td><td>775 +/- 25</td></tr>
<tr><td>Silicon process technology</td><td>N90_eFLASH_6M1T_DNW_HVT_VTNC_ESD_ULL_RDL</td></tr>
<tr><td>Number of masks</td><td>47</td></tr>
<tr><td>Die finishing front side (passivation) materials/thicknesses (µm)</td><td>USG + NITRIDE / 1.75µm</td></tr>
<tr><td>Die area (Stepping die size) (µm)</td><td>3697 x 3543</td></tr>
<tr><td>Die pad size (X,Y) (µm)</td><td>59 x 123</td></tr>
<tr><td>Sawing street width (X,Y) (µm)</td><td>80</td></tr>
<tr><td>Metal levels/Materials/Thicknesses (µm)</td><td>
<table>
<tr><th>Layer</th><th>composition</th><th>Thickness</th></tr>
<tr><td>Metal 1</td><td>TaN/Ta/CuSeed/Cu</td><td>0.24</td></tr>
<tr><td>Metal 2</td><td>TaN/Ta/CuSeed/Cu</td><td>0.31</td></tr>
<tr><td>Metal 3</td><td>TaN/Ta/CuSeed/Cu</td><td>0.31</td></tr>
<tr><td>Metal 4</td><td>TaN/Ta/CuSeed/Cu</td><td>0.31</td></tr>
<tr><td>Metal 5</td><td>TaN/Ta/CuSeed/Cu</td><td>0.31</td></tr>
<tr><td>Metal 6</td><td>TaN/Ta/CuSeed/Cu</td><td>3.4</td></tr>
<tr><td>Metal 7</td><td>AlCu</td><td>1.45</td></tr>
</table>
</td></tr>
<tr><td>Die over coating (material/thickness)</td><td>No</td></tr>
</table>

FIT level	2.2 FITs at qualification date
Soft Error Rate - Alpha SER [FIT/Mb] - Neutron SER [FIT/Mb] - Conditions	Alpha SER: 491 FIT/Mb Neutron SER: 445 FIT/Mb Neutron SER is an estimation at sea level of NYC (14n/h/cm²). Alpha result is estimated using a nominal flux of 0.001α/h/cm²
Wafer Level Reliability - Electro-Migration (EM) - Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) - Hot Carrier Injection (HCI) - Negative Bias Thermal Instability (NBTI) - Stress Migration (SM)	Yes
Other Device(s) using same process	STM32L4 family and STM32WB family for RF option

2.2.2 Assembly information

Table 2

UFBGA 5X5X0.6 73L P 0.5 MM|B08E	
Assembly plant name / location	ASE TAIWAN
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	75 +/- 10
Die sawing method	Laser Grooving + step cut
Bill of Material elements	
Lead Frame material /supplier/reference	SUBSTRATE UFBGA 5x5 73L P0.5 ASE A26559
Die attach material/type(glue/film)/supplier	D/A Tape ABLESTICK ATB-125
Wire bonding material/diameter/supplier	wire gold 2N 0.8 mils
Balls metallurgy/diameter/supplier	SOLDER BALLS WITH 200 DIAM SN96.5 AG3.5%
Molding compound material/supplier/reference	Resin KYOCERA G1250AAS ULA
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3
UFQFPN 7X7X0.55 48L 0.5 MM PITCH|A0B9	
Assembly plant name / location	JSCC
Pitch (mm)	0.5
Die thickness after back-grinding (µm)	150 +/- 25
Die sawing method	Laser Grooving + step cut
Bill of Material elements	
Lead Frame material /supplier/reference	LF FOR UQFN 7x7 48L Sn PAD 5.2 MM SQ Groove
Die attach material/type(glue/film)/supplier	Glue Hitachi EN4900GC
Wire bonding material/diameter/supplier	0.8mils 3N Gold wire
Molding compound material/supplier/reference	RESIN SUMITOMO G770
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL 3

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	ST RSST in Rousset

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
1	P62F70 Wafer#17	1.0	AA923001	X0JB*497ESXA	BGA73	Die & Package Reliability assessment
2	P62F70 Wafer#16	1.0	GQ92325R	71MI*497ESXA	QFN48	Die SMPS Reliability assessment
3	P62X38 Wafer#1	1.1	AA937080	X2JB*497ESXZ	BGA73	Die Reliability assessment
4	P62X38 Wafer#16	1.1	GQ94221M	71MI*497ESXZ	QFN48	Package Reliability assessment
5	P64T44 Wafer#7	1.2	AA045011	X0JB*497ESXY	BGA73	Die Reliability assessment

3.2 Test plan and results summary

Table 5 - ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A=Not Applicable)
HTOL	JESD22 A108	Ta=125°C Duration= 1200H	1	77	77	Lot1: 0/77	
HTOL	JESD22 A108	Ta=125°C Duration= 168H	1	77	77	Lot3: 0/77	
HTOL	JESD22 A108	Ta=125°C Duration= 168H	1	77	77	Lot5: 0/77	
HTOL	JESD22 A108	Ta=125°C Duration= 1200H	1	77	77	Lot2: 0/77	SMPS IP trials
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF 2kV class2	3	3	9	Lot1: 0/3 Lot3: 0/3 Lot5: 0/3	
Latch Up	JESD78	105°C	3	3	9	Lot1: 0/3 Lot3: 0/3 Lot5: 0/3	
EDR	JESD22-A117	10kcy EW @ 125°C then Storage HTB 150°C - Duration 1500H	1	77	77	Lot1: 0/77	
EDR	JESD22-A117	10kcy EW @ 125°C then Storage HTB 150°C - Duration 168H	1	77	77	Lot3: 0/77	
EDR	JESD22-A117	10kcy EW @ 25°C then Storage HTB 150°C - Duration 168h	2	77	154	Lot1: 0/77 Lot3: 0/77	
EDR	JESD22-A117	10kcy EW @ -40°C then Storage HTB 150°C - Duration 168H	2	77	154	Lot1: 0/77 Lot3: 0/77	
ELFR	JESD22-A108 JESD74	Ta=125°C Duration= 48hrs	1	500	500	Lot1: 0/500	
ELFR	JESD22-A108 JESD74	Ta=125°C Duration= 48hrs	1	500	500	Lot2: 0/500	SMPS IP trials

Table 6 - ACCELERATED ENVIRONMENT STRESS TESTS
For UFBGA 5X5 73L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	3	3	9	Lot1: 0/3 Lot3: 0/3 Lot5: 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	231	231	Lot1: 0/231	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot1: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot1: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH Duration= 1000hrs VDD=3v6 ☒ After PC	1	77	77	Lot1: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution

For UFQFPN 48L

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	500V	1	3	3	Lot4 0/3	
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	1	231	231	Lot4: 0/308	
UHAST	JESD22-A118	Ta=130°C / 85% RH Duration= 96hrs ☒ After PC	1	77	77	Lot4: 0/77	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	1	77	77	Lot4: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ☒ After PC	1	77	77	Lot4: 0/77	
THB	JESD 22-A101	Ta=85°C/85%RH Duration= 1000hrs VDD=3v6 ☒ After PC	1	77	77	Lot4: 0/77	

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A110:	Temperature Humidity Bake
JESD 22B102:	Solderability test
JESD22B100/B108:	Physical dimension

5 GLOSSARY

Reference	Short description
HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HAST	Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up
CA	Construction Analysis

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Patrick AUBERT	Initial Release	Div. Quality Manager	Rousset	Pascal NARCHE	9th January 2020
			Q&R Quality Manager	Grenoble	Dominique GALIANO	7th January 2020
1.1	Patrick AUBERT	Cut 1.1 results	Q&R Quality Manager	Grenoble	Dominique GALIANO	13th March 2020
1.2	Patrick AUBERT	QFN48 Pack. results	Q&R Quality Manager	Grenoble	Dominique GALIANO	15th April 2020
1.3	Patrick AUBERT	Cut 1.2 results	Q&R Quality Manager	Grenoble	Dominique GALIANO	5th Feb. 2021

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PRODUCT/PROCESS CHANGE NOTIFICATION
PCN12623– Additional information

STM32WL 256K product enhancement

MDG - Microcontrollers Division (MCD)

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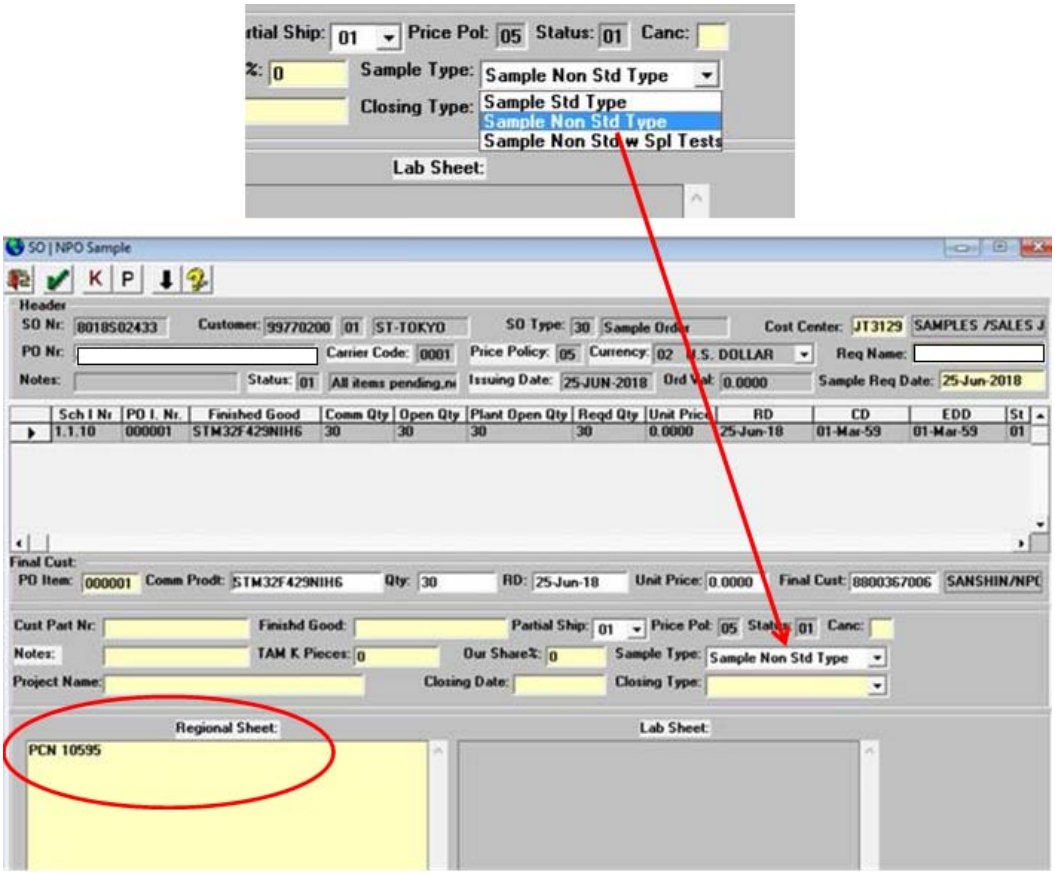
- insert the PCN number "**PCN12623**" into the NPO Electronic Sheet/**Regional Sheet**
- request sample(s) through Notice tool, indicating a single Commercial Product for each request



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PCN Title : STM32WLxx products enhancement

PCN Reference : MDG/21/12623

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STM32WLE5JCI6TR	STM32WL55CCU7	STM32WL55JCI7
STM32WLE5J8I6	STM32WL55CCU6	STM32WLE5CCU6
STM32WLE4CCU6	STM32WLE5C8U6	STM32WLE5CCU7
STM32WLE5JCI6	STM32WL54JCI6	STM32WL55JCI6
STM32WLE5JBI6	STM32WLE4JCI6	STM32WLE5CBU6
STM32WL54CCU6		

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