

PRODUCT / PROCESS CHANGE NOTIFICATION	
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1. PCN basic data	
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1.1 Company		STMicroelectronics International N.V
1.2 PCN No.		MDG/21/12540
1.3 Title of PCN		Amkor ATP (Philippines) TSSOP20 package additional line for STM32G listed products
1.4 Product Category		STM32G03 64K in TSSOP20 package
1.5 Issue date		2021-04-26

2. PCN Team	
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2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Ricardo Antonio DE SA EARP
2.2.2 Marketing Manager	Veronique BARLATIER
2.2.3 Quality Manager	Pascal NARCHE

3. Change		
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3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	AMKOR ATP (Philippines)

4. Description of change		
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	Old	New
4.1 Description	Back-End Source: - ST Shenzhen (China)	Back-End Source: - ST Shenzhen (China) - AMKOR ATP (Philippines) Added
4.2 Anticipated Impact on form, fit, function, quality, reliability or processability?	Lead color and surface finish will change due to different leadframe finishing. Pin1 identifier might change in terms of form and positioning. Package darkness changes depending on molding.	

5. Reason / motivation for change	
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5.1 Motivation	To sustain MCD microcontrollers success in the market, ST Microcontrollers Division must convert the line to maintain state of the art service level to our customers
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change	
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6.1 Description	Second level interconnect changes from e4 to e3. Tracability ensured by ST internal Tools.
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7. Timing / schedule	
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7.1 Date of qualification results	2021-04-08
7.2 Intended start of delivery	2021-05-14
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation	
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8.1 Description	12540 MDG-MCD-RER1712 V3.0 - PCN10233-PCN12540-ATP1 TSSOP20 XDLF for additional source - reliability evaluation report.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-04-26

**9. Attachments (additional documentations)**

12540 Public product.pdf

12540 MDG-MCD-RER1712 V3.0 - PCN10233-PCN12540-ATP1 TSSOP20 XDLF for additional source - reliability evaluation report.pdf

12540 PCN12540 \_Additional information.pdf

**10. Affected parts**

<b>10. 1 Current</b>		<b>10.2 New (if applicable)</b>
<b>10.1.1 Customer Part No</b>	<b>10.1.2 Supplier Part No</b>	<b>10.1.2 Supplier Part No</b>
	STM32G030F6P6	
	STM32G030F6P6TR	
	STM32G031F4P3	
	STM32G031F4P6	
	STM32G031F6P6	
	STM32G031F8P6	
	STM32G041F8P6	

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# Reliability Evaluation Report

## MDG MCD 1712

*STM32F030, STM8AF6223, STM8L051,*

*STM32G051, STM8S003*

**ATP1 TSSOP20 XDLF for additional source / PCN10233/PCN12540**

General Information		Traceability	
<b>Commercial Product :</b>	STM32F030F4P6 STM8AF6223PDU STM8L051F3P6 STM32G051F8P6 STM8S003F3P6		
<b>Product Line :</b>	758X19 79JX19 444X66 456X66 767X19		<b>Assembly Plant :</b> Amkor ATP1 Philippines
<b>Die revision :</b>	758XXXZ 79JX10A 444XXX1 456ESXA 767ESX7		
<b>Product Description :</b>	STM8 / STM32	Reliability Assessment	
<b>Package :</b>	TSSOP20	Pass	<input checked="" type="checkbox"/>
<b>Silicon Technology :</b>	CMOSF9G01 CMOSF9G02 TSMC0.18 TSMC90nm	Fail	<input type="checkbox"/>
<b>Division :</b>	MDG-MCD		

**Note:** this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).

Version	Date	Author	Function
1.0	25th-Mar-2019	Cédric CHASTANG	MDG-MCD-Q&R BE Engineer
2.0	09th-Dec-2019	Cédric CHASTANG	MDG-MCD-Q&R BE Engineer
3.0	07th-Apr-2021	Gabin BOSCO	MDG-MCD-Q&R BE Engineer

**APPROVED BY:**

Function	Location	Name	Date
Division Quality Manager	ST Rousset	Pascal NARCHE	25th-Mar-2019
Division Back-End Quality Manager	ST Rousset	Gisele SEUBE	25th-Mar-2019
Division Quality Manager	ST Rousset	Pascal NARCHE	09th-Dec-2019
Division Back-End Quality Manager	ST Rousset	Gisele SEUBE	09th-Dec-2019
Division Quality Manager	ST Rousset	Pascal NARCHE	07th-Apr-2021

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## 1 RELIABILITY EVALUATION OVERVIEW

### 1.1 Objective

Due to the success on the market of STM8L & STM32 devices, ST Microcontrollers Division decided to qualify an additional back-end line for TSSOP20 in XDLF at ATP1.

Test vehicles are selected by Change Review Board based on key parameters such as Front-end technologies and volumes allowing to qualify the entire product families in TSSOP20 XDLF at AMKOR ATP1.

Test vehicle is described here below:

Product	Process or Package	Diffusion or Assembly plant
STM32F030F4P6	TSSOP20	SC AMKOR ATP1
STM8AF6223PDU		
STM8L051F3P6		
STM32G051F8P6		
STM8S003F3P6		

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard.

### 1.2 Reliability Strategy

This reliability evaluation concerns the qualification of CMOSF9S, CMOSF9, TSMC0.18 and TSMC90nm Technologies.

Similarity strategy will be applied to cover all combinations of Diffusion Plant, Diffusion Process and TSSOP packages listed below:

- TSMC 0.18µm / TSMC 90nm/ Rousset R8 F9GO2 / Rousset R8 & SG8E Singapore F9GO1 diffusion process.
- Full similarity is applicable on STM8L devices in CMOS F9 GO2 diffusion process as using same passivation and pad structure than STM8S in CMOS F9 GO1 diffusion process.

CMOSF9S, CMOSF9 and TSMC0.18 Technology change HDLF to XDLF in ATP1 was done under Process Change Notification PCN10233.

PCN10233: Changes are described here below:

	Previous	New
Back-end site	Amkor TP (Philippines)	Amkor ATP (Philippines)
Leadframe (1)	Pre-plated Frame (PPF), High Density Leadframe (HDLF)	Tin Post-plated Frame, Extreme Density Leadframe (XDLF)
Molding compound (2)	Sumitomo EME-G700K	Sumitomo EME-G700LS
Second level interconnect	e4	e3
Enhanced traceability in marking	No digit	2 digits added

TSMC 90nm Technology assembly change from ST Shenzhen to ATP1 was done under Process Change Notification PCN12540.

PCN12540: Changes are described here below:

	Current back-end lines	New back-end line
<b>Assembly site</b>	ST Shenzhen (China)	AMKOR ATP (Philippines)
<b>Leadframe (1)</b>	Pre-Plated Frame (PPF) High Density Leadframe (HDLF)	Tin Post-plated Frame, Extreme Density Leadframe (XDLF)
<b>Die Attach</b>	ABLESTIK 8601S-25	ABLESTIK 8290
<b>Molding compound (2)</b>	Sumitomo EME-G700KC	Sumitomo EME-G700LS
<b>Bonding Wire</b>	Ag 96.5% 0.8mil	Au 0.8mil
<b>Second level interconnect</b>	e4	e3

(1) Lead color and surface finish change depending on leadfinishing.

(2) Package darkness changes depending on molding compound.

Pin1 identifier can change in terms of form and positioning.

Marking position and size could be different upon assembly site, without any loss of information.

*SG8E GO1 diffusion technology change from ST Rousset 8 to ST Singapore SG8E was done under Process change notification PCN10630/ PCN10941/ PCN11442.*

### 1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification for CMOSF9GO1 RSST, CMOSF9GO2 RSST, TSMC0.18 and TSMC90nm is granted for new XDLF Back-end line for TSSOP20 at Amkor ATP. The qualification for CMOSF9GO1 SG8E is planned to be granted for July2021.

Refer to Section 3.0 for reliability test results.

## 2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

### 2.1 Generalities

Package line	Assembly Line Package	Device (Partial RawLine Code)	Diffusion Process	Number of Lots
TSSOP20	ATP1	STM8(YA*79J)	CMOSF9GO1	2
		STM8(YA*767)		
		STM32(YA*758)	CMOSF9GO2	1
		STM8(YA*444)	TSMC0.18	1
		STM32(YA*456)	TSMC90nm	1

### 2.2 Traceability

#### 2.2.1 Wafer fab information

Table 1

FAB1	Die 758	Die 79J	Die 767
Wafer fab name / location	RS8F-Rousset	RS8F-Rousset	SG8E-ST
Wafer diameter (inches)	8 inches		
Wafer thickness (µm)	375±25 µm		
Silicon process technology	CMOSF9GO2	CMOSF9GO1	
Number of masks	39	29	
Die finishing front side (passivation) materials/thicknesses	USG + NitUV (HFP USG+UV Nitride)		
Die finishing back side Materials/thicknesses	RAW SILICON – BACK GRINDING		
Die area (Stepping die size)	1562 x 2238 µm 3,5mm <sup>2</sup>	1334 x 2210 µm 2,94mm <sup>2</sup>	
Die pad size	65x108 µm		
Sawing street width (X,Y) (µm)	80 x 80 µm		
Metal levels/Materials/Thicknesses	Metal 1 TaN/Ta/Cu 0.280µm Metal 2 TaN/Ta/Cu 0.350µm Metal 3 TaN/Ta/Cu 0.350µm Metal 4 TaN/Ta/Cu 0.350µm Metal 5 Ti/AlCu/TxTN 0.900µm	Metal 1 TaN/Ta/Cu 0.280µm Metal 2 TaN/Ta/Cu 0.350µm Metal 3 TaN/Ta/Cu 0.350µm Metal 4 Ti/AlCu/TxTN 0.900µm	

FAB1	Die 456	Die 444
Wafer fab name / location	T14F – TSMC	TS8F – TSMC
Wafer diameter (inches)	12 inches	8 inches
Wafer thickness (µm)	775±25 µm	381±25 µm
Silicon process technology	TSMC90	TSMC0.18
Number of masks	45	33
Die finishing front side (passivation) materials/thicknesses	USG + NITRIDE	HDPox 10kA+SRO 1.5kA+PESIN 6kA
Die finishing back side Materials/thicknesses	RAW SILICON – BACK GRINDING	
Die area (Stepping die size)	1967 x 2422 µm 4,76mm <sup>2</sup>	2458 x 2360 µm 5,8mm <sup>2</sup>
Die pad size	65x59µm	65,70 µm
Sawing street width (X,Y) (µm)	80 x 80 µm	
Metal levels/Materials/Thicknesses	Metal 1 TaN/Ta/CuSeed/Cu 0.240µm Metal 2 TaN/Ta/CuSeed/Cu 0.310µm Metal 3 TaN/Ta/CuSeed/Cu 0.310µm Metal 4 TaN/Ta/CuSeed/Cu 0.310µm Metal 5 TaN/Ta/CuSeed/Cu 0.310µm Metal 6 TaN/Ta/CuSeed/Cu 0.850µm Metal 7 AlCu 1.450µm	Metal 1 Tin/AlCu/Tin 0.450µm Metal 2 Tin/AlCu/Tin 0.450µm Metal 3 Tin/AlCu/Tin 0.450µm Metal 4 Tin/AlCu/Tin 0.450µm Metal 5 Tin/AlCu/Tin 0.875µm

## 2.2.2 Assembly information

**Table 2**

Assembly Information		
Package 1 – TSSOP20		
Die	758 & 79J & 444 & 767	456
Assembly plant name / location	AMKOR TECNOLOGY PHILIPPINES, INC (ATP1) KM 22 East Service Road Cupang, Muntinlupa City 1771 Philippines	
Pitch (mm)	0,65	
Die thickness after back-grinding (µm)	275µm +/- 25	
Die sawing method	Step cut	Laser groove + Single cut
Lead frame/Substrate material	Rough Copper Frame	
Lead frame finishing (material/thickness)	Pure tin / 7 to 20µm	
Die attach material/type(glue/film)/supplier	GLUE D/A 8290 / ABLESTIK	
Wire bonding material/diameter/supplier	GOLD WIRE 0.8MIL	
Molding compound material/supplier/reference	Resin Sumitomo / EMEG700LS	
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL1	

## 2.2.3 Reliability testing information

**Table 3**

Reliability Testing Information	
Reliability laboratory name / location	ST GRAL in GRENOBLE ST RSST in ROUSSET ATP1 in PHILIPPINES

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.

ST certification document can be downloaded under the following link:

[http://www.st.com/content/st\\_com/en/support/quality-and-reliability/certifications.html](http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html)

## 3 TESTS RESULTS SUMMARY

### 3.1 Lot Information

**Table 4**

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package
1	758	Z	7B835496	43YA*758XXXZ	TSSOP20
2	444	1	7B835632	46YA*444XXX1	TSSOP20
3	79J	A	7B835579	43YA*79JX10A	TSSOP20
4	456	A	7B043542	40YA*456ESXA	TSSOP20
5	767	To be defined	To be defined	45YA*767ESX7	TSSOP20

### 3.2 Test plan and results summary

**Table 5 – ACCELERATED ENVIRONMENT STRESS TESTS**

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C , MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	5	308	1540	Lot1: 0/308 Lot2: 0/308 Lot3: 0/308 Lot 4: 0/308 Lot 5: July21	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc / 1000cyc (monitoring)  <input checked="" type="checkbox"/> After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: July21	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs  <input checked="" type="checkbox"/> After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: July21	
HTSL	JESD 22-A103	Ta=150°C , Duration= 500hrs & 1000hrs  <input checked="" type="checkbox"/> After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: July21	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 Duration : 1000hrs  <input checked="" type="checkbox"/> After PC	5	77	385	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77 Lot 4: 0/77 Lot 5: July21	

**Table 7 – ELECTRICAL VERIFICATION TESTS**

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	JESD22-C101 ANSI/ESD STM5.3.1	500V	5	3	15	Lot 1: 0/3 Lot 2: 0/3 Lot 3: 0/3 Lot 4: 0/3 Lot 5: July21	

Note: Test method revision reference is the one active at the date of reliability trial execution

**Table 8 – PACKAGE ASSEMBLY INTEGRITY TESTS**

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
CA	Construction Analysis including –Wire bond shear –Wire bond pull –Solderability	JESD 22B102 JESDB100/ B108	5	50	250	Lot 1: No concern Lot 2: No concern Lot 3: No concern Lot 4: No concern Lot 5: July21	N/A

#### 4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
DMS 0061692	Reliability Tests and Criteria for Product Qualification
JESD47	Stress–Test–Driven Qualification of Integrated Circuits
JESD22–A101	Temperature Humidity Bias
JESD22–A104:	Temperature cycling
JESD22–A110:	Temperature Humidity Bake
JESD22–A113	Preconditioning of non–hermetic surface mount devices prior to reliability testing
JESD 22B102:	Solderability test
JESD22B100/B108:	Physical dimension
JESD22–A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD 22–A103	High Temperature Storage Life
JESD22–C101	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
ANSI/ESD STM5.3.1	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
J–STD–020	Moisture/reflow sensitivity classification for non–hermetic solid state surface mount devices
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP 2.6.19	Process maturity level

#### 5 GLOSSARY

Reference	Short description
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD CDM	Electrostatic discharge (charge device model)
CA	Construction Analysis

## 6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Cédric CHASTANG	Initial Release	Div. Quality Manager	ST Rousset	Pascal NARCHE	25th-Mar-2019
			Div. Back-End Quality Manager	ST Rousset	Gisèle SEUBE	25th-Mar-2019

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
2.0	Cédric CHASTANG	Update results THB 1000h Lot 3	Div. Quality Manager	ST Rousset	Pascal NARCHE	09th-Dec-2019
			Div. Back-End Quality Manager	ST Rousset	Gisèle SEUBE	09th-Dec-2019

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
3.0	Gabin Bosco	Update lot4 and lot5	Div. Quality Manager	ST Rousset	Pascal NARCHE	07th-Apr-2021

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**PRODUCT/PROCESS  
CHANGE NOTIFICATION  
PCN12540– Additional information**

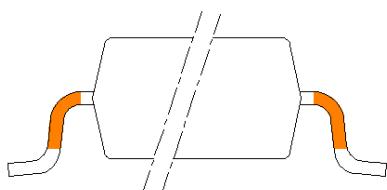
**Amkor ATP (Philippines) TSSOP20 package additional line  
for STM32G listed products**

**MDG - Microcontrollers Division (MCD)**

**What is the change?**

	Current back-end lines	New back-end line
Assembly site	ST Shenzhen (China)	AMKOR ATP (Philippines)
Leadframe (1)	Pre-Plated Frame (PPF) High Density Leadframe (HDLF)	Tin Post-plated Frame, Extreme Density Leadframe (XDLF)
Die Attach	ABLESTIK 8601S-25	ABLESTIK 8290
Molding compound (2)	Sumitomo EME-G700KC	Sumitomo EME-G700LS
Bonding Wire	Ag 96.5%, 0.8mil	Au, 0.8mil
Second level interconnect	e4	e3

**(1)** Lead color and surface finish change depending on leadfinishing.



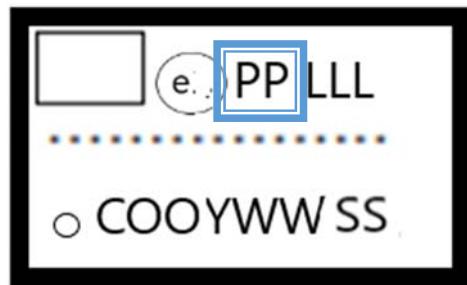
**(2)** Package darkness changes depending on molding compound.

Pin1 identifier can change in terms of form and positioning.

Marking position and size could be different upon assembly site, without any loss of information.

## How can the change be seen?

Marking example:



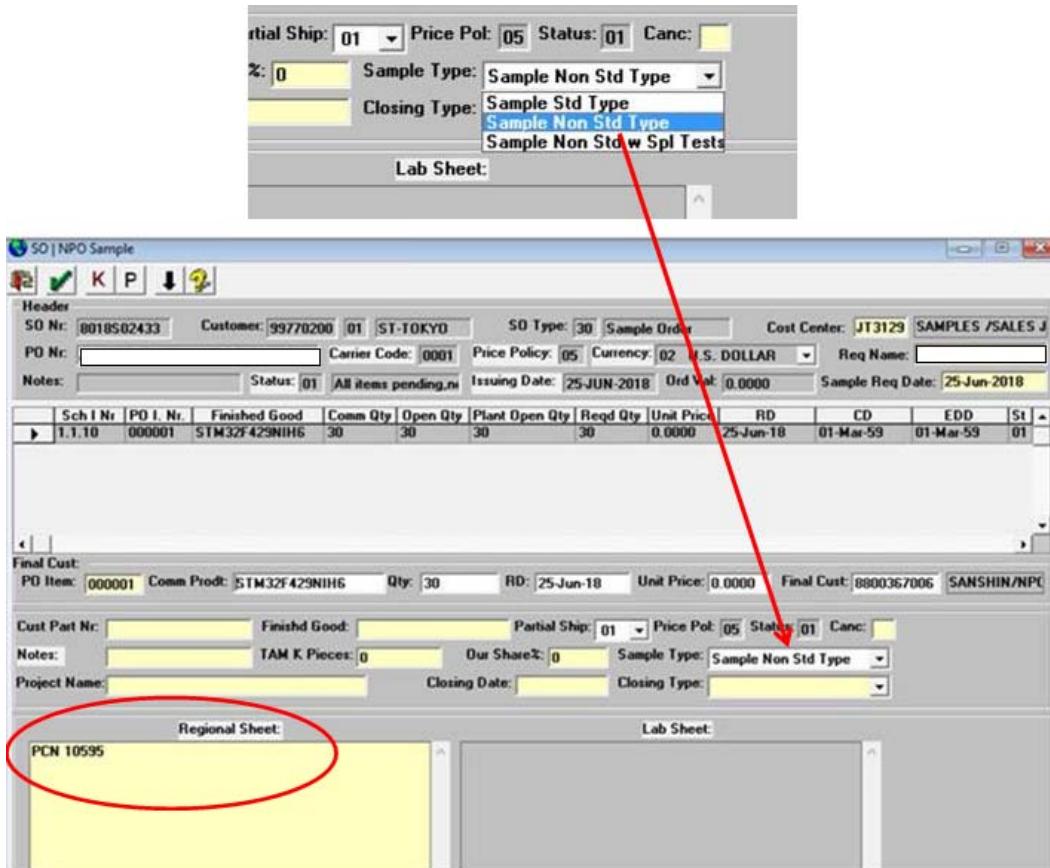
Where **PP** code indicates the Assembly traceability plant code.

PP code	Assembly Line - Fab
GK	ST Shenzhen (China)
7B	AMKOR ATP (Philippines)

## How to order samples?

For all samples request linked to this PCN, please:

- place a **Non-standard** sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number “**PCN12540**” into the NPO Electronic Sheet/**Regional Sheet**
- request sample(s) through Notice tool, indicating a single Commercial Product for each request



SO | NPO Sample

Header

SO Nr: 0018502433 Customer: 99770200 01 ST-TOKYO SO Type: 30 Sample Order Cost Center: JT3129 SAMPLES /SALES J

PO Nr: Carrier Code: 0001 Price Policy: 05 Currency: 02 U.S. DOLLAR Req Name:

Notes: Status: 01 All items pending,ni Issuing Date: 25-JUN-2018 Ord Val: 0.0000 Sample Req Date: 25-Jun-2018

Sch I Nr	PO I. Nr.	Finished Good	Comm Qty	Open Qty	Plant Open Qty	Reqd Qty	Unit Price	RD	CD	EDD	St
1.1.10	000001	STM32F429NIH6	30	30	30	30	0.0000	25-Jun-18	01-Mar-59	01-Mar-59	01

Final Cust:

PO Item: 000001 Comm Prod: STM32F429NIH6 Qty: 30 RD: 25-Jun-18 Unit Price: 0.0000 Final Cust: 8800367006 SANSIN/NPC

Cust Part Nr: Finished Good: Partial Ship: 01 Price Pol: 05 Status: 01 Canc:

Notes: TAM K Pieces: 0 Our Share%: 0 Sample Type: Sample Non Std Type

Project Name: Closing Date: Closing Type:

Regional Sheet: **PCN 10595**

Lab Sheet:



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**PCN Reference :** MDG/21/12540

**Subject :** Public Products List

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