PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	DIGITAL ICS AND RF/24/14588
1.3 Title of PCN	TESEO-VIC3DA, TESEO-VIC3D: Bill of Material Optimization
1.4 Product Category	TESEO-VIC3DA, TESEO-VIC3DATR, TESEO-VIC3D, TESEO-VIC3DTR
1.5 Issue date	2024-09-02

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Lorenzo MOIOLI
2.1.2 Marketing Manager	Gianvito GIUFFRIDA
2.1.3 Quality Manager	Alberto MERVIC

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Materials	(Not Defined)	Subcon ASE - Korea

4. Description of change		
	Old	New
4.1 Description	LDO LD39020DTPU18R MEMS ASM330LHH Diode ESD7501MUT5G	LDO STLQ020J18R + additional resistor MEMS SM330LHHX Diode ESD7501MUT5G and ESDAXLC6-1BU2 (second source) PCB fix (see details)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change	
5.1 Motivation	Product Optimization
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change	
6.1 Description	Dedicated Finished Good Codes

7. Timing / schedule	
7.1 Date of qualification results	2024-08-07
7.2 Intended start of delivery	2025-02-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	14588 RR-2024-02-0050-DP - Teseo VIC3D_DA - VB8Z_New_LDO+PCB_fix_Reliability_Report - Rev2.0.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2024-09-02

9. Attachments (additional documentations)

14588 Public product.pdf
14588 Details.pdf
14588 RR-2024-02-0050-DP - Teseo VIC3D_DA - VB8Z_New_LDO+PCB_fix_Reliability_Report - Rev2.0.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	TESEO-VIC3D	
	TESEO-VIC3DA	

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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : TESEO-VIC3DA, TESEO-VIC3D: Bill of Material Optimization

PCN Reference : DIGITAL ICS AND RF/24/14588

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

TESEO-VIC3DA	TESEO-VIC3D	TESEO-VIC3DATR
TESEO-VIC3DTR		

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Product/process change notification:

TESEO-VIC3DA, TESEO-VIC3D: Bill of Material Optimization

ADG/24/14588

Product family	Technology	Package
TESEO-VIC3DA, TESEO-VIC3DATR, TESEO-VIC3D, TESEO-VIC3DTR		LCC 24 Pins

(optional)

Description of the change
TESEO Module optimization with new Bill Of Material. See below details

Reason
Product Optimization

Date of implementation
January 2025

Samples Availability
November 2024

Impact of the change	
Form	No Impact
Fit	Tollerance bottom leads As-Is from 0.1mm to 0.125mm
Function	No Impact
Reliability	No Impact
Processibility	No Impact

Qualification of the change
Qualification according to AEC-Q100 See below details.

Qualification strategy
Teseo GNSS Module – VIC3DA new BOM

ADG Q&R – Automotive Digital Group

M. Arani, D.Pop, E. Mariani

Wk 08 2024

Rev. 9.0

QP-2022-11-0026-DP

VIC3DA - Changes overview

Aim of this document is to report the reliability trials plan for Teseo-VIC3DA (VB8Z) product in order to qualify the following changes:

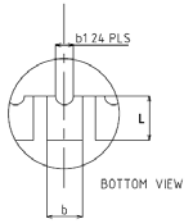
- Improvements
  - New MEMS from **ASM330LHH** to **ASM330LHHX** → enabling possible new SW features supported by **ASM330LHHX**
  - New diode **ESDAXLC6-1BU2** in addition to **ESD7501MUT5G** → Second source strategy
- Robustness

Move the TCXO supply enabling from stand-by out pin to VOL2 pin:

STA8089FGA (TeseoIII) standby_out pin could not be able to drive properly the TCXO VCC enable at start-up

  - Schematic change: TCXO supplied by switched VCC controlled by VOL2 → move from stand-by out pin to VOL2 pin the TCXO supply enabling
  - New LDO from **LD39020DTPU18R** to **STLQ020J18R** + additional resistor → to keep same level SW Stand-by current consumption

- Other
  - POA pads' length **L** dimension tolerance aligned to supplier's specification (from **0.9 ± 0.100** mm to **0.9 ± 0.125** mm)
    → no impact on customer PCB design



See the following slides for more details.

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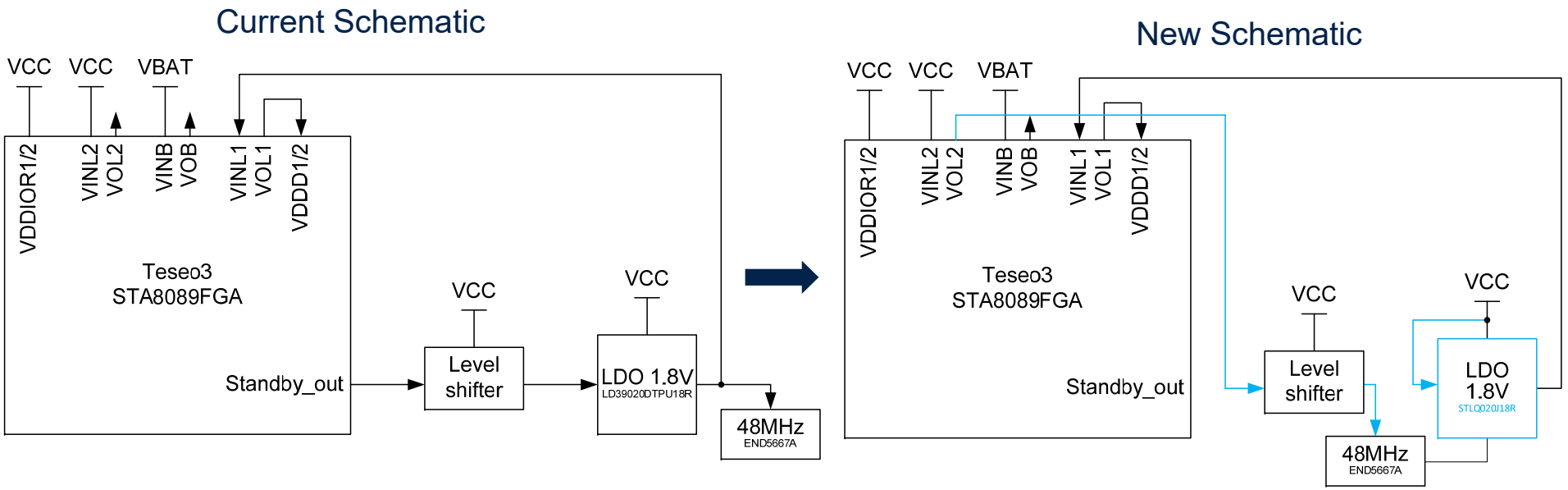
VIC3DA - Schematic changes details



- 48MHz TCXO supplied by switched VCC controlled by VOL2.
- New LDO **STLQ020J18R** has been selected for its low quiescent current (300 nA typ) in order to keep Teseo-VIC3DA SW stand-by current consumption same level as before.

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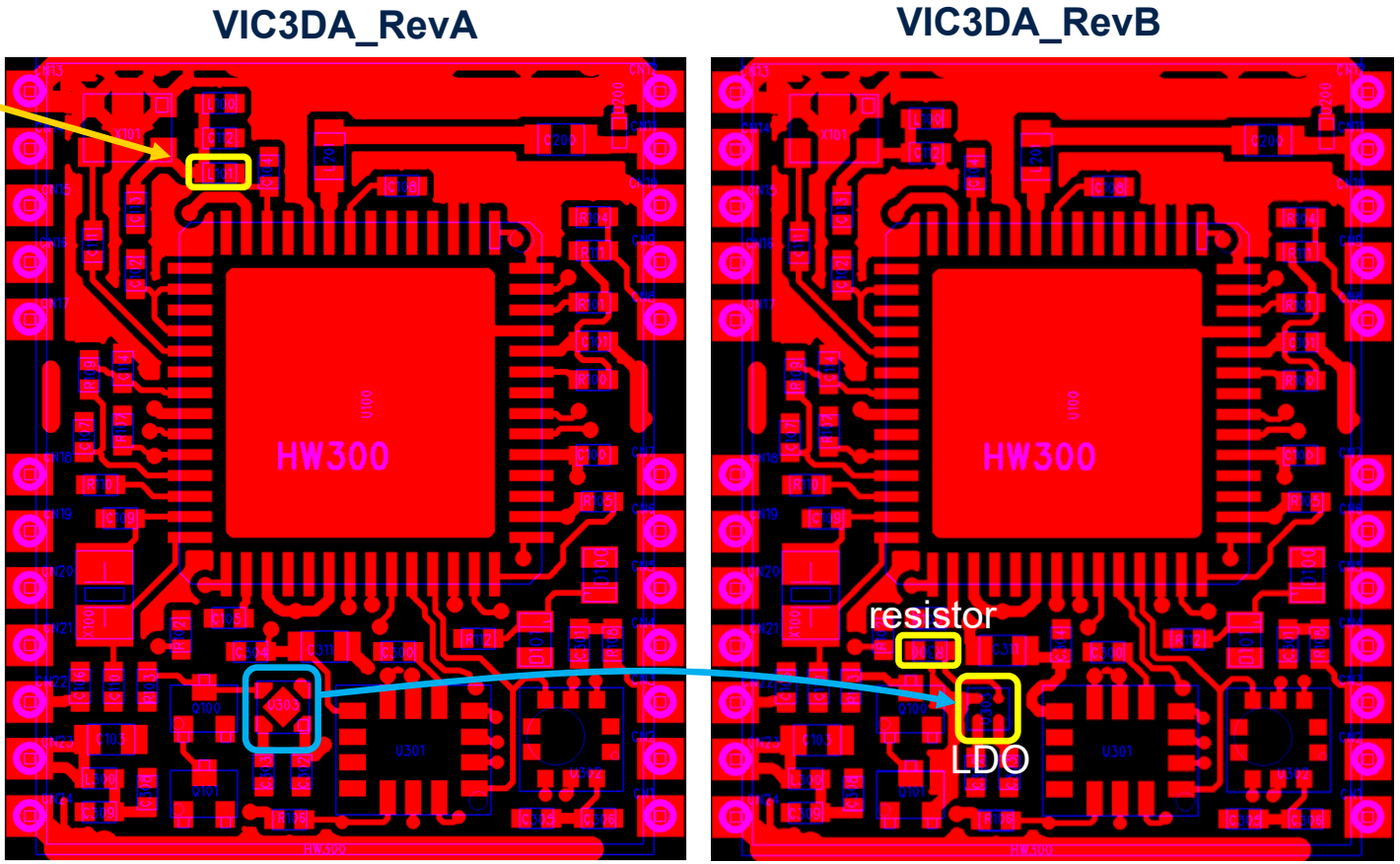
VIC3DA - PCB changes details

Highlighted footprint has been removed (no components mounted on it)



LDO: new component

Resistor: new component

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Qualification approach

- AEC-Q Table 2 (Process change qualification guidelines for the selection of tests)

Test #		A2	A3	A4	A5	A6	B1	B2	B3	C1	C2	C3	C4	C5	C6	C7	E2	E3	E4	E5	E6	E7	E8	E9
Test Abbreviation		**THB**	**AC**	**TC**	**PTC**	**HTSL**	**HTOL**	**ELFR**	**EDR**	**WBS**	**WBP**	**SD**	**PD**	**SBS**	**LI**	**XRAY**	**HBM**	**CDM**	**LU**	**ED**	**FG**	**CHAR**	**EMC**	**SER**
Change Type	**Change Impact**																							
Change from one AEC Qualified sub-component to another AEC Qualified sub-component	Critical characteristics of sub-component are affected						•		•								•	•	•	•	•	•	•	M
Change that adds or subtracts sub-components from the module BOM	Any		•	•			•	•									•	•	•	•	•	•	•	M

- ZVEI matrix indications

		THB	AC	TC	PTC	HTSL	HTOL	ELFR	EDR	WBS	WBP	SD	PD	SBS	LI	XRAY	HBM	CDM	LU	ED	FG	CHAR	EMC	SER	MECH	DROP	LT	DS	IWV	BLR	LTSL	STEP	MCMDROP	DPA	XRAY	AM
MCM-DE-02	Change that adds or subtracts sub-components from the module BOM	@•	•	•	@•	@•	•	•	-	-	-	-	-	-	-	-	•	•	•	•	•	•	•	M	@•,D	-	-	@F	-	-	-	-	-	-	-	-
MCM-PA-02	Replacement of any sub-component by an AEC qualified sub-component	-	-	-	-	-	•	-	•	-	-	-	-	-	-	-	•	•	•	•	•	•	•	M	@•,D	@•	-	@F	-	-	-	-	-	@•	@•	@•

Teseo VIC3DA – AECQ Qualification Matrix

Trial	Conditions	Trial2	Conditions	Sample x DIFFUSION Lot	Test Temperature
HTOL	1000hrs @ Ta = 85°C	-	-	77x1	C/R/H
ESD	HBM, CDM	-	-	50x1	R/H
LU	@25°C and @85°C	-	-	50x1	R/H
PC	JL3	THS	1000hrs [85°C/85°RH]	77x1	R/H
PC	JL3	TC	500cyc [-40°C/+85°C]	77x1	R/H

NOTE:

- PTC is not applicable due to the low device power consumption (based on the AECQ guideline).
- HTSL and THB are not necessary since new subcomponent (LDO) is already qualified as a standalone device.
- Production flow, must be done before starting all reliability trials.
- Parts need to be tested with individual datalog at each readout step.

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Mission Profile

Ta	15yrs Mission Profile			Equivalent Time at Tj temperature		
	Duration [h]	Junction Temperature [C°]	Operting Mode	HTDR Equivalent time at Tjunction 150°C Ea=0.7eV	HTSL Equivalent time at Tjunction 150°C Ea=1.0eV	HTOL Equivalent time at Tjunction 125°C Ea=0.75eV
-40	90	-20	Active operation	0.0	0.0	0.0
-20	450	0	Active operation	0.0	0.0	0.0
43	2700	63	Active operation	18.5	2.2	47.4
60	4950	80	Active operation	109.0	21.2	303.0
85	810	105	Active operation	82.0	30.7	254.1
			Active operation	0.0	0.0	0.0
			Active operation	0.0	0.0	0.0
			Active operation	0.0	0.0	0.0
9000						
	9000	Total active operation time		209	54	604
				Taking into account V acceleration		110
	131400	55	not operating	499.0695696	45.7964817	
		50	not operating	0	0	
		80	not operating	0	0	
		85	not operating	0	0	
		90	not operating	0	0	
		95	not operating	0	0	
		100	not operating	0	0	
		105	not operating	0	0	
	131400	Total not operation time		499	46	
				total HTSL (active + not operating time)		100

- Voltage acceleration factor (from CROLLES R&D): ~ 5.2x
- Mission profile is covered by AECQ standard with wide margin:
  - 1000hrs HTOL vs 110hrs profile and HTSL 1000hrs vs 100hrs profile (active + non active)

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Reliability Report

Teseo VIC3D/DA – VB8Z

New Version

General Information		
Commercial Product	:	*Teseo-VIC3D/DA*
Product Line	:	*F0CE*VIC3DA1, G0CE*VIC3D01*
Product Description	:	*Automotive GNSS dead-reckoning module with 6-axis IMU*
Package	:	*LCC 24 pins (16.0mm x 12.2mm x 2.42mm)*
Silicon Technology	:	*CMOS055*
Division	:	*MID*

Traceability		
Diffusion Plant	:	*ST Crolles 300*
Assembly Plant	:	*ASE Kr (996G)*

Reliability Assessment	
Passed	☒
Failed	☐

Disclaimer: *this report is a summary of the qualification plan results performed in good faith by STMicroelectronics to evaluate the electronic devices conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party, except in full, without previous written agreement by STMicroelectronics or under the approval of the author (see below)*

REVISION HISTORY

Version	Date	Author	Changes description
1.0	07/02/2024	M. Arani	First document release
2.0	12/02/2024	M. Arani	Minor errors fixed

APPROVED BY: **STEFANO TESTA**

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

Aim of this document is to describe the reliability trials needed to qualify the new LDO and PCB fix for Teseo-VIC3D/DA - VB8Z, device assembled in LCC 24 pins package family (ASE Kr).

The qualification plan takes into account the fact that this product is already qualified (RR-2021-06-0019-DP) and in production since Q2.2021. The attention is focused on the new sub-component used.

Qualification Plan is built based on Q100 Rev J Grade 3 (-40/+85°C) specification for electrical trials. Electrical and Package qualification executed under AEC-Q100 Grade 3 conditions.

Teseo-VIC3D/DA will be packaged in ASE Korea (996G) assembly line as LCC 24 pins. Assy report collected on the qualification lot.

The qualification strategy is based on one assembly lot.

1.2 Reliability Test Plan

Reliability tests performed on this device are in agreement with **ST 0061692** and **AEC Q100 Rev J** specification and are listed in the Test Plan.
For details on test conditions, generic data used and spec reference see test result summary at Par.3.

1.2.1 Test Plan

TEST GROUP	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
A Accelerated Environment Stress	**PC (JL3)**	Preconditioning (JL3+3 reflow simulation)	Y
	THB	Temperature Humidity Bias	N
	THS	Temperature Humidity Storage	Y
	TC	Temperature Cycling	Y
	PTC	Power Temperature Cycling	NA
	HTSL	High Temperature Storage Life	N
B Accelerated Environment Stress	**HTOL**	High Temperature Operating Life	Y
	ELFR	Early Life Failure Rate	NA
	EDR	Electrical Data Retention for NVM	NA
C Package Assembly Integrity	**WBS**	Wire Bond Shear	NA
	WBP	Wire Bond Pull	NA
	SD	Solderability	Y
	PD	Physical Dimension	Y
	SBS	Solder Ball Shear	NA
	LI	Lead Integrity	NA
E Electrical Verification	**ESD (HBM)**	Electrostatic Discharge (Human Body Model)	Y
	ESD (CDM)	Electrostatic Discharge (Charged Device Model)	Y
	LU	Latch Up	Y
	ED	Electrical distribution	Y
	FG	Fault grade	NA
	CHAR	Characterization	N
	EMC	Electromagnetic Compatibility	NA
	SC	Short Circuit Characterization	NA
	SER	Soft Error Rate	NA
D Die Fabrication Reliability	Test list is reported in AEC-Q100 table at Par.4	Performed during process qualification	Y
F Defect Screening	Test list is reported in AEC-Q100 table at Par.4	To be implemented starting from first production lot	Y
G Cavity Package Integrity	Test list is reported in AEC-Q100 table at Par.4	Not for plastic packaged devices	NA

Flag agenda: Y= Done; N= Not Done; S= Similarity (Generic Data); NA= Not Applicable.

1.3 Conclusion

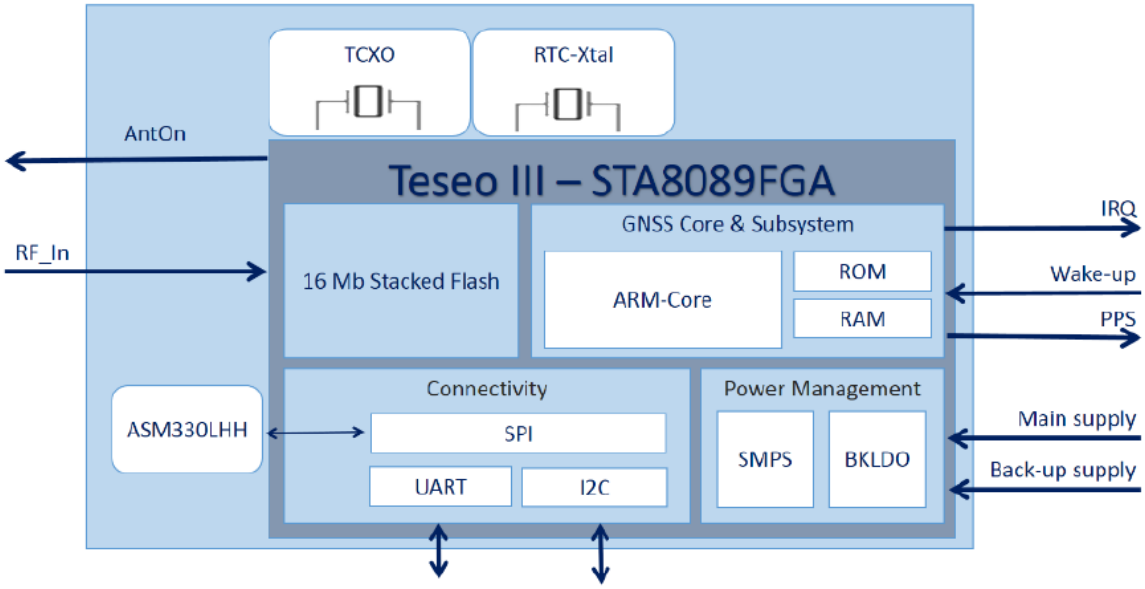
All necessary Q100 reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at electrical testing.
Package oriented tests have not put in evidence any criticality up to Grade 3 specification.
ESD & Latch-UP completed following AEC-Q100 dedicated spec. Details available in the specific report section.

Based on the overall results obtained, we can give a positive judgment on the reliability evaluation of new LDO used + PCB fix for Teseo-VIC3D/DA assembled ASE Korea (996G).

2 DEVICE CHARACTERISTICS

2.1 Ballout

2.2 Block diagram



2.3 Traceability

2.3.1 Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	NA
Wafer diameter (inches)	NA
Silicon process technology	NA

2.3.2 Assembly information

Assembly Information	
Assembly plant location	*996G – ASE KOREA*
Package code description	*LCC 24 pins 16.0mm x 12.2mm x 2.42mm*

2.3.3 Reliability testing information

Reliability Testing Information	
Reliability laboratory location	*ST - Agrate Brianza, ST - Castelletto,*
Electrical testing location	*ST – Agrate Brianza*
Tester	*Diamond X*

3 TESTS RESULTS SUMMARY

3.1 Lot Information

QUALIFICATION LOTS				
Lot #	**Diffusion Lot**	**Assy Lot/ Trace Code**	**RawLine**	**Note**
1	NA	HA332GZA	F0CE*VIC3DA1	Qual Lot 1

3.2 Test results summary

Test plan results are summarized in the Q100 Rev J Template.
In Test Conditions column are also reported Electrical Temp and Physical Analysis required by AEC spec (**in bold**) and any additional STM requirements.
Test method revision reference is the one active at the date of reliability test trial.

3.2.1 Test results summary (Q100 Rev J)

Test	#	Reference	Q100/STM Test Conditions	Lots	S.S.	Total	Results Lot/Fail/S.S.	Comments: (N/A =Not Applicable)
TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS								
PC	A1	JESD22 A113 J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C ☒ **Testing at Room *(pre)*** ☐ Testing at Cold *(pre)* ☒ **Testing at Hot *(pre)*** ☐ 100 Temperature Cycles *(pre)* ☐ C/T-SAM *(pre / post)* ☐ Cross section ** Post test temp according to subsequent test requirement*		Lot 1: 0 / 170	All lots completed PC without any fail.

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Fail/S.S.	Comments: (N/A =Not Applicable)
THB	A2	JESD22 A101	Ta=85°C, 85%RH, Duration= 1000hrs ☐ After PC ☐ Testing at Room ☐ Testing at Cold ☐ Testing at Hot ☐ Drift Analysis ☐ C-SAM post ☐ WBP (first / second bond) ☐ WBS ☐ Internal Inspection ☐ Cross section ☐ Cratering test	-	-	-		Not planned
THS	A3	JESD22-A102	Ta=85°C, 85%RH Duration= 1000hrs ☒ **After PC** ☒ **Testing at Room** ☐ Testing at Cold ☒ **Testing at Hot** ☐ Drift Analysis ☐ C/T SAM pre ☐ C/T SAM post ☐ WBP (first / second bond) ☐ WBS ☐ Internal Inspection ☐ Cross section ☐ Cratering test	1	77	77	Lot 1: 0 / 77	All lots completed 1000hrs of stress without any fail
TC	A4	JESD22 A104	Ta=-40°C /+85 °C Duration= 500 cyc ☒ **After PC** ☒ **Testing at Room** ☐ Testing at Cold ☒ **Testing at Hot** ☐ Drift Analysis ☐ C/T SAM pre ☐ C/T SAM post ☐ WBP (first / second bond) ☐ WBS ☐ Internal Inspection ☐ Cross section ☐ Cratering test	1	77	77	Lot 1: 0 / 77	All lots completed 1000cyc of stress without any fail.

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Fail/S.S.	Comments: (N/A =Not Applicable)
HTSL	A6	JESD22 A103	Ta= 150ºC Duration= 500hrs ☐ After PC ☐ Testing at Room ☐ Testing at Cold ☐ Testing at Hot ☐ Drift Analysis ☐ C/T SAM pre ☐ C/T SAM post ☐ WBP (first / second bond) ☐ WBS ☐ Internal Inspection ☐ Cross section ☐ Cratering test	-	-	-		Not planned

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

HTOL	B1	JESD22 A108	Ta= 85ºC (TJ=**?**C) Duration= 1000hrs These are the min values. (*Tj and Duration must be defined to cover product mission profile approach)* ☐ After PC ☒ **Testing at Room** ☒ **Testing at Cold** ☒ **Testing at Hot** ☐ Drift Analysis ☐ Internal Inspection	1	77	77	Lot 1: 0 / 77	All lots completed 1000hrs stress without any fail.
ELFR	B2	AEC-Q100-008	Burn-in conditions with -Tj=125C (Ta max=105C) -Duration=24hrs ☐ Testing at Room ☐ Testing at Cold ☐ Testing at Hot ☐ Drift Analysis	-	-	-		Not planned

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Fail/S.S.	Comments: (N/A =Not Applicable)

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)	-	-	-		NA
WBP	C2	Mil-STD-883, Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	-	-	-		NA .
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8hr steam aging prior to testing	1	10	10	PASSED	Data collected in assy report
PD	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	1	10	10	PASSED	Data collected in assy report
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	-	-	-		NA
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through- hole only; 10 leads from each of 5 devices	-	-	-		NA (Through-hole devices only)

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

EM	D1	JESD61	Data, test method and criteria should be available upon request	-	-	-		NA
TDDB	D2	JESD35	Data, test method and criteria should be available upon request	-	-	-		NA
HCI	D3	JESD60 & 28	Data, test method and criteria should be available upon request	-	-	-		NA
NBTI	D4	JESD90	Data, test method and criteria should be available upon request	-	-	-		NA
SM	D5	JESD61, 87, & 202	Data, test method and criteria should be available upon request	-	-	-		NA

Test	#	Reference	STM Test Conditions	Lots	S.S.	Total	Results Lot/Fail/S.S.	Comments: (N/A =Not Applicable)

TEST GROUP E – ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test: All parametric and functional tests	All	All	All	PASSED	
HBM	E2	AEC-Q100-002	Target HBM=+/-2kV ☒ **Testing at Room** ☐ Testing at Cold ☒ **Testing at Hot** ☐ Drift Analysis	1	See test method		PASSED	ESD report: EL018723AG8209
CDM	E3	AEC-Q100-011	Target CDM=+/-750V on corner pins; +/- 500V all others ☒ **Testing at Room** ☐ Testing at Cold ☒ **Testing at Hot** ☐ Drift Analysis	1	See test method		PASSED	ESD report: EL018723AG8209
LU	E4	AEC-Q100-004	Current Injection Class II – Level A (+/- 100mA) ☒ **Testing at Room** ☐ Testing at Cold ☒ **Testing at Hot**	1	6	6	PASSED	ESD report: EL018723AG8209
LU	E4	AEC-Q100-004	Overvoltage Class II – Level A (1,5 x Vmax) ☒ **Testing at Room** ☐ Testing at Cold ☒ **Testing at Hot**	1	6	6	PASSED	ESD report: EL018723AG8209
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk >1.67)	All	All	All		Done on qualification units
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-		Not Planned
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	-	-	-		Not planned
SC	E10	AEC Q100-012	Short Circuit Characterization	-	-	-		NA

SER	E11	JESD89-1 JESD89-2 JESD89-3	Applicable to devices with memory sizes 1Mbit SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications	-	-	-		NA

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Fail/S.S.	Comments: (N/A =Not Applicable)

TEST GROUP F – DEFECT SCREENING TESTS

PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	All	All	All	Requested	It will be implemented starting from first production lot
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	All	All	All	Requested	It will be implemented starting from first production lot