


**PRODUCT / PROCESS CHANGE NOTIFICATION**

**1. PCN basic data**

1.1 Company		STMicroelectronics International N.V
1.2 PCN No.	AMS/23/14305	
1.3 Title of PCN	Introduction of additional SO8 package products on TSHT China assembly lines (General Purpose Analog)	
1.4 Product Category	See product list	
1.5 Issue date	2023-09-20	

**2. PCN Team**

<b>2.1 Contact supplier</b>	
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<b>2.2 Change responsibility</b>	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Salvatore DI VINCENZO
2.1.3 Quality Manager	Jean-Marc BUGNARD

**3. Change**

<b>3.1 Category</b>	<b>3.2 Type of change</b>	<b>3.3 Manufacturing Location</b>
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	TSHT CHINA

**4. Description of change**

	<b>Old</b>	<b>New</b>
4.1 Description	Assembly plant : ST Bouskoura	Assembly plant : ST Bouskoura TSHT China
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

**5. Reason / motivation for change**

5.1 Motivation	SO8 line in TSHT is already running with high volumes for 6 years for GPA products. ST is pleased to announce the introduction of additional products on this line. The goal is to provide a better support to our customers by enhancing the manufacturing process for higher volume production.
5.2 Customer Benefit	CAPACITY INCREASE

**6. Marking of parts / traceability of change**

6.1 Description	New finished good codes
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**7. Timing / schedule**

7.1 Date of qualification results	2023-09-18
7.2 Intended start of delivery	2023-12-31
7.3 Qualification sample available?	Upon Request

**8. Qualification / Validation**

8.1 Description	14305 ExternalReliabilityEvaluationReport_TSHT bin1.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2023-09-20

9. Attachments (additional documentations)
14305 Public product.pdf 14305 ExternalReliabilityEvaluationReport_TSHT bin1.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
LM258ADT	LM258ADT	
	LM258AWDT	
LM293ADT	LM293ADT	
LM358AD	LM358AD	
LM358ADT	LM358ADT	
	LM358AWDT	
LM393ADT	LM393ADT	
TL071ACDT	TL071ACDT	
TL071IDT	TL071IDT	
TL072ACDT	TL072ACDT	
	TL072BIDT	
TL072IDT	TL072IDT	
TL081IDT	TL081IDT	
TL082ACDT	TL082ACDT	
	TL082BCDT	
TL082ID	TL082ID	
TL082IDT	TL082IDT	
	TS9222IDT	
TS922AID	TS922AID	
TS922AIDT	TS922AIDT	

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**PRODUCT/PROCESS  
CHANGE NOTIFICATION**

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PCN AMS/23/14305

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**Analog, MEMS & Sensors (AMS)**

**Introduction of additional SO8 package products  
on TSHT China assembly lines  
(General Purpose Analog)**

## WHAT:

SO8 line in TSHT is already running with high volumes for 6 years for GPA products. ST is pleased to announce the introduction of additional products on this assembly line.

Please find more information related to material change in the table here below

Material	Current process	Modified process	Comment
Diffusion location	ST Singapore UMC (Taiwan)/Crolles	ST Singapore UMC (Taiwan)/Crolles	No change
Assembly location	ST Bouskoura	TSHT China	
Molding compound	Sumitomo G700KC	Hitachi CEL-9220	
Die attach	Ablestick 8601-S25	Henkel 8200T	
Leadframe	Copper	Copper	
Plating	Matte Sn	Matte Sn	
Wire	Copper 1mil	Copper Pd coated 1 mil	

## WHY:

The purpose of the extension to additional product of usage of SO8 TSHT line is to provide a better support to our customers by enhancing the manufacturing process for higher volume production.

## HOW:

The qualification program consists mainly of comparative electrical characterization and reliability tests.

You will find here after the qualification test plan which summarizes the various test methods and conditions that ST uses for this qualification program.

## WHEN:

The production in TSHT China for these additional products will start Q4/2023.

## Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.

There is -as well- no change in the packing process or in the standard delivery quantities. Shipments may start earlier with the customer's written agreement.

# External Reliability Evaluation Report

*New assembly plant TSHT for selected products*

General Information		Locations	
<b>Product Line</b>	0158, 0922, 3702, V802,	<b>Wafer fab</b>	Ang Mo Kio 6", ST Catania
<b>Product Description</b>	Low power dual op-amps with low input bias current, Dual op amp, Dual comparator, Dual op amp	<b>Assembly plant</b>	TSHT (TianShui Huatian Technology) China
<b>P/N</b>	LM358ADT, TS922AIDT, TS3702IPT, LMV358LIPT	<b>Reliability Lab</b>	Grenoble
<b>Product Group</b>	AMG		
<b>Product division</b>	GPA		
<b>Package</b>	SO8, TSSOP8		
<b>Silicon Process technology</b>	Bipolar, BCD6, HF2CMOS, HC1PA, HF5CMOS		

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.  
 This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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## **1 APPLICABLE AND REFERENCE DOCUMENTS**

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

## **2 GLOSSARY**

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

## **3 RELIABILITY EVALUATION OVERVIEW**

### **3.1 Objectives**

The goal of the qualification is to introduce additional general purpose analog products products assembled is SO8 package on TSHT production line.

The line under qualification will serve several part numbers.  
The qualification plan is based on the similarity and based on the JESD47 specification.

### **3.2 Conclusion**

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Reliability agreement for qualification.



## 4 DEVICE CHARACTERISTICS

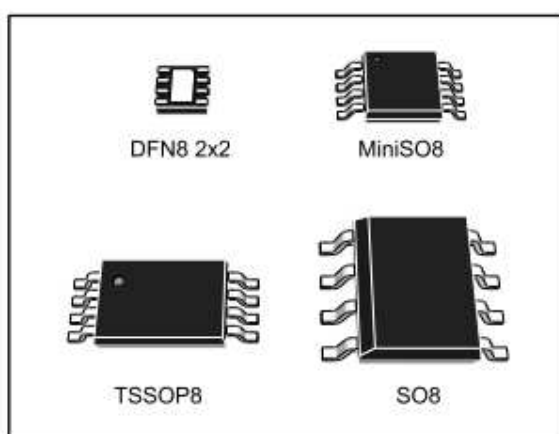
### 4.1 Device description



## LM158, LM258, LM358, LM158A, LM258A, LM358A

### Low-power dual operational amplifiers

Datasheet - production data



#### Related products

- See LM158W for enhanced ESD ratings
- See LM2904 and LM2904W for automotive grade versions

#### Description

These circuits consist of two independent, high-gain, internally frequency-compensated op amps, specifically designed to operate from a single power supply over a wide range of voltages. The low-power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits, which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard 5 V, which is used in logic systems and will easily provide the required interface electronics with no additional power supply.

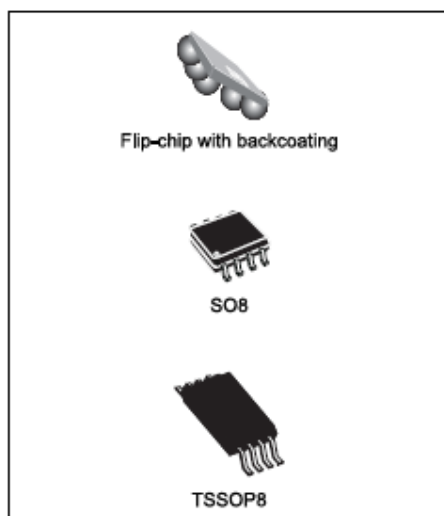
In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

#### Features

- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current per channel essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 2 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rails
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing  
0 V to ( $V_{CC} - 1.5$  V)

## Rail-to-rail, high output current, dual operational amplifier

Datasheet - production data



### Applications

- Headphone and servo amplifiers
- Sound cards, multimedia systems
- Line drivers, actuator drivers
- Mobile phones and portable equipment
- Instrumentation with low noise as key factor
- Piezoelectric speaker drivers

### Description

TS922 and TS922A devices are rail-to-rail dual BiCMOS operational amplifiers optimized and fully specified for 3 V and 5 V operation. These devices have high output currents which allow low-load impedances to be driven.

Very low noise, low distortion, low offset, and a high output current capability make these devices an excellent choice for high quality, low voltage, or battery operated audio systems.

The devices are stable for capacitive loads up to 500 pF.

### Features

- Rail-to-rail input and output
- Low noise: 9 nV/√Hz
- Low distortion
- High output current: 80 mA (able to drive 32 Ω loads)
- High-speed: 4 MHz, 1 V/μs
- Operating from 2.7 to 12 V
- Low input offset voltage: 900 μV max. (TS922A)
- ESD internal protection: 2 kV
- Latch-up immunity
- Macromodel included in this specification
- Dual version available in Flip-chip package



## TS3702

### Micropower dual CMOS voltage comparators

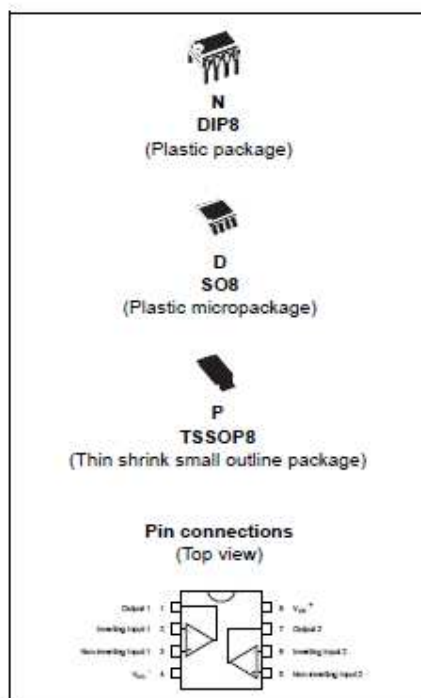
#### Features

- Push-pull CMOS output (no external pull-up resistor required)
- Extremely low supply current: 9µA typ / comparator
- Wide single supply range: 2.7V to 16V or dual supplies ( $\pm 1.35V$  to  $\pm 8V$ )
- Extremely low input bias current: 1pA typ
- Extremely low input offset currents: 1pA typ
- Input common-mode voltage range includes GND
- High input impedance:  $10^{12}\Omega$  typ
- Fast response time: 2µs typ for 5mV overdrive
- Pin-to-pin and functionally compatible with bipolar LM393

#### Description

The TS3702 is a micropower CMOS dual voltage comparator with extremely low consumption of 9µA typ / comparator (20 times less than bipolar LM393). The push-pull CMOS output stage allows power and space saving by eliminating the external pull-up resistor required by usual open-collector output comparators.

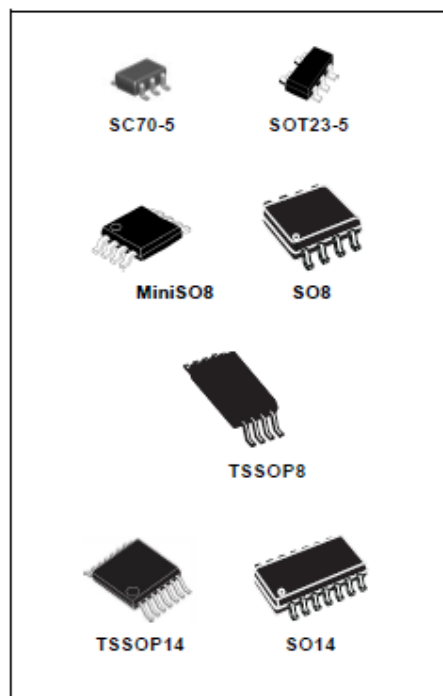
Thus response times remain similar to the LM393.



## LMV321L, LMV358L, LMV324L

Low-power, general-purpose operational amplifiers

Datasheet - production data



### Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

### Description

The LMV321L, LMV358L, and LMV324L are single, dual, and quad operational amplifiers with rail-to-rail output capabilities. They are specifically designed to operate at low voltages (2.7 V to 5 V) with enhanced performances compared to the industry standard LM3xx series.

The LMV321L, LMV358L, and LMV324L are offered in tiny packages, allowing the devices to be used in small portable electronic applications and to be placed closer to the actual signal.

The LMV321L, LMV358L, and LMV324L are complete cost-effective solutions for application designs where cost is of primary importance.

### Features

- Low-power consumption: 250  $\mu$ A max at 5 V
- Low offset voltage: 7 mV max at 25 °C
- Industrial temperature range: -40 °C to +125 °C
- Low supply voltage: 2.7 V - 5.5 V
- Gain bandwidth product: 1.3 MHz
- Tiny packages

## Construction note

New Plant Qualification				
	P/N LM358DT	P/N TS922IPT	P/N TS3702IPT	P/N LMV358LIPT
Wafer/Die fab. information				
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore	UMC Taiwan
Technology	PRO450S-C	HF2CMOS	HC1PA	HF5CMOS
Process family	Bipolar	HF2CMOS	HC1PA	HF5CMOS
Die finishing back side	Raw Silicon	Raw Silicon	Lapped silicon	Lapped silicon
Die size	1070 x 1010 $\mu\text{m}^2$	1720x1190 $\mu\text{m}^2$	1366x1136 $\mu\text{m}^2$	1062x802 $\mu\text{m}^2$
Passivation type	SiN (nitride)	PVAPOX+Nitride	PVAPOX+Nitride	USG-PSG-SiON-PIX
Wafer Testing (EWS) information				
Electrical testing manufacturing location	ST SINGAPORE	ST SINGAPORE	ST SINGAPORE	ST SINGAPORE
Assembly information				
Assembly site	TSHT	TSHT	TSHT	TSHT
Package description	SO8	TSSOP8	TSSOP8	TSSOP8
Molding compound	Hitachi CEL-9220	Hitachi CEL-9220	Hitachi CEL-9220	Hitachi CEL-9220
Frame material	Copper	Copper	Copper	Copper
Die attach process	Glue	Glue	Glue	Glue
Die attach material	Ablestik - 8200T-	Ablestik - 8200T	Ablestik - 8200T	Ablestik - 8200T
Wire bonding process	Wire	Wire	Wire	Wire
Wires bonding materials/diameters	1.0mil PdCu	1.0mil PdCu	1.0mil PdCu	1.0mil PdCu
Lead finishing process	Copper	Copper	Copper	Copper
Lead finishing/bump solder material	Sn	Sn	Sn	Sn
Final testing information				
Testing location	TSHT	TSHT	TSHT	TSHT

## 5 TESTS RESULTS SUMMARY

### 5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	SO8/Bipolar	0158	
2	SO8/Bipolar	0158	
3	SO8/Bipolar	0158	
4	TSSOP8/HF2CMOS	0922	
5	TSSOP8/HC1PA	3702	
6	TSSOP8/HF5CMOS	V802	

Detailed results in below chapter will refer to P/N and Lot #.

### 5.2 Test plan and results summary

P/N LM358ADT

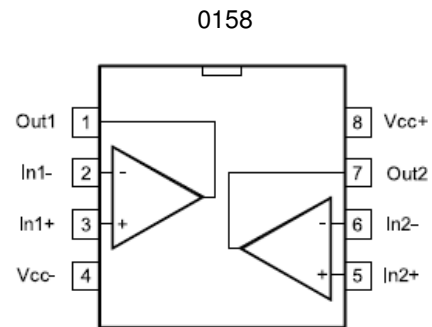
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
Die Oriented Tests									
HTOL	N	JESD22 A-108	Tj = 125°C, BIAS	80	168 H	0/80	0/80	0/80	
					500 H	0/80	0/80	0/80	
					1000 H	0/80	0/80	0/80	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/77	0/77		
					500 H				
					1000 H	0/77	0/77		
ELFR	N	AEC Q100 - 008		400	48H	0/400	0/401	0/396	
Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125°C		Final	PASS	PASS	PASS	
			Store 192 H @ Ta=30°C Rh=60%						
			Over Reflow @ Tpeak=260°C 3 times						
uHAST	Y	JESD22 A-118	T°=130°C; Pressure=2.3 atm; HR=85%		96 H	0/80	0/80		
THS	Y	JESD22 A-110	Ta = 85°C, RH = 85%,		168 H	0/80			
					1000 H	0/80			
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77		
					1000 cy	0/77	0/77		
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
Other Tests									
ESD	N	AEC Q101-001, 002 and 005	CDM	3	1.5kV	PASS			

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						Lot 7 0922	Lot 8 3702	Lot9 V802		
HTOL	N	JESD22 A-108	Ta=125°C, BIAS		168 H	0/77	0/77	0/77		
					500 H	0/77	0/77	0/77		
					1000 H	0/77	0/77	0/77		
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/77	0/77	0/77		
					500 H	0/77	0/77	0/77		
					1000 H	0/77	0/77	0/77		
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS		
UHAST	Y	JESD22 A-102	85%RH / Ta=130°C		96 H	0/77	0/77	0/77		
TC	Y	JESD22 A-104	Ta = -55°C to 150°C		100 cy	0/77	0/77	0/77		
					200 cy	0/77	0/77	0/77		
					500 cy	0/77	0/77	0/77		
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H	0/77	0/77	0/77		
					500 H	0/77	0/77	0/77		
					1000 H	0/77	0/77	0/77		

## **6 ANNEXES**

### **6.1 Device details**

#### **6.1.1 Pin connection**





## 6.1.2 Package outline/Mechanical data

### PACKAGE OUTLINE ASSEMBLY

TITLE: POA SO 8L

PLANT CODE: 999L

PACKAGE CODE: 07

PACKAGE WEIGHT: 0,0765 g/unit typ

JEDEC REFERENCE NUMBER: JEDEC MS-012-AA

Option C

### PACKAGE DIMENSIONS

DATABOOK				
SYMBOL				NOTE
	MIN.	NOM.	MAX.	
A	-	-	1.75	
A1	0.10	-	0.225	
A2	1.30	1.40	1.50	
A3	0.60	0.65	0.70	
b	0.39	-	0.47	
b1	0.38	0.41	0.44	
c	0.20	-	0.24	
c1	0.19	0.20	0.21	
D	4.80	4.90	5.00	
E	5.80	6.00	6.20	
E1	3.80	3.90	4.00	
e	1.27BSC			
L1	1.05REF			
h	0.25	-	0.50	
L	0.50	-	0.80	
Ø	0	-	8°	

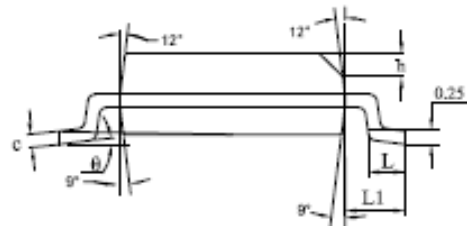
#### NOTES:

1. Controlling Dimension: MILLIMETER
2. Package outline exclusive of any mold flashes dimensions and metal burrs
3. Max resin gate protrusion : 0.20mm

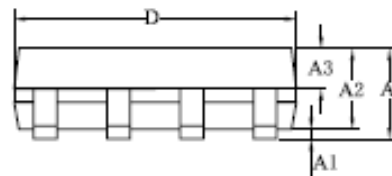
# PLANT CODE: 999L

## SO 8L

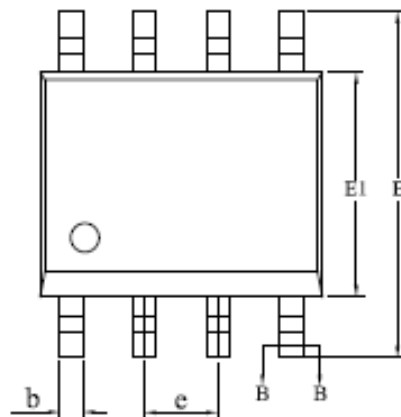
SIDE VIEW



SIDE VIEW

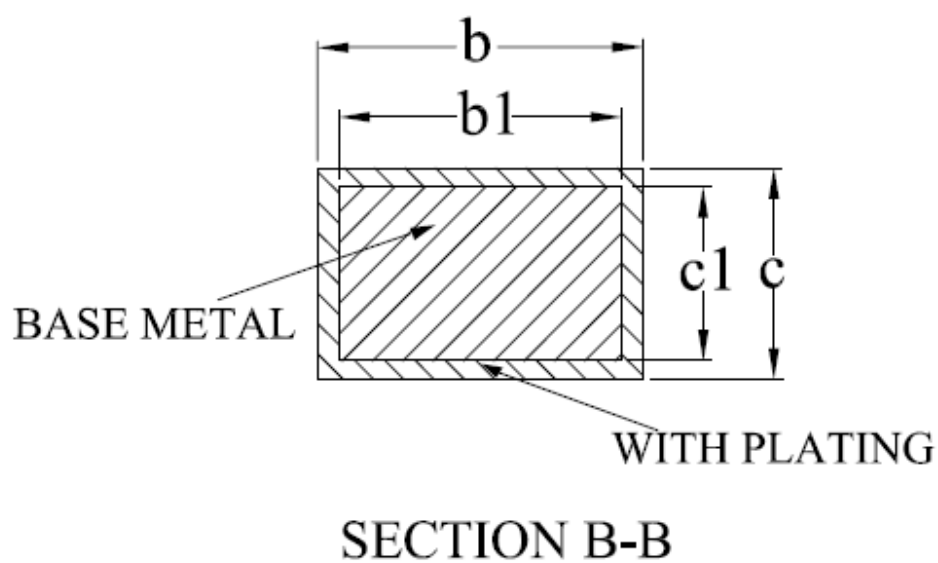


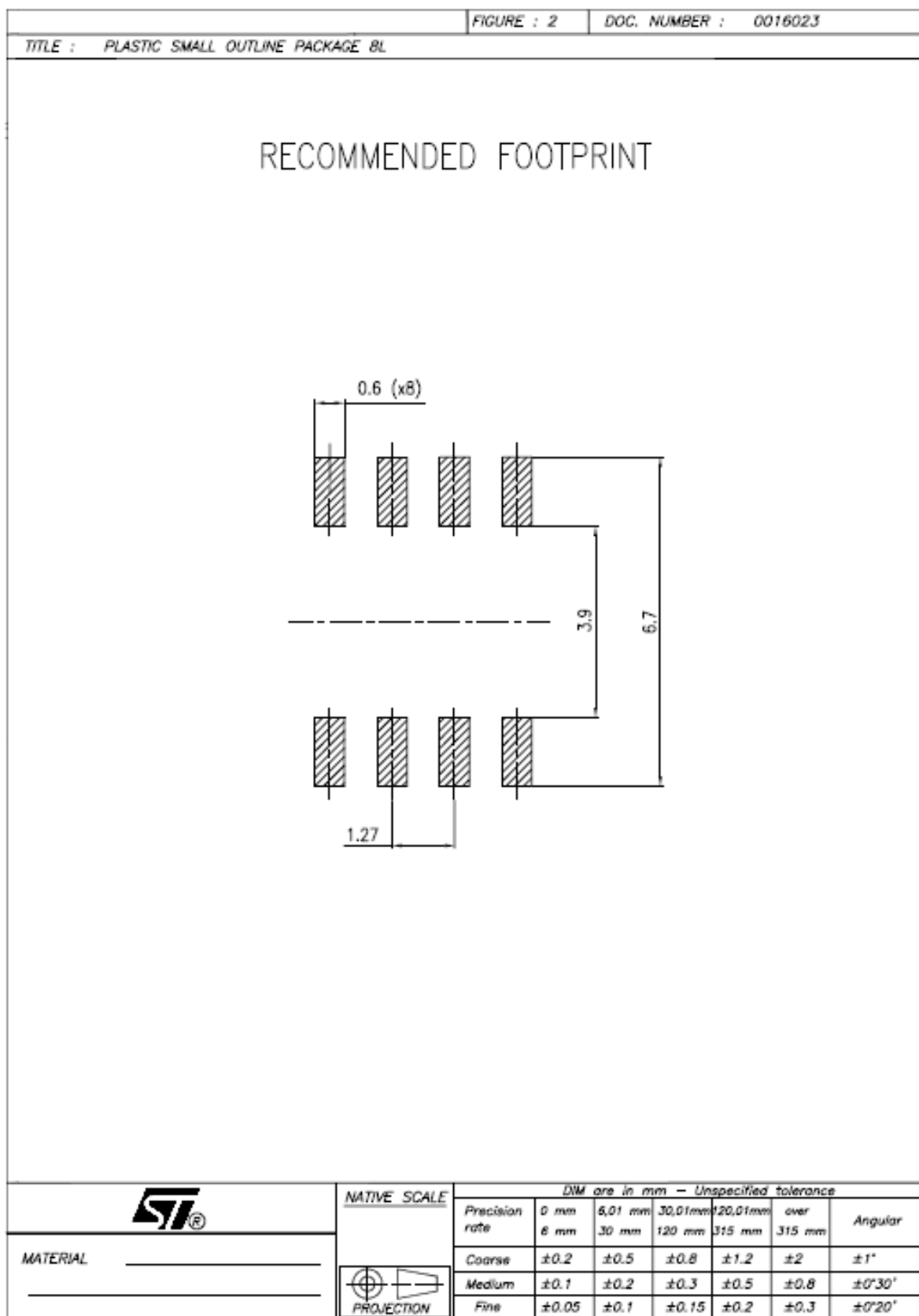
TOP VIEW



PLANT CODE: 999L

S0 8L





## 6.2 Tests Description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTOL</b> Higt Temperature Operating Life  <b>HTB</b> High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
<b>HTSL</b> High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
<b>ELFR</b> Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
<b>Package Oriented</b>		
<b>PC</b> Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
<b>AC</b> Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>TC</b> Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>THB</b> Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
<b>Other</b>		
<b>ESD</b> Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. <b>CBM:</b> Charged Device Model <b>HBM:</b> Human Body Model <b>MM:</b> Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.

## Annex 1: Other results

## Wire pull test

Value in gram (min limit 4g)						
	Unit 1	Unit 2	Unit 3	Unit 4	Unit 5	Unit 6
	23.67	23.97	22.2	21.1	22.17	20.99
	24.06	23.24	23.14	20.26	19.5	24.18
	19.33	24.01	21.18	23	25.42	19.36
	19.58	22.17	20.99	21.15	24.64	22.17
	20.16	20.35	24.87	22.87	24.2	20.5
	20.48	20.69	22.96	21.55	22.5	25.97
	20.77	21.29	21.34	21.51	21.3	24.64
	21.65	21.79	20.85	23.26	23.31	24.2
Min(g)	19.33					
Max(g)	25.97					
average(g)	22.09					
cpl	3.56					

## Wire shear test

Value in gram (min limit 18g)						
	Unit 1	Unit 2	Unit 3	Unit 4	Unit 5	Unit 6
	46.89	49.58	48.33	49.26	46.21	46.88
	48.15	46.33	46.27	47.55	48.71	49.54
	45.25	49.88	16.86	45.65	49.55	49.67
	48.22	48.37	48.17	48.14	46.35	49.18
	47.36	48.16	46.88	49.33	45.33	49.24
	48.31	48.87	47.33	48.98	49.36	48.98
	49.16	49.33	45.33	50.17	48.71	48.36
	48.24	47.24	46.24	48.98	49.36	48.78
Min (g)	16.86					
Max (g)	50.17					
Average (g)	46.67					
cpl	2.05					

Conclusion: in line with ST specification

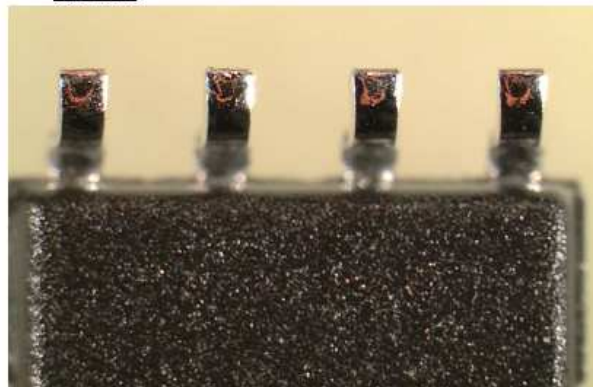
Solderability  
Coverage minimum 95% after dipping

PACKAGE	SOLDER BATH	SOLDER BATH TEMP.	SOLDER DIPPING TIME	AGING	SAMPLING	REJECT
Lead finishing Sn Preplated	SnPb	220°C	10s	8h steam @85°C/85HR	10	0
			10s	16hrs dry air @150°C	10	0
	SnAgCu	245°C	10s	8h steam @85°C/85HR	10	0
			10s	16hrs dry air @150°C	10	0

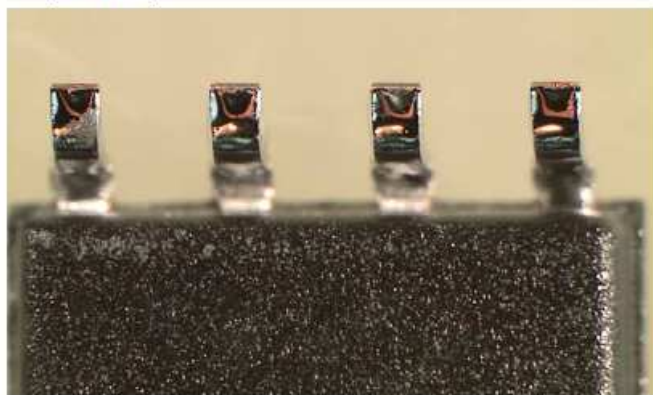
Dry air SnAgCu



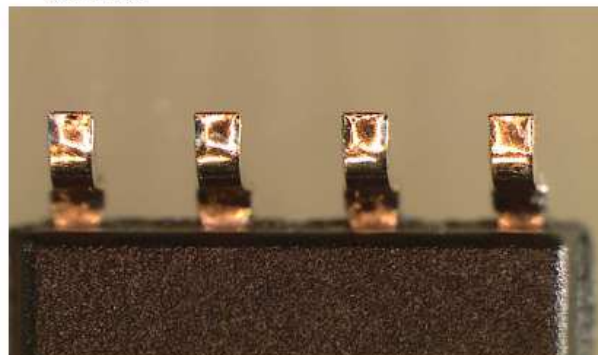
Steam SnPb



Dry air SnPb

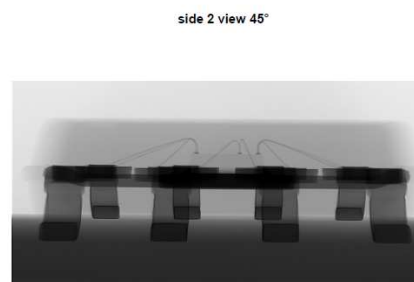
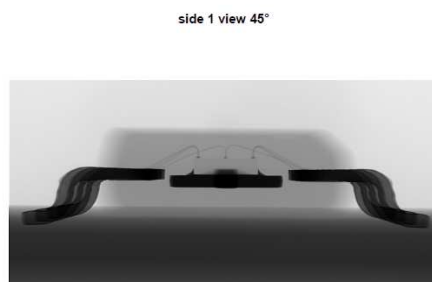
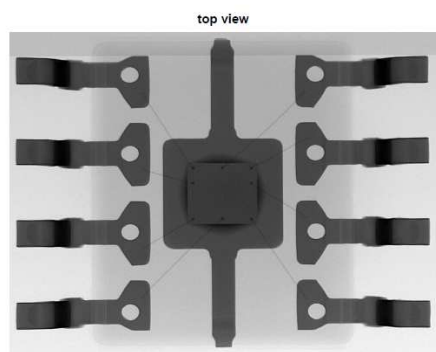


Steam SnAgCu



Conclusion: in line with ST specification.

## Xray pictures







## Public Products List

Public Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

**PCN Title :** Introduction of additional SO8 package products on TSHT China assembly lines (General Purpose Analog)

**PCN Reference :** AMS/23/14305

**Subject :** Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

TS922AIDT	LM258AWDT	TL071IDT
TL072ACDT	LM258ADT	LM358ADT
TL082ID	TL072BIDT	TL082ACDT
LM358AD	LM293ADT	TS9222IDT
TS922AID	LM393ADT	TL082IDT
TSL6002IDT	TL072IDT	TL082BCDT
LM358AWDT	TL081IDT	

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