PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	AMS/22/13267
1.3 Title of PCN	Qualification of UTAC / UTL3 for Assembly of selected products in VFQFPN
1.4 Product Category	See product list
1.5 Issue date	2022-02-21

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Salvatore DI VINCENZO
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	UTAC

4. Description of change		
	Old	New
4.1 Description	Assembly : - UTAC UTL1	Assembly : - UTAC UTL3
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	Additional Capacity
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change	
6.1 Description	New finished good codes

7. Timing / schedule	
7.1 Date of qualification results	2022-02-11
7.2 Intended start of delivery	2022-05-20
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13267 Report_utac-V526-intermediate.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2022-02-21

9. Attachments (additional documentations)
13267 Public product.pdf 13267 Report_utac-V526-intermediate.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STG3482QTR	
	STG3692QTR	
	STG3693QTR	

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PCN Title : Qualification of UTAC / UTL3 for Assembly of selected products in VFQFPN

PCN Reference : AMS/22/13267

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STG3693QTR	STG3692QTR	STG3482QTR

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Internal Reliability Evaluation Report

line V52601

General Information	
Product Line	V52601
Product Description	Low voltage high bandwidth quad SPDT switch
P/N	STG3693QTR
Product Group	AMG
Product division	GPA&RF
Package	VFQFPN16
Silicon Process technology	HCMOS6
Production mask set rev.	1

Locations	
Wafer fab	USIF (UMC Fab8"C)
Assembly plant	UTL3
Reliability Lab	Grenoble
Reliability assessment	In Progress

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	09/02/2022		Claudine Larato		

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this qualification is to qualify V52601, V48201 and V69201 Qual in UTL3, on one selected lines V52601, standard version, in VFQFPN16 package.
The qualification plan is based on the similarity and based on the JESD47 specification.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Reliability agreement for the maturity 30 level is done for this V52601 and similar family line.

4 DEVICE CHARACTERISTICS

4.1 Device description

life.augmented

STG3693

Datasheet

Low voltage high bandwidth quad SPDT switch

QFN16L
(2.6x1.8 mm)

Features

- Ultra low power dissipation:
  - I_{CC} = 0.3 µA at T_A = 125 °C
- Low on-resistance:
  - $R_{DS(on)}$ = 4 Ω (T_A = 25 °C) at V_{CC} = 3.0 V
- Wide operating voltage range:
  - V_{CC} (opr) = 1.65 V to 5 V single supply
- 5 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 V to 3.0 V
- Typical bandwidth (-3 dB) at 800 MHz on all channels
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance exceeds JESD22
  - 2000-V human body model (A114-A)
- USB (2.0) high speed (480 Mbps) signal switching compliant

Description

The STG3693 is a high-speed CMOS low voltage quad analog SPDT (single pole dual throw) switch or 2:1 multiplexer /demultiplexer switch fabricated in silicon gate C2MOS technology. It is designed to operate from 1.65 V to 5 V, making this device ideal for portable applications.

The nSEL inputs are provided to control the switch. The switch S1 is ON (it is connected to common ports Dn) when the nSEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (it is connected to common port D) when the nSEL input is held low and OFF (high impedance state exists between the two ports) when nSEL is held high. Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Product status link
STG3693

Product summary	
Order code	STG3693QTR
PackageQFN16L	QFN16L (2.6x1.8 mm)
Packing	Tape and reel

4.2 Construction note

	New Plant Qualification **P/N** STG3693QTR
Wafer/Die fab. information	
Wafer fab manufacturing location	USIF
Process family	HCMOS6
Die finishing back side	Raw Silicon - Back Grinding
Die size	1180x 820 µm²
Bond pad metallization layers	Ti/AlCu 0.918 µm
Passivation type	PSG + NITRIDE
Wafer Testing (EWS) information	
Electrical testing manufacturing location	
Tester	
Test program	
Assembly information	
Assembly site	UTL3
Package description	VFQFPN16
Molding compound	G770HCD
Frame material	QFN 16L 2.6 x 1.8 mm NiPdAu (Paddle)
Die attach process	Glue
Die attach material	8006NS epoxy
Die pad size	76 x 76 µm
Wire bonding process	Wire
Wires bonding materials/diameters	1.0 mils Au
Lead finishing process	NiPdAu Pre-plated
Lead finishing/bump solder material	NiPdAu Pre-plated
Final testing information	
Testing location	UTAC Thai Limited
Tester	
Test program	

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	LC916005	1C365780	FN14400B	VFQFPN16	V52601	LL WB PARAMETER
2	LC916005	1C365790	FN14400B	VFQFPN16	V52601	NN WB PARAMETER
3	LC916005	1C365800	FN14400B	VFQFPN16	V52601	HH WB PARAMETER

Detailed results in below chapter will refer to P/N and Lot #.

5.2 Test plan and results summary

P/N:STG3693QTR

Package Oriented Tests									
PC		JESD22 A-113	Drying 24 H @ 125°C Store 192 H @ Ta=30°C Rh=60% Over Reflow @ Tpeak=260°C 3 times		Final	**0/180**	**0/180**	**0/180**	No delam Pre and Post PC (40 parts)
uHAST	Y	JESD22 A-118	T°=130°C; Pressure=2.3 atm; HR=85%		96 H	**0/80**	**0/80**	**0/80**	No delam Post trial (22 parts)
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		500 cy	**0/80**	**0/80**	**0/80**	No delam Post trial (22 parts)
					1000 cy				ongoing
HTSL	Y	JESD22 A103	TA ≥ 150°C		168 H	**0/80**	**0/80**	**0/80**	
					500 H	**0/80**	**0/80**	**0/80**	DPA ongoing 5 parts/lot
					1000 H	**0/80**	**0/80**	**0/80**	
Other Tests									
SD	N	JESD22-B-102	Solderability		15	**PASS**	**PASS**	**PASS**	
BPS	N	MIL – STD683	Bond Pull Strength		30 bonds / 5 devices	**PASS**	**PASS**	**PASS**	
BS	N	AECQ100 - 001	Bond shear strength		30 bonds / 5 devices	**PASS**	**PASS**	**PASS**	

In case of rejects include a short description of the failure analysis and corrective actions.

Die Oriented		
HTOL Higt Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.