

PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data

1.1 Company		STMicroelectronics International N.V
1.2 PCN No.		AMS/21/13153
1.3 Title of PCN		Power Management BU: Alternative die for TL431AIL3T and TL432AIL3T
1.4 Product Category		See product list
1.5 Issue date		2021-12-20

2. PCN Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Salvatore DI VINCENZO
2.1.3 Quality Manager	Giuseppe LISI

3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Die redesign: Mask or mask set change with new die design - Design changes in active elements.	Front end plant : ST Singapore

4. Description of change

	Old	New
4.1 Description	Mask Set 0431H rev B	Mask Set M431A rev A
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	Yield Improvements. No impact on Quality and Reliability Characteristics on final product	

5. Reason / motivation for change

5.1 Motivation	Following ST's commitment toward a continuous improvement philosophy, we are pleased to announce the introduction of an alternative die, using the same technology (HBIP40) and same wafer fab (ST AMK Singapore) for the Voltage references TL431AIL3T and TL432AIL3T. This change will increase our manufacturing flexibility and allow us to improve our customer delivery support.
5.2 Customer Benefit	MANUFACTURING FLEXIBILITY

6. Marking of parts / traceability of change

6.1 Description	The traceability of the new parts will be ensured by different internal codification and QA number
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7. Timing / schedule

7.1 Date of qualification results	2021-12-03
7.2 Intended start of delivery	2022-03-25
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation

8.1 Description	13153 W1258-2020-TL431 SOT23 3L.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-12-20

9. Attachments (additional documentations)

13153 Public product.pdf
13153 W1258-2020-TL431 SOT23 3L.pdf

10. Affected parts

10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	TL431AIL3T	
	TL432AIL3T	

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Public Products List

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PCN Title : Power Management BU: Alternative die for TL431AIL3T and TL432AIL3T

PCN Reference : AMS/21/13153

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

TL431AIL3T	TL432AIL3T	
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AMS (Analog, MEMS & Sensor Group)

General Purpose Analog & RF Division

Power Management
Quality and Reliability

REL.6088-1258-2020.W

Reliability

Voltage References

New Product qualification

TL431BL3T

M43101 Line
Technology HBIP40V
Package SOT23 3 L

General Information		Locations	
Product Lines	<i>M43101</i>	Wafer fab	<i>Singapore 6</i>
Product Description	Programmable voltage reference	Assembly plant	<i>Carsen / Shenzhen</i>
P/N	TL431BL3T	Reliability Lab	<i>Catania Reliability LAB</i>
Product Group	<i>AMG</i>		
Product division	<i>General Purpose Analog & RF Division</i>		
Package	<i>SOT23 3 L / SO8</i>		
Silicon Process technology	<i>HBIP40</i>		

DOCUMENT INFORMATION

Version	Date	Pages	Handled by	Approved by	Comment
1	August 2020	6	Angelo.Basile	Giuseppe Giacopello	Final Report



AMS (Analog, MEMS & Sensor Group)

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Power Management
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Power Management
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW OBJECTIVES

To qualify the New Product TL431BL3T

4 CONCLUSION

The present reliability results are positive.

5 DEVICE CHARACTERISTIC

5.1 Device description

The TL431 is an adjustable shunt voltage reference with guaranteed temperature stability over the entire operating temperature range .the operating output voltage may be set any value between 2.5 and 36V with two impedanca external resistors.The TL431operates with a wide current range from 1 to 100mA with a typical dynamic impedance of 0.2

5.2 Construction note

P/N	TL431	
Wafer/Die fab. information		
Wafer fab manufacturing location	Singapore AMK6	
Technology	HBIP40V	
Die finishing back side	Lapped Silicon	
Die size	830 x 780 micron	
Wafer Passivation type	PVAPOX-NITRIDE	
Assembly information		
Assembly Site	Carsem M	SHENZHEN B/E
Package description	SOT23 3 L	SO8
Molding compound	Epoxy	Epoxy
Frame	HDLF NiPdAu	NiThPdAgAu
Die attach material	Epoxy	Epoxy
Wires bonding materials/diameters	1 mils Cu	1 mils Cu
Final testing information		
Testing location	Carsem S	SHENZHEN B/E
Tester	ASL1000	
Test program	M431 1	M431_STS_01

6 TEST VEHICLE & TEST PLAN

Lot #	Diffusion Lot	Assy Lot	Package	Product Line	Comments
1	V6010VYY	E016A11	SOT23 3L	M43101	
2	6208FFJH32	9Y233ADH	SOT23 3L		
3	60197XV	GK2320LN	SO8	M43101	

Test	PC	Std ref.	Conditions	Steps	Failure/SS			Generic Data For Voltage Reference
					1° Lot SOT23-3L	2° Lot SOT23-3L	3° Lot SO8	
Silicon related								
HTOL	N	JESD22 A-108	T _j = 125° C, V _{bias} =+5V	77	168 h	0/77		0/77
					500 h	0/77		0/77
					1000 h	0/77		0/77
HTSL	N	JESD22 A-103	Ta = 150° C	45	168 h	0/45	0/45	0/45
					500 h	0/45	0/45	0/45
					1000 h	0/45	0/45	0/45
Package related								
PC		JESD22 A-113	Driving 24 h @125°C store 168h @ Ta=85°C Rh = 85 % Oven Reflow @ Tpeak=260°C 3 times	231	Final	PASS	PASS	PASS
AC	Y	JESD22 A-102	Ta = 121°C, Pa = 2 Atm	77	168h	0/77	0/77	0/77
						0/77	0/77	0/77
						0/77	0/77	0/77
TC	Y	JESD22 A-104	Ta = -65° C to 150° C	77	100 cy	0/77	0/77	0/77
					0/77	0/77	0/77	
					0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85° C, RH = 85%, V _{bias} =+2.5V	77	168 h	0/77	0/77	0/77
					0/77	0/77	0/77	
					0/77	0/77	0/77	
Other Tests								
ESD	N	JESD22-A114	HBM	3	2KV		PASS	
		JESD22-C101	CDM	3	1.5KV			

Note: All samples are assembly on dedicated PCB in agreement with JEDEC020

7 TEST DESCRIPTION

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other Test		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model HBM: Human Body Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.