PRODUCT / PROCESS CHANGE INFORMATION

1. PCI basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCI No.	AMS/21/13120
1.3 Title of PCI	Change of ASIC EWS Test platform from C372 to DOT100 for the selected products.
1.4 Product Category	See products list.
1.5 Issue date	2021-11-19

2. PCI Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Andrea Mario ONETTI
2.1.2 Marketing Manager	Simone FERRI
2.1.3 Quality Manager	Michele CALDERONI

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Equipment (EWS-FT)	New tester, or prober option or major HW changes (ex: computer), brand or model (Unknown type)	ST Catania

4. Description of change		
	Old	New
4.1 Description	SPEA C372 as EWS Test Platform	SPEA DOT 100 as EWS Test Platform
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change	
5.1 Motivation	The C372 is an old model, no longer well supported by the vendor. Additionally, the DOT100 will significantly increase the EWS throughput capability.
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change	
6.1 Description	Internal Trace code

7. Timing / schedule	
7.1 Date of qualification results	2021-11-03
7.2 Intended start of delivery	2021-12-13
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13120 V683AA4_Report_03112021.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-11-19

9. Attachments (additional documentations)
13120 Public product.pdf 13120 V683AA4_Report_03112021.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	AIS328DQTR	
	IIS328DQTR	

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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCI Title : Change of ASIC EWS Test platform from C372 to DOT100 for the selected products.

PCI Reference : AMS/21/13120

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

AIS328DQTR	IIS328DQTR	

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AIS328DQ / IIS328DQ:

ASIC wafer testing porting from SPEA C372 to SPEA DOT100

A. Di Martino/ Marco Morezzi

03 Nov 2021

Reason of the change

- SPEA C372 are old testers.
- They have been in production since 1998 and the supplier (SPEA) cannot fully guarantee adequate support in case of tester problems.
- Due to equipment obsolescence, ST is moving the ASIC EWS test platform used in the product AIS328DQTR (internal line code V683) based on SPEA C372 to the new one based on SPEA DOT100.
- The tester DOT100 has been in production at ST for several years and it is used already for several other products, including some used in the Automotive domain
- With the new equipment there is also a significant increase of testing throughput
- **Traceability of the change will be done providing the QA number of the first shipment**

- **The following slides show that the electrical results using the two tester models are equivalent**

*EWS: Electrical Wafer Sorting

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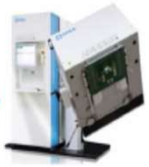
Production flow and plants involved in the change

TESTER upgrade:
from SPEA C372
to SPEA DOT100



MEMS/ASIC
DIFFUSION
ST Crolles

MEMS/SENSOR
DIFFUSION
ST Agrate

MEMS/ASIC
EWS TEST
ST Catania

MEMS/SENSOR
EWS TEST
ST Agrate

ASSEMBLY
ASE

FINAL TEST and
FINISHING
ST Malta

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5M/1E change analysis

Change	Element	Control	Remarks
EWS ASIC testing platform change	**Machine**	Old tester : C372 from SPEA	New tester: DOT100 from SPEA
	Man	EWS plant and operators: ST Catania	No change
	Material	Bill of material (BOM)	No change
	Measurement	The testing program is simply transferred from the old to the new tester	No change
	Method	The testing flow is unchanged: EWS1 @ambient + EWS2 @ambient + EWS3 @cold	No change
	Environment	ST plant in Catania is fully qualified for automotive production	No change

Qualification plan : wafer correlation and validation

According ZVEI governance matrix qualification is done comparing electrical results before and after the change (refer to DeQuMa)

- Lot ID: J121XNM-24
  - One full wafer (#24)
  - Gross number of dies: 6731

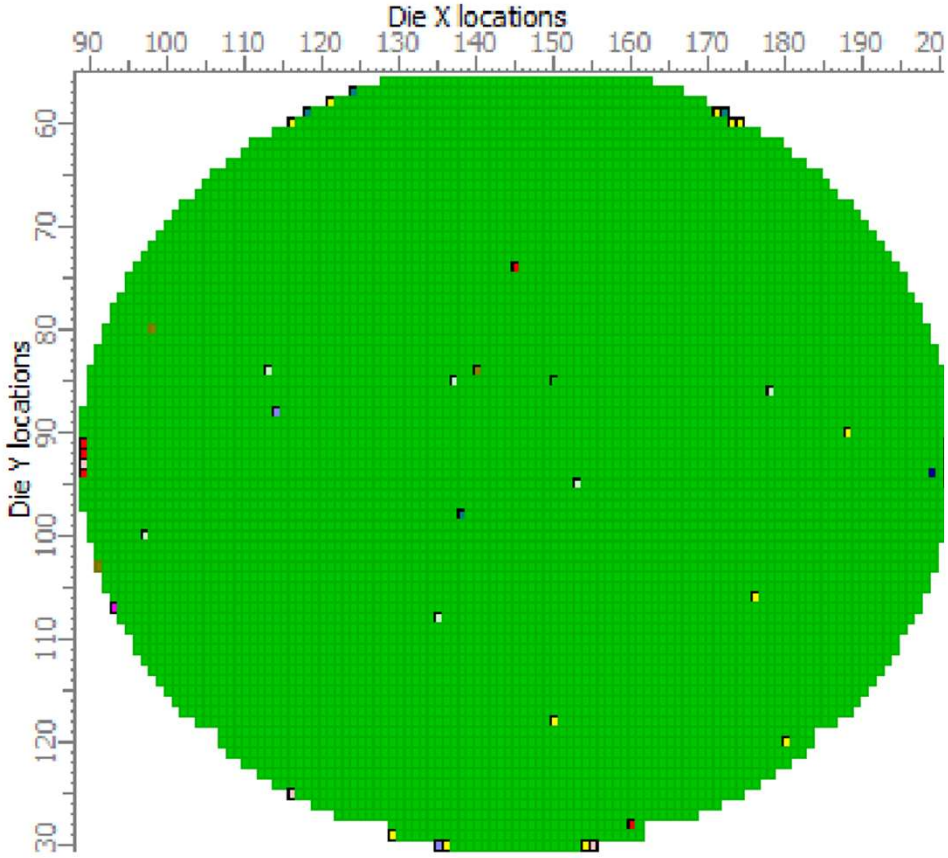
- Testing flow:
  - EWS1@T_{amb} ➔ EWS2@ T_{amb} ➔ EWS3@T_{cold} =-40°C
  - Vdd settings:
    - Vdd_Min = 1.71V
    - Vdd_Cal = 2.5V
    - Vdd_Max= 3.6V

- Method: the wafer #24 is first tested on C372, and then on DOT100

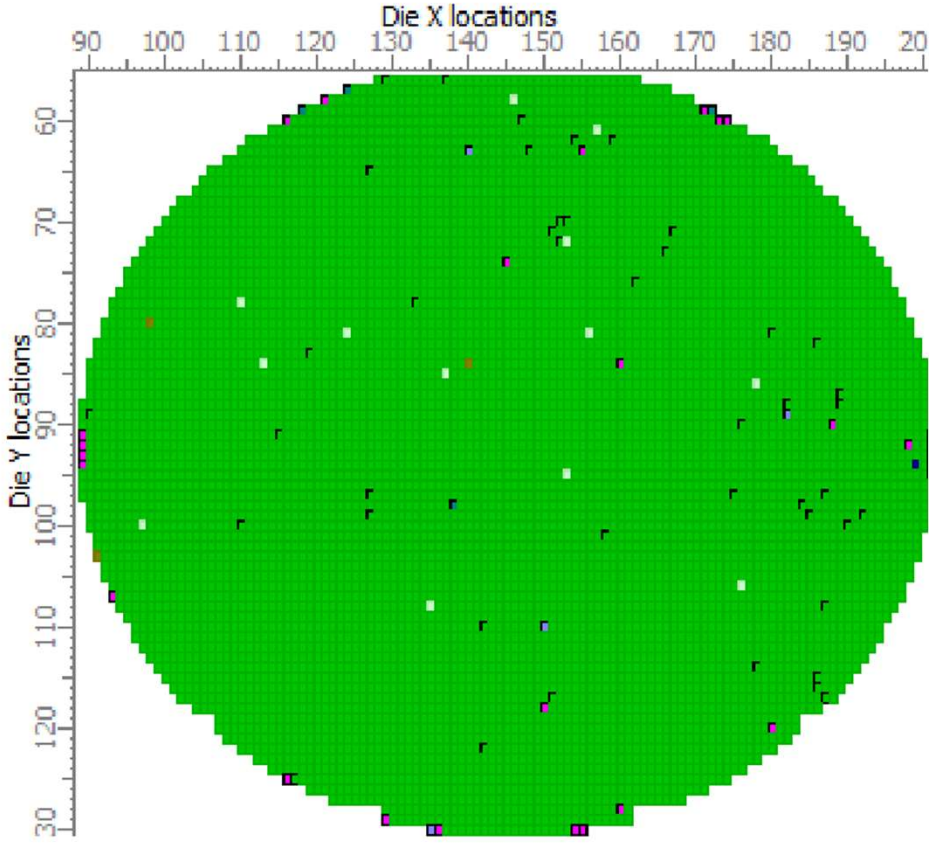
- Purpose: the EWS results are compared to validate the change

Maps of EWS1@T_{amb}

C372



DOT100



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EWS1: Bin Pareto

Group name : C372

Software Binning	Bin Name	Count	Percentage	Software Binning Chart
1	Good	6689	99.4 %	
3	I2C–SPI_Functional	17	0.3 %	
8	ATP_Scan	6	0.1 %	
2	Supply Current	5	0.1 %	
6	Short	4	0.1 %	
9	Erase Flash	3	0.0 %	
7	Inp/Out Resistance	3	0.0 %	
5	Open	2	0.0 %	
4	Leakages	1	0.0 %	
11	Read Flash	1	0.0 %	
Cumul.	Cumul.	6731	100.0%	

On DOT, the bins 2, 3, 4, 7 are grouped in the leakage task with bin 4

Group name : DOT

Software Binning	Bin Name	Count	Percentage	Software Binning Chart
1	Pass	6678	99.2 %	
4	Leakages	27	0.4 %	
8	Scan Test	13	0.2 %	
5	Open	5	0.1 %	
6	Short	4	0.1 %	
9	Erase Flash	3	0.0 %	
11	Read Flash	1	0.0 %	
Cumul.	Cumul.	6731	100.0%	

EWS1: DIE TO DIE ANALYSIS

Delta yield binning pareto: Pass to Fail

C372 – Wafer: J121XNM-24B1	DOT – Wafer: J121XNM-24B1	Frequency (#)	Frequency (% of common dies)
1	4	3	0.04%
1	5	3	0.04%
1	8	6	0.09%
Total	–	12	0.18%

Delta yield binning pareto: Fail to Pass

C372 – Wafer: J121XNM-24B1	DOT – Wafer: J121XNM-24B1	Frequency (#)	Frequency (% of common dies)
5	1	1	0.01%
Total	–	1	0.01%

Open-short false rejects ➔ Contact issue

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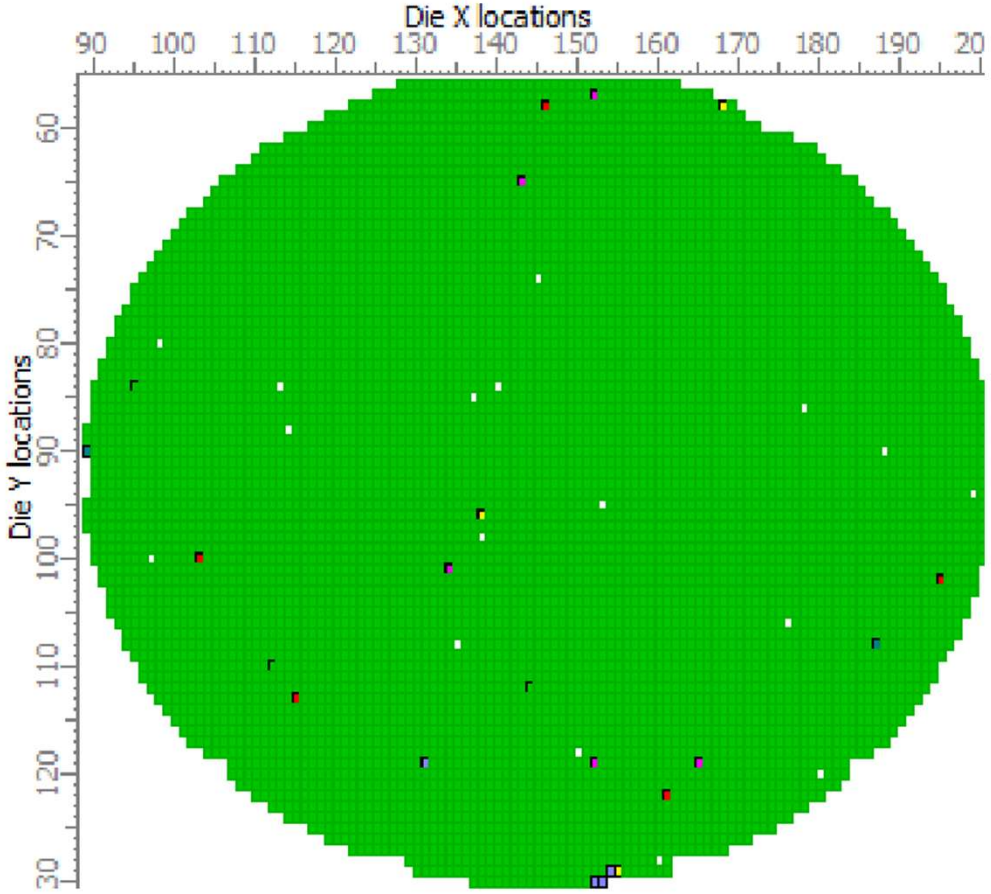
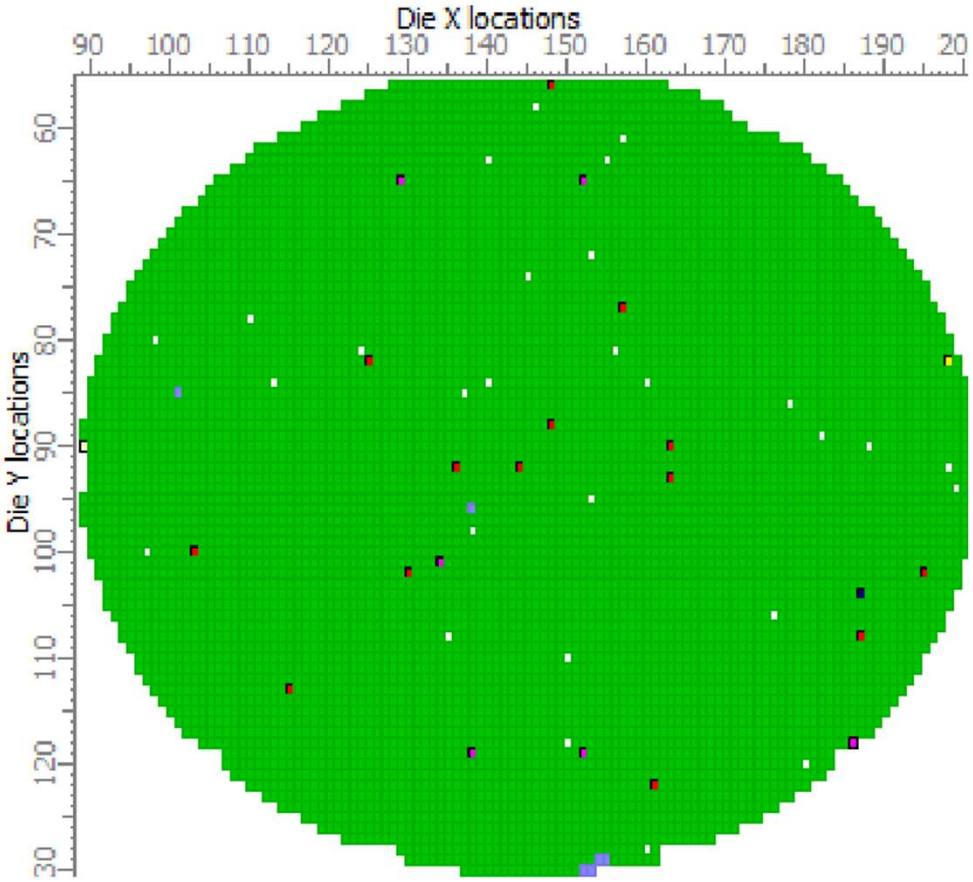
Maps of EWS2@T_{amb}

C372



DOT100



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EWS2 Bin Pareto

Group name : C372

Software Binning	Bin Name	Count	Percentage	Software Binning Chart
1	Good	6670	99.7 %	
15	30KFrequency_Trim	5	0.1 %	
2	Supply Current	5	0.1 %	
17	ADC_Trim	4	0.1 %	
13	Current_Trim	3	0.0 %	
20	Ews_Sk12	2	0.0 %	
Cumul.	Cumul.	6689	100.0%	

Group name : DOT

Software Binning	Bin Name	Count	Percentage	Software Binning Chart
1	Pass	6649	99.6 %	
2	Supply Current	14	0.2 %	
17	ADC_Trim	6	0.1 %	
15	30KFrequency_Trim	6	0.1 %	
13	Current_Trim	1	0.0 %	
5	Open	1	0.0 %	
18	Voltage_Reference	1	0.0 %	
Cumul.	Cumul.	6678	100.0%	

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EWS2: DIE TO DIE ANALYSIS

Delta yield binning pareto: Pass to Fail

C372 – Wafer: J121XNM–24B1	DOT – Wafer: J121XNM–24B1	Frequency (#)	Frequency (% of common dies)
1	17	1	0.01%
1	13	1	0.01%
1	5	1	0.01%
1	15	4	0.06%
1	2	9	0.13%
Total	–	16	0.24%

Delta yield binning pareto: Fail to Pass

C372 – Wafer: J121XNM–24B1	DOT – Wafer: J121XNM–24B1	Frequency (#)	Frequency (% of common dies)
17	1	1	0.01%
13	1	1	0.01%
15	1	3	0.04%
Total	–	5	0.07%

Contact issue. Not confirmed after re-probing done on C372 by Product Engineering in Eng Mode retesting the die one by one

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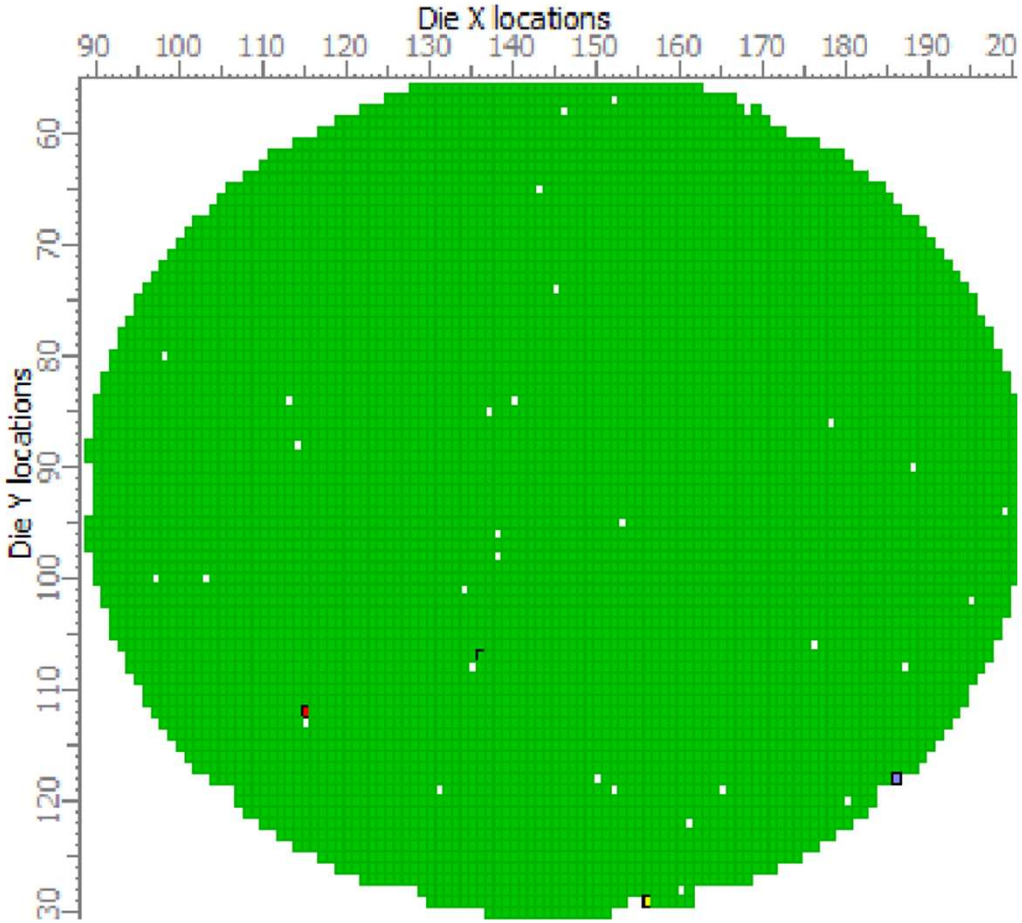
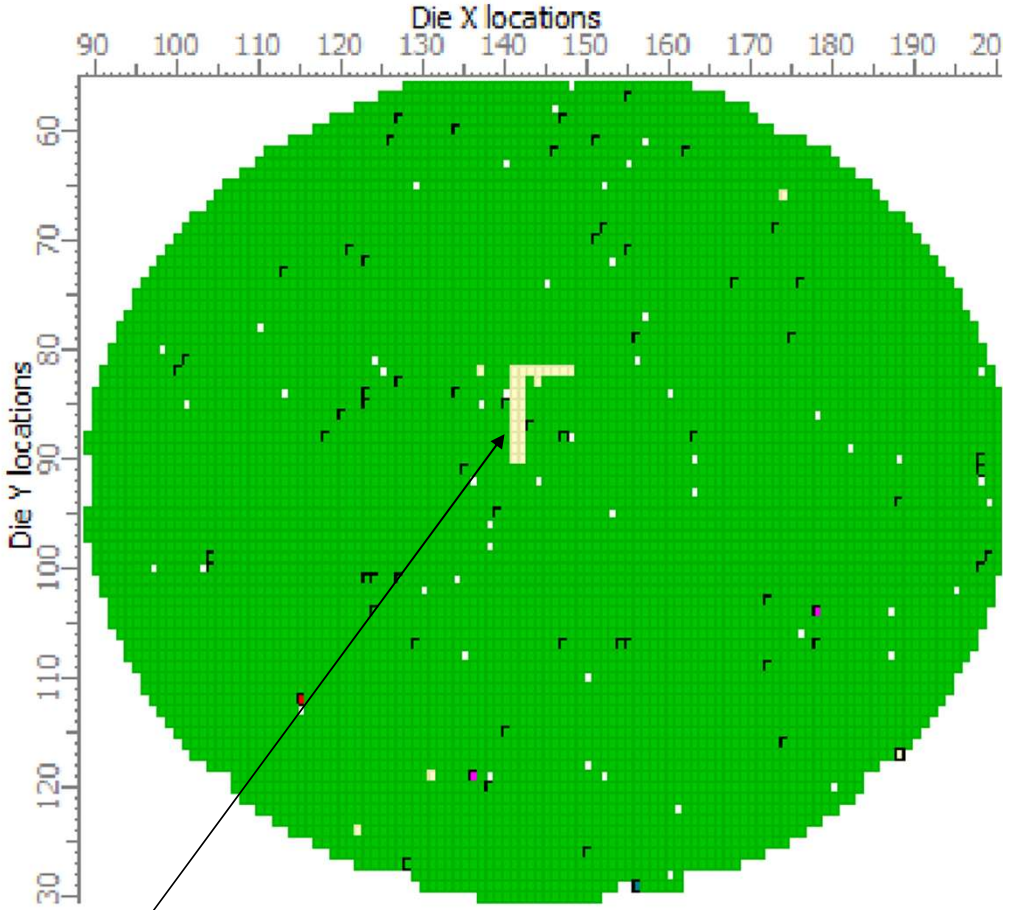
Maps of EWS3@T_{cold}

C372



DOT100



Failure due to setup

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EWS3 Bin Pareto

Group name : C372

Software Binning	Bin Name	Count	Percentage	Software Binning Chart
1	Good	6667	100.0 %	
15	30KFrequency_Trim	1	0.0 %	
3	I2C-SPI_Functional	1	0.0 %	
2	Supply Current	1	0.0 %	
Cumul.	Cumul.	6670	100.0%	

Group name : DOT

Software Binning	Bin Name	Count	Percentage	Software Binning Chart
1	Pass	6615	99.5 %	
4	Leakages	27	0.4 %	
17	ADC_Trim	2	0.0 %	
5	Open	2	0.0 %	
13	Current_Trim	1	0.0 %	
2	Supply Current	1	0.0 %	
18	Voltage_Reference	1	0.0 %	
Cumul.	Cumul.	6649	100.0%	

25 false rejects generated during setup

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EWS3: DIE TO DIE ANALYSIS

Delta yield binning pareto: Pass to Fail

C372 – Wafer: J121XNM–24B1	DOT – Wafer: J121XNM–24B1	Frequency (#)	Frequency (% of common dies)
1	13	1	0.02%
1	17	1	0.02%
1	5	2	0.03%
1	4	27	0.41%
Total	–	31	0.47%

Delta yield binning pareto: Fail to Pass

No dies for this section!!

25 false rejects generated during setup

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Traceability

- There won’t be a dedicated finished good (FG) to track this change
- The traceability will be granted by Date Code/QA number of the first shipment
- Lots with Date Codes after first shipment will be already embedding the change

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Conclusions

- The EWS results of a complete wafer of V683 (ASIC die code used in AIS328DQ and IIS328DQ) were compared after testing on current and new equipment
- The wafer maps, after contact verification and re-probing on the old C372, proved to be perfectly correlated
- Overall, the wafer testing solution implemented on the new DOT100 is also providing a higher throughput capability

- The wafer testing program is confirmed to be validated and qualified on the new DOT100 platform

Thank you

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