PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	AMS/21/12927
1.3 Title of PCN	Transfer from UMC to Crolles Wafer fab with redesign of STG3692 and STG3856
1.4 Product Category	See product list
1.5 Issue date	2021-07-19

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Lionel GRILLO
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication	Wafer fab : ST Crolles (France)

4. Description of change		
	Old	New
4.1 Description	Wafer Fab : - UMC (Taiwan) Process : - HCMOS6	Wafer Fab : - ST Crolles (France) Process : - HCMOS7
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	Progressing on the activities related to quality continuous improvement, and production rationalization ST is glad to announce redesign of STG3856 and STG3692 products in HCMOS7 technology (currently HCMOS6)
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	New finished good codes

7. Timing / schedule	
7.1 Date of qualification results	2021-07-15
7.2 Intended start of delivery	2021-10-30
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	12927 STG in HCMO7.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-07-19

9. Attachments (additional documentations)
12927 Public product.pdf 12927 STG in HCMO7.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STG3692QTR	
	STG3856QTR	

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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Transfer from UMC to Crolles Wafer fab with redesign of STG3692 and STG3856

PCN Reference : AMS/21/12927

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STG3856QTR	STG3692QTR	

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PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/21/12927

Analog, MEMS & Sensors (AMS)

Transfer from UMC to Crolles Wafer fab with redesign of STG3692 and STG3856

WHAT:

Progressing on the activities related to quality continuous improvement, and production rationalization ST is glad to announce redesign of STG3856 and STG3692 products in HCMOS7 technology (currently HCMOS6)

Please find more information related to material change in the table here below

Material	Current process	Modified process	Comment
Diffusion location	UMC Taiwan	ST Crolles	
Process	HCMOS6	HCMOS7	
Assembly location	Amkor Philippine, UTAC Thailand	Amkor Philippine, UTAC Thailand	No change
Bill of material assembly	No change	No change	No change
Datasheet	See modification page21		

WHY:
This change will contribute to ST's continuous quality product improvement and production rationalization

HOW:
The qualification program consists mainly of comparative electrical characterization and reliability tests.

You will find here after the qualification test plan which summarizes the various test methods and conditions that ST uses for this qualification program.

WHEN:
The new material set will be implemented in Q3/2021 in ST Crolles.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.

There is -as well- no change in the packing process or in the standard delivery quantities.
Shipments may start earlier with the customer's written agreement.

Reliability Evaluation Report

STG3692 , STG3856

Reliability Evaluation Purpose

General Information	
Commercial Product	*: STG3692QTR, STG3856QTR*
Product Line	*: VB2R14, VB2X14*
Product Description	*: Low voltage high BW quad SPDT switch, Low voltage 1.0 Ω max dual SP3T switch with break-before-make feature*
Package	*: QFN16L , QFN 12L*
Silicon Technology	*: HCMOS7A*
Division	*: General purpose Analog*

Traceability	
Diffusion Plant	*: Crolles 200*
Assembly Plant	*: UTAC*

Reliability Assessment	
Pass	☒
Fail	☐
Investigation required	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

The objective of this qualification is to qualify as an industrial product, the transfer from HCMOS6 to HCMOS7A the low-voltage, high bandwidth quad SPDT, from Crolles 200 plant.
The package under qualification is the QFN16L, from UTAC plant.
The qualification plan is based on the similarity analysis with HCMOS6 counterpart on FE side, and with other STG products on BE side (QBS), using the Jedec/AEC-Q100 specifications.

1.2 Reliability Strategy and Test Plan

Reliability trials performed as part of this reliability evaluation are in agreement with **ST 0061692** specification and are listed in below Test Plan. For details on test conditions, generic data used and specifications references, refer to test results summary in section 4.

As specified in the previous section, STG3692 and STG3856 dice are converted from H6 to H7A technology. Furthermore, STG3692 and STG3856 product shares the same BOM on BE side as other STG products (STG3693, STG3856).

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.
Parameter drift analysis performed on samples submitted to die oriented test showed a good stability of the main electrical monitored parameters.
Package oriented tests have not put in evidence any criticality.
ESD & Latch-Up are in accordance with ST specifications.

Based on the overall results obtained, STG3692QTR and STG3856 product diffused in HCMOS7A (Crolles 200) and assembled in QFN16L and QFN 12L (UTAC) , have positively passed reliability evaluation performed in agreement to Jedec specification.

2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

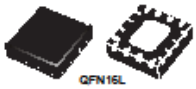
2.1 Generalities

life.augmented

STG3692

Datasheet

Low voltage high bandwidth quad SPDT switch



QFN16L
(2.6x1.8 mm)

Features

- Ultra low power dissipation:
  - I_{CC} = 0.2 µA at T_A = 85 °C
- Low on-resistance:
  - $R_{DS(on)}$ = 4.6 Ω (T_A = 25 °C) at V_{CC} = 4.3 V
  - $R_{DS(on)}$ = 5.8 Ω (T_A = 25 °C) at V_{CC} = 3.0 V
- Wide operating voltage range:
  - V_{CC} (opr) = 1.65 V to 4.3 V single supply
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 V to 3.0 V
- Typical bandwidth (-3 dB) at 800 MHz on all channels
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance exceeds JESD22
  - 2000-V human body model (A114-A)
- USB (2.0) high speed (480 Mbps) signal switching compliant

Description

The STG3692 is a high-speed CMOS low voltage quad analog SPDT (single pole dual throw) switch or 2:1 multiplexer /demultiplexer switch developed in silicon gate C2MOS technology. It is designed to operate from 1.65 V to 4.3 V, making this device ideal for portable applications.

The nSEL inputs are provided to control the switch. The switch S1 is ON (connected to common ports Dn) when the nSEL input is held high and OFF (high impedance state exists between the two ports) when SEL is held low; the switch S2 is ON (connected to common port D) when the nSEL input is held low and OFF (high impedance state exists between the two ports) when nSEL is held high. Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Product status link
STG3692

Product summary	
Order code	STG3692QTR
Package	QFN16L (2.6x1.8 mm)
Packing	Tape and reel

STG3856

Low voltage 1.0 Ω max dual SP3T switch with break-before-make feature

Features

- High speed:
  - t_{PD} = 0.3 ns (typ.) at V_{CC} = 3.0 V
  - t_{PD} = 0.4 ns (typ.) at V_{CC} = 2.3 V
- Ultra low power dissipation:
  - I_{CC} = 0.2 µA (max.) at T_A = 85°C
- Low ON resistance V_{IN} = 0 V:
  - R_{ON} = 1.0 Ω (max. T_A = 25°C) at V_{CC} = 4.3 V
  - R_{ON} = 1.5 Ω (max. T_A = 25°C) at V_{CC} = 3.0 V
  - R_{ON} = 1.8 Ω (max. T_A = 25°C) at V_{CC} = 2.3 V
- Wide operating voltage range:
  - V_{CC} (opr) = 1.65 V to 4.3 V single supply
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 to 4.3 V
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance (analog channel vs. GND): HBM > 2 kV (MIL STD 883 method 3015)

QFN12L

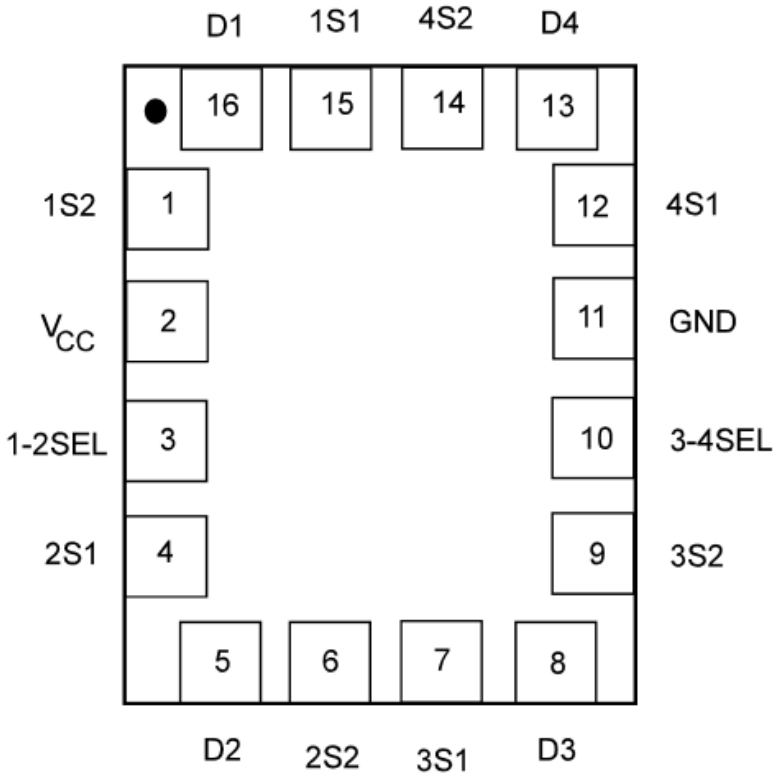
Description

The STG3856 is a high-speed CMOS low voltage dual analog SP3T (single pole triple throw) switch or dual 3 : 1 multiplexer /demultiplexer switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65 V to 4.3 V, making this device ideal for portable applications.

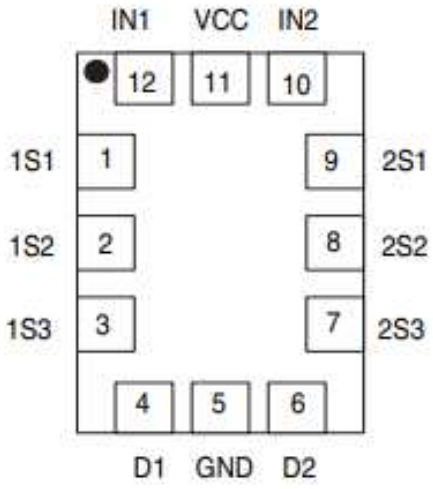
The device offers very low ON resistance (< 1.0 Ω) at V_{CC} = 4.3 V. The disabling and enabling of switches are done by setting the 1IN and 2IN control pins. Additional key features are fast switching speed, and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

2.2 Pin connection

STG3692



STG3856



2.3 Block diagram

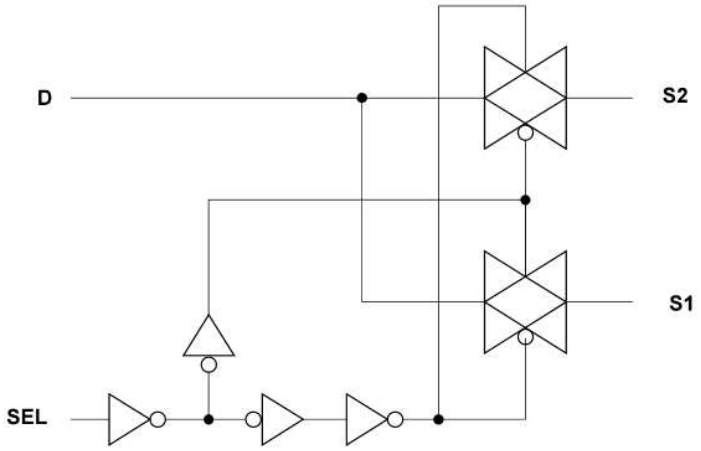
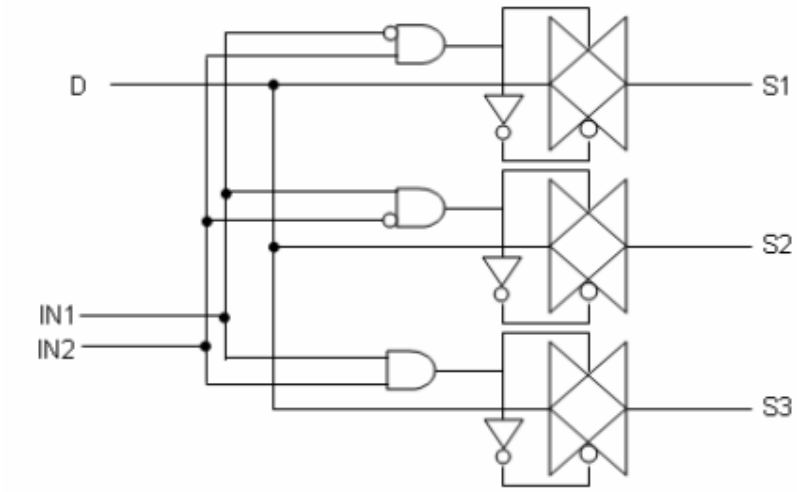


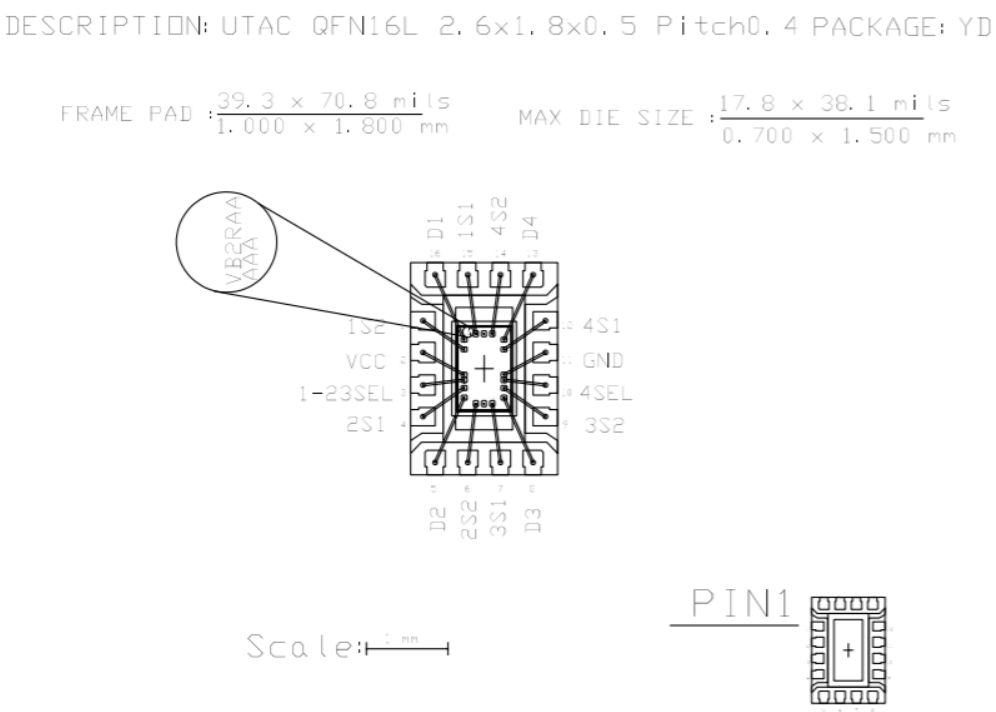
Table 2. Truth table

SEL	SWITCH S1	SWITCH S2
H	ON	OFF(1)
L	OFF(1)	ON

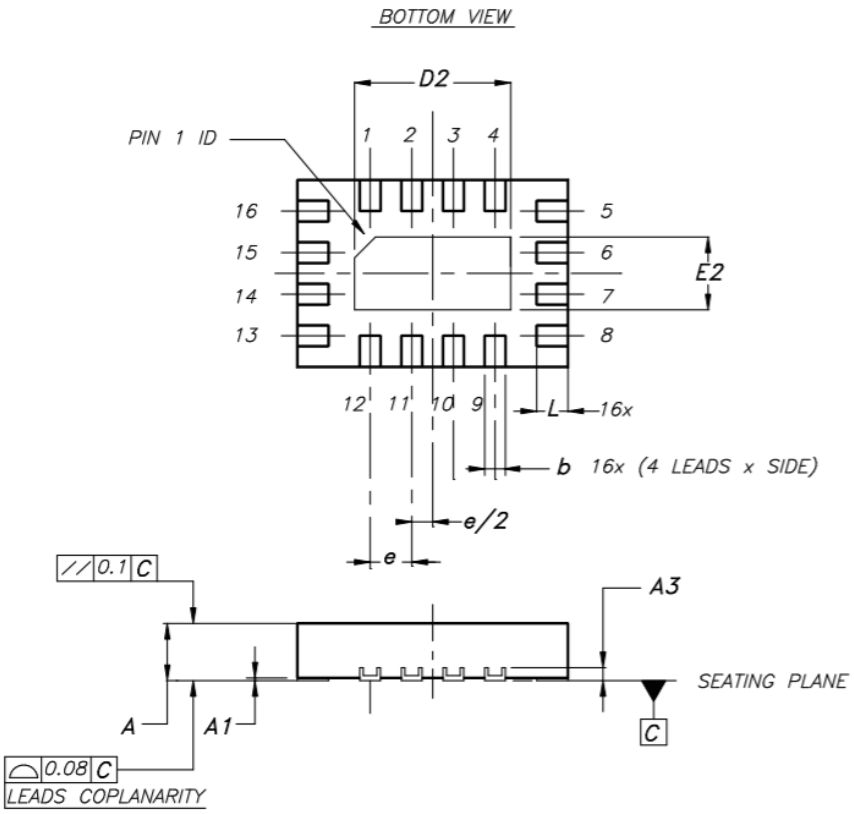
1. *High impedance*



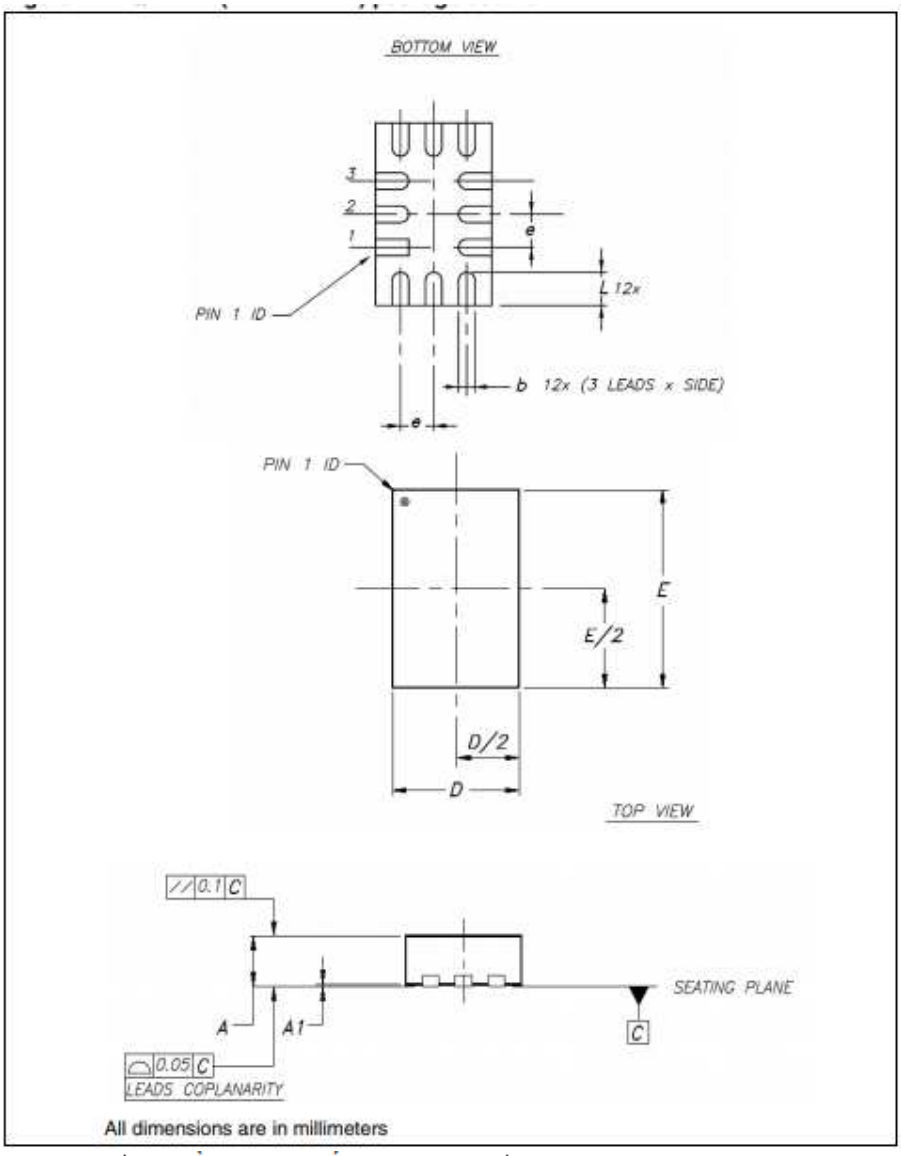
2.4 Bonding diagram (DM00670990)



2.5 Package Outline / Mechanical data (7957177)



DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A	0.50	0.45	0.55	
A1	0.02	0	0.05	
A3	0.127			
b	0.20	0.15	0.25	
D	2.60	2.55	2.65	
D2	1.50	1.45	1.55	
E	1.80	1.75	1.85	
E2	0.70	0.65	0.75	
e	0.40			
L	0.30	0.25	0.35	



All dimensions are in millimeters

Symbol	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.60	0.019	0.021	0.023
A1	0	0.02	0.05	0	0.001	0.002
b	0.15	0.20	0.25	0.006	0.007	0.010
D	1.30	1.40	1.50	0.051	0.055	0.059
E	2.10	2.20	2.30	0.082	0.086	0.090
e		0.40			0.015	
L	0.35	0.40	0.45	0.013	0.015	0.017

2.6 Traceability

2.6.1 Wafer fab information

Wafer fab information		
	STG3692	**STG3856**
Wafer fab name / location	Crolles 200 (CROF)	Crolles 200 (CROF)
Wafer diameter (inches)	8	8
Wafer thickness	725 +/- 25µm	725 +/- 25µm
Silicon process technology	HCMOS7A	HCMOS7A
Number of masks	23	23
Die finishing front side (passivation) materials/thicknesses	PSG + Nitride	PSG + Nitride
Die finishing back side Materials/thicknesses	Raw silicon	Raw silicon
Die area (Stepping die size)	1158*790µm²	800x1600µm²
Die pad size	60*73µm²	60*73µm²
Scribe Line size	100*100µm	100*100µm
Last metal level/Materials/Thicknesses	M4: AlCu @2.5µm	M4: AlCu @2.5µm

2.6.2 Assembly information

Assembly Information		
Package description	**STG3692**	**STG3856**
Assembly plant name / location	UTAC (997G)	UTAC (997G)
Package code description	QFN16L	QFN12L
Pitch	0.65	0.4
Die thickness after back-grinding	127 +/- 12.7µm	127 +/- 12.7µm
Die sawing method	Blade	Blade
Bill of Material elements	See below	See below
Lead frame/Substrate material/supplier/reference	16L UQFN 1.8x2.6/0.4mm Pitch	VFQFPN-12 2.2x1.4x0.55 PITCH 0.4
Lead frame finishing (materials)	Precious metals (Ag, Au, NiPdAu)	Precious metals (Ag, Au, NiPdAu)
Die attach material/type(glue/film)/supplier	Glue, Ablestik 8006NS	Glue, Ablestik 8006NS
Wire bonding material/diameter/supplier	Au @1mil	Au @0.8mil
Molding compound material/supplier/reference	RESIN SUMITOMO G770HCD	RESIN SUMITOMO G770HCD
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL1	MSL1

2.6.3 Reliability testing information

Reliability Testing Information	
Accelerated lifetime simulation tests	
Reliability laboratory name / location	*GRAL, Grenoble*
Electrical testing location (internal)	*Grenoble*
Tester	*ASL1K*
Accelerated environment stress tests	
Reliability laboratory name / location	*GRAL, Grenoble*
Electrical testing location (internal)	*Grenoble*
Tester	*ASL1K*

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Lot #	Die Revision (Cut)	Raw Line	Note
1	1.0	ANYD*VB2RBBJ	STG3692QTR$NA
2	1.0	AN5T*VB2XAAJ	STG3856QTR$NA

3.2 Test results summary

Electrical Testing Temperature and Physical Analysis required by STM requirements are reported in the table below in Test Conditions column.

Test method revision reference is the one active at the date of reliability trial execution.

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS

Test	#	Reference	Q100/STM Test Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments (N/A =Not Applicable)
PC	A1	JESD22 A113 J-STD-020	24h bake@125°C, MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C ☐ **Testing at Room *(pre)*** ☐ Testing at Cold *(pre)* ☐ Testing at Hot *(pre)* ☐ 100 Temperature Cycles *(pre)* ☒ **C/T-SAM *(pre / post)*** ☐ Cross section	Performed before uHAST & TC trials			Lot 1: 0 / 231 Lot 1: 0 / 231	
THB	A2	JESD22 A101	Ta=85°C, 85%RH, Duration= 1000hrs ☐ **After PC** ☒ **Testing at Room** ☐ Testing at Cold ☐ **Testing at Hot** ☐ Drift Analysis ☐ C-SAM post ☐ WBP (first / second bond) ☐ WBS ☐ Internal Inspection ☐ Cross section ☐ Cratering test	1	77	77	Lot 1: 0 / 77 Lot 2: 0 / 77	
UHAST	A3	JESD22 A118	P=2.08atm Ta=121°C, Duration = 96hrs ☒ **After PC** ☒ **Testing at Room** ☐ Testing at Cold ☐ Testing at Hot ☐ Drift Analysis ☐ C-SAM post ☐ WBP (first / second bond) ☐ WBS ☐ Internal Inspection ☐ Cross section ☐ Cratering test	1	77	77	Lot 1: 0 / 77 Lot 2: 0 / 77	

TC	A4	JESD22 A104	Ta=-55°C /+150 °C Duration= 1000 cyc ☒ **After PC** ☒ Testing at Room ☐ Testing at Cold ☐ **Testing at Hot** ☐ Drift Analysis ☐ C/T-SAM post ☐ **WBP (first / second bond)** ☐ WBS ☐ Internal Inspection ☐ Cross section ☐ Cratering test	1	77	77	Lot 1: 0 / 77 Lot 2: 0 / 77	
HTSL	A6	JESD22 A103	Ta= 150ºC Duration= 1000hrs ☐ **After PC** ☒ **Testing at Room** ☐ Testing at Cold ☐ **Testing at Hot** ☐ Drift Analysis ☐ WBP (first / second bond) ☐ WBS ☐ Internal Inspection ☐ Cross section ☐ Cratering test	1	77	77	Lot 1: 0 / 77 Lot 2: 0 / 77	

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

Test	#	Reference	Q100/STM Test Conditions	Lots	S.S.	Total	Re-sults/ Lot	Comments: (N/A =Not Applicable)
HTOL	B1	JESD22 A108	Ta= 125ºC (TJ=150°C) Duration= 1000hrs ☐ After PC ☒ **Testing at Room** ☐ **Testing at Cold** ☐ **Testing at Hot** ☒ Drift Analysis ☐ Internal Inspection	1	77	77	Lot 1: 0 / 77 Lot 2: 0 / 77	.

TEST GROUP C - ELECTRICAL VERIFICATION

Test	#	Reference	STM Test Conditions	Lots	S.S.	To-tal	Results/Lot Pass/Fail	Comments: (N/A =Not Applicable)
HBM	E2	AEC-Q100-002	Target HBM=+/-2kV ☒ **Testing at Room** ☐ Testing at Cold ☐ **Testing at Hot** ☐ Drift Analysis	2	3	3	All samples are pass	
CDM	E3	AEC-Q100-011	Target CDM=+/-1kV ☒ **Testing at Room** ☐ Testing at Cold ☐ **Testing at Hot** ☐ Drift Analysis	2	3	3	All samples are pass	
LU	E4	AEC-Q100-004	Current Injection Class II - Level A (+/- 100mA) ☒ **Testing at Room** ☐ Testing at Cold ☐ **Testing at Hot**	2	6	6	All samples are pass	

A. Applicable and reference documents

Reference	Short description
AEC-Q100	Failure Mechanism Based Stress Test Qualification for Integrated Circuits in automotive applications
AEC-Q101	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in automotive applications
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification

GLOSSARY

AC	Autoclave
ACBV	AC Blocking Voltage
ASER	Accelerated Soft Error Rate
AST	Adhesion Shear Test
BI	Burn-In
BT3P	Board 3 points Bending Test
BT4P	Board 4 points Bending Test
CA	Constant Acceleration
CDM	Electrostatic Discharge – Charged Device Model
ConA	Construction Analysis
CVS	Constant Voltage Stress
DBT	Dead Bug Test
DPA	Destructive Physical Analysis
DROP	Package drop
DS	Die Shear
DToB	Drop Test on Board
EDR	NVM Program/Erase Endurance & Data Retention Stress Test
ELFR	Early Life Failure Rate
EMC	Electromagnetic Compatibility
EOS	Electrical Overstress characterization
ESeq	Environmental sequence
EV	External Visual
GFF	
GFL	Gross/Fine Leak
GL	Electro-thermally Induced Gate Leakage
GStress	Gate Stress
GUN	Electrostatic Discharge - System Level Test
H^{3}TRB	High Humidity High Temperature Reverse Bias
HAST	Biased HAST (Highly Accelerated Stress Test)
HBM	Electrostatic Discharge - Human Body Model
HER	Hermeticity
HMM	Electrostatic Discharge - Human Metal Model
HTFB	High Temperature Forward Bias
HTGB	High Temperature Gate Bias
HTHHB	High Temperature High Humidity Bias
HTOL	High Temperature Operating Life
HTRB	High Temperature Reverse Bias.
HTSL	High Temperature Storage Life
IOL	Intermittent Operating Life

IWV	Internal Water Vapor
LF	Lead Free
LI	Lead Integrity
LT	Lid Torque
LTOL	Low Temperature Operating Life
LTSL	Low Temperature Storage Life
LU	Latch-Up
MM	Electrostatic Discharge - Machine model

MR	Multiple Reflow
MS	Mechanical Shock
MSeq	Mechanical sequence
MSL	Moisture Sensitivity Level
NVM	Non Volatile Memory
PC	Preconditioning
PD	Physical Dimensions
PTC	Power Temperature Cycling
RS	Repetitive Surge Test
TSH	Resistance to Solder Heat
RTSER	Real-Time Soft Error Rate
SAM	Scanning Acoustic Microscopy
SBP	Solder Ball Pull
SBS	Solder Ball Shear
SC	Short Circuit Characterization
SCCSS	Smartcard – Constant Supply Stress
SCMCMS	Smartcard – MasterCard Mechanical Stress
SCMF	Smartcard – Magnetic Field Stress
SCPOOS	Smartcard – Power Off/On Stress
SCRFC	Smartcard – RF On/Off Cyclic Stress
SCRFS	Smartcard – RF On Static Stress
ScrT	Screw Test
SCSA	Smartcard – Salt Atmosphere
SCUV	Smartcard – UV Test
SCXRAY	Smartcard – XRAY Test
SD	Solderability
SSOP	Steady State Operational
SToB	Shock Test on Board
TC	Temperature Cycling
TCDT	Temperature Cycling Delamination Test
TCHT	Temperature Cycling Hot Test
TCoB	Temperature Cycling on Board
THB	Temperature Humidity Bias
THS	Temperature Humidity Storage
TLP	Electrostatic Discharge – Transmission Line Pulse
TS	Thermal Shocks
TStr	Terminal Strength
Tumb	Tumbler Test
UHAST	Unbiased HAST (Highly Accelerated Stress Test)
VToB	Vibration Test on Board
VFV	Variable Frequency Vibration
WAT	Tin (Sn) Whisker Acceptance Testing
WBI	Wire Bond Integrity
WBP	Wire Bond Pull
WBS	Wire Bond Shear
WBSt	Wire Bond Strength
XRAY	X ray inspection

Datasheet update

STG3692
Page 6 of datasheet (current one)

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
I_{ON}	ON-state leakage current (D)	4.3	V_S=0.3 V and V_D=4 V or V_S=4 V and V_D=0.3 V			±20		±100	nA
I_{SEL}	SEL input leakage current	0 to 4.3	V_{SEL} = 0 to 4.3 V			±0.1		±1	µA
I_{CC}	Quiescent supply current	1.65 to 4.3	V_{SEL} = V_{CC} or GND			±0.1		±1	µA
I_{CCLV}	Quiescent supply current low voltage driving	4.3	$V_{1\text{-}2SEL}$, $V_{3\text{-}4SEL}$ = 1.65 V		±37	±50		±100	µA
			$V_{1\text{-}2SEL}$, $V_{3\text{-}4SEL}$ = 1.80 V		±33	±40		±50	
			$V_{1\text{-}2SEL}$, $V_{3\text{-}4SEL}$ = 2.60 V		±11	±20		±30	

Page 6 of datasheet (New version)

Symbol	Parameter	Test conditions		Datasheet Value				
		Vcc (V)		TA = 25 °C			-40 to 85 °C	
				Min.	Typ.	Max.	Min.	Max.
ISEL	SEL leakage current	0 to 4.3	VSEL = 0 to 4.3 V			**±0.1**		2
ICC	Quiescent supply current	1.65 to 4.3	VSEL = VCC or GND			**0.1**		3
ICCLV	Quiescent supply current low voltage driving	4.3	V1-2 SEL, V3-4 SEL = 1.65 V		20	25		35
			V1-2 SEL, V3-4 SEL = 1.80 V		17	22		30
			V1-2 SEL, V3-4 SEL = 2.60 V		6	11		20

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
B_W	-3 dB bandwidth	3.0-4.3	RL = 50 Ω, signal= 0 dBm		800				MHz

Typical value becomes 500MHz

STG3856

As -55°C/+125°C is no more a range existing for this product family the range in datasheet will move to -40/+125°C

Current datasheet

Table 6. DC electrical characteristics (continued)

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
I_{OFF}	OFF state leakage current (nSN), (Dn)	4.3	V_S = 0.3 or 4 V	–	–	± 20	–	±100	–	–	nA
I_{IN}	Input leakage current	0 - 4.3	V_{IN} = 0 to 4.3 V	–	–	± 0.1	–	± 1	–		µA
I_{CC}	Quiescent supply current	1.65 - 4.3	V_{IN} = V_{CC} or GND	–	–	± 0.05	–	± 0.2	–	± 1	µA

New revision

Symbol	Parameter	V_{CC} (V)		T_A = 25°C			-40 to 85°C		-40 to 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
I_{OFF}	OFF state leakage current (nSN), (Dn)	4.3	V_S = 0.3 or 4 V	–	–	± 20	–	±100	–	–	nA
I_{IN}	Input leakage current	0 - 4.3	V_{IN} = 0 to 4.3 V	–	–	± 0.1	–	± 2	–	±I5	µA
I_{CC}	Quiescent supply current	1.65 - 4.3	V_{IN} = V_{CC} or GND	–	–	± 0.05	–	± 3	–	±25	µA