


# PRODUCT / PROCESS CHANGE NOTIFICATION

## 1. PCN basic data

1.1 Company		STMicroelectronics International N.V
1.2 PCN No.	AMS/21/12801	
1.3 Title of PCN	Changes Notification on STGAP2S.	
1.4 Product Category	Motion Control&Automation	
1.5 Issue date	2021-06-07	

## 2. PCN Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Domenico ARRIGO
2.1.2 Marketing Manager	Fabio CHELLI
2.1.3 Quality Manager	Alessandro PLATINI

## 3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Product transfer from one site to another site, even if test or process line is qualified	ASSY plant: ASE FT plant: MUAR

## 4. Description of change

	Old	New
4.1 Description	IP FE ISOLATION: 1.7KV ASSY plant: SHENZEN (BOM 1F137576) FT plant: AGRATE DS version 1	IP FE ISOLATION: 6KV ASSY plant: ASE (BOM 1F142589) FT plant: MUAR DS version 2
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

## 5. Reason / motivation for change

5.1 Motivation	The listed changes are qualified and implemented to guarantee the quality improvement of the impacted product: STGAP2S.
5.2 Customer Benefit	QUALITY IMPROVEMENT

## 6. Marking of parts / traceability of change

6.1 Description	New FGs
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## 7. Timing / schedule

7.1 Date of qualification results	2021-02-17
7.2 Intended start of delivery	2021-09-24
7.3 Qualification sample available?	Upon Request

## 8. Qualification / Validation

8.1 Description	12801 RR002220CS6080_3.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-06-07

9. Attachments (additional documentations)
12801 Public product.pdf 12801 RR002220CS6080_3.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STGAP2SCM	
	STGAP2SCMTR	
	STGAP2SMTR	

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**PCN Title :** Changes Notification on STGAP2S.

**PCN Reference :** AMS/21/12801

**Subject :** Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STGAP2SMTR	STGAP2SCMTR	STGAP2SM
STGAP2SCM		



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# Reliability Evaluation Report

**RR002220CS6080**

(New Product)

General Information		Traceability	
Product Line	: MY1D	Diffusion Plant	: Catania (U1SD) + Agrate (U1SF)
Product Description	: Galvanically Isolated 4A single gate driver	Assembly Plant	: ASE CL
Package	: SO8W : SO8N	Reliability Assessment	
Silicon Technology	: U1SD (BCD6s) + U1SF (BCD6s)	Pass	<input checked="" type="checkbox"/>
		Fail	<input type="checkbox"/>

***Note:** this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Content description	Date	Author	Function
1.0	Initial Revision	29-Jun-2020	Gianfranco D'Angelo	Reliability Engineer
1.1	Update Test Plan and narrow package option	17-Feb-2021	Gianfranco D'Angelo	Reliability Engineer

## APPROVED BY:

Function	Location	Name
Division Reliability Manager	Italy	Alceo Paratore
Division Quality Manager	Italy	Alessandro Platini

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## 1 RELIABILITY EVALUATION OVERVIEW

### 1.1 Objective

This report contains the reliability evaluation of MY1D device diffused in Catania (U1SD) + Agrate (U1SF) and assembled in SO8W and SO8N in ASE CL.

### 1.2 Reliability Strategy

Reliability trials performed as part of this reliability evaluation are in agreement with **ST 0061692** specification and are listed in below Test Plan. For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

### 1.3 Conclusion

All reliability tests have been completed with positive results.

Based on the overall results obtained, MY1D product in Catania (U1SD) + Agrate (U1SF) and assembled in SO8W and SO8N in ASE CL, has positively passed reliability evaluation.

## 2 PRODUCT OR TEST VEHICLE CHARACTERISTICS

### 2.1 Product Description

The MY1D device is a single gate driver which provides galvanic isolation between the gate driving channel and the low voltage control and interface circuitry.

The gate driver is characterized by 4A capability and rail-to-rail output, making the device also suitable for mid and high-power applications such as power conversion and motor driver inverters in industrial applications.

## 2.2 Pin connection

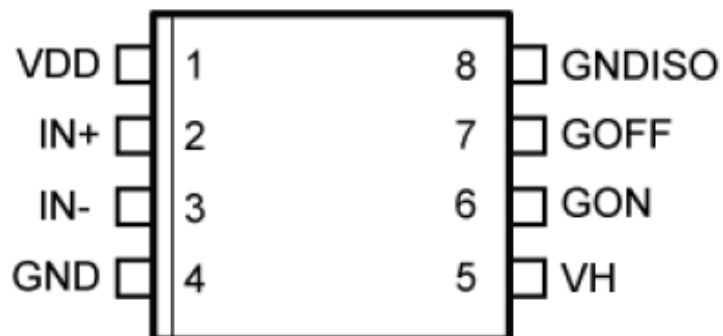


Figure 1. Pin connection with Separated Output option

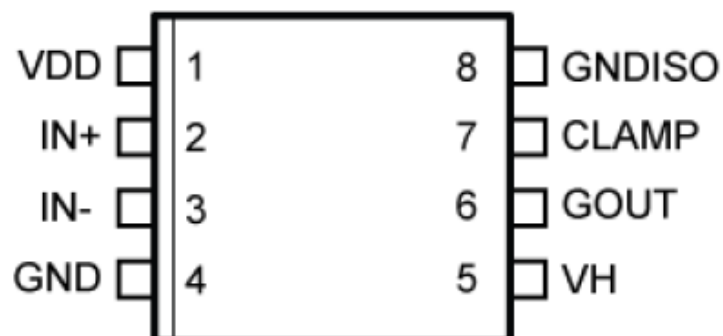


Figure 2. Pin connection with Single Output and Miller CLAMP option

## 2.3 Block diagram

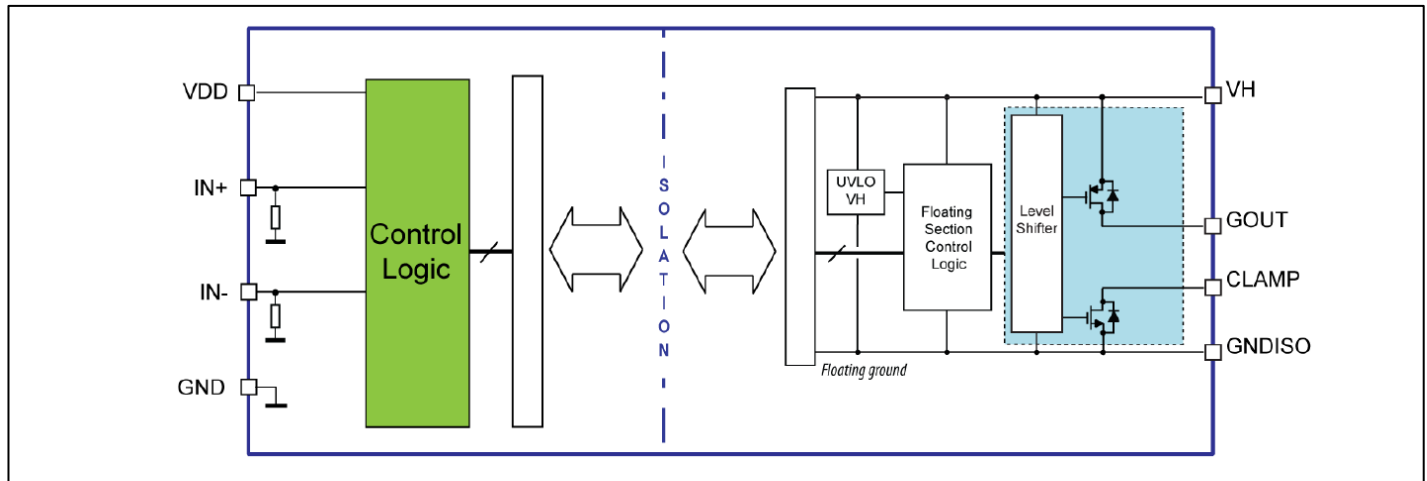


Figure 3. Block Diagram with Separate output

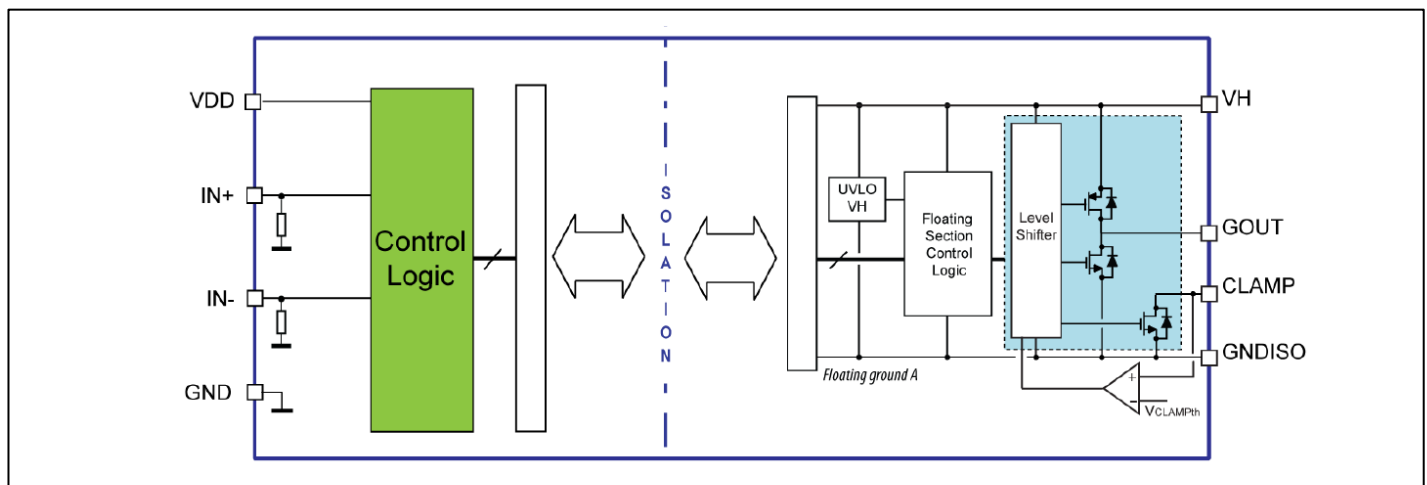
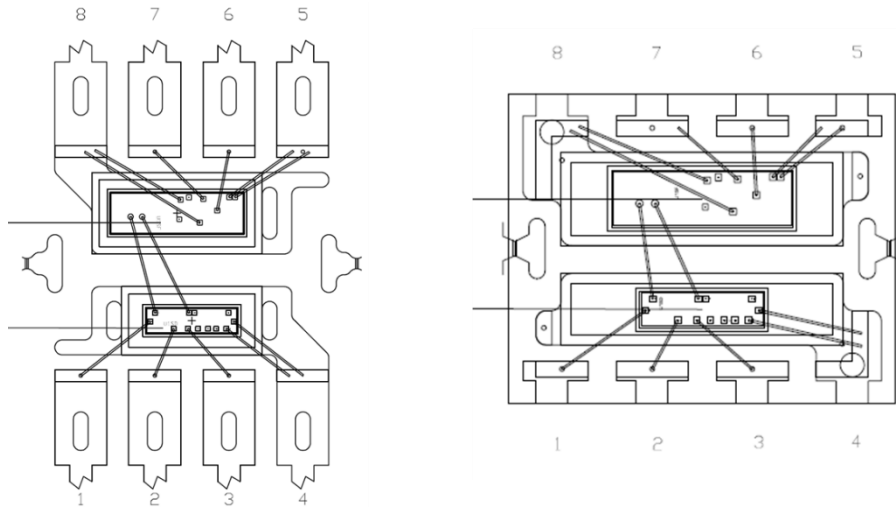
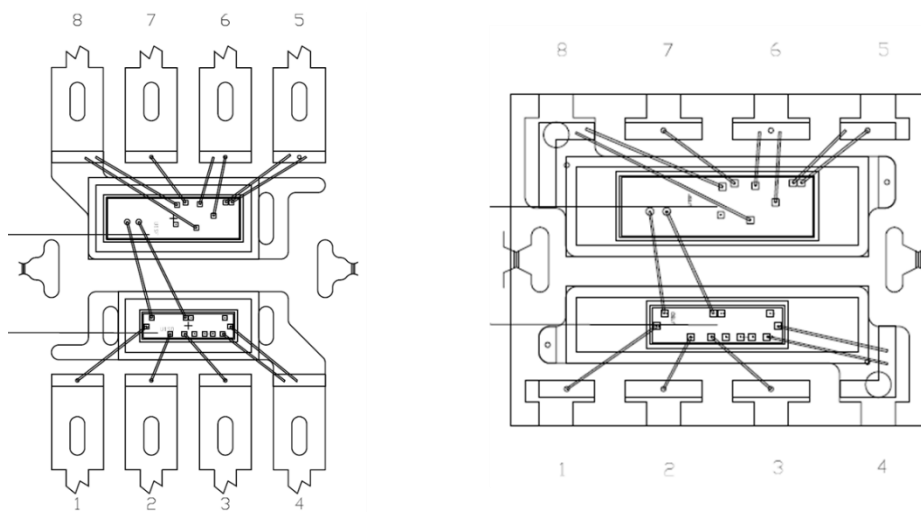


Figure 4. Block Diagram with Single Output and Miller Clamp

## 2.4 Bonding diagram



*Figure 5. Bonding Diagram with Separate Output in package wide (left) and narrow (right)*



*Figure 6. Bonding Diagram with Single Output and Miller Clamp in package wide (left) and narrow (right)*

## 2.5 Traceability

### 2.5.1 Wafer fab information

Table 1

Wafer fab information ( U1SD )	
FAB1	
Wafer fab location	Catania
Wafer diameter (inches)	8 inches
Die thickness (µm)	280+/-20 UM
Silicon process technology	BCD6s
Die finishing front side (passivation)	TEOS/SiN/Polyimide
Die finishing back side	Cr/Ni/Au
Die area (X,Y) (µm)	1679,552 UM
Metal levels	3
Wafer fab information ( U1SF )	
FAB1	
Wafer fab location	Agrate
Wafer diameter (inches)	8 inches
Die thickness (µm)	280+/-20 UM
Silicon process technology	BCD6s
Die finishing front side (passivation)	SiN/TEOS/SiN/Polyimide
Die finishing back side	Cr/NiV/Au
Die area (X,Y) (µm)	816,2393 UM
Metal levels	4

## 2.5.2 Assembly information

**Table 2**

Assembly Information	
Package 1 – SO8W – SO8N	
Assembly plant location	ASE CHUNG LI
Lead frame finishing (material)	Sn
Die attach material	EN4900G
Wire bonding material/diameter	Au 1.0 mils
Molding compound material	EME-G631H

### 2.5.3 Reliability information

**Table 3**

Reliability Information	
Reliability laboratory name / location	Cornaredo (Italy)

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.

ST certification document can be downloaded under the following link:

[http://www.st.com/content/st\\_com/en/support/quality-and-reliability/certifications.html](http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html)

### 3 TESTS RESULTS SUMMARY

#### 3.1 Lot Information

Table 4

Lot #	Diffusion Lots	Trace Code	Die Revision	Package	Note
1	5832X8K (U1SD) A838461T01(U1SF)	AA008AJV	ABA	SO8 WIDE	<i>Miller clamp option</i>
2	5832X8K (U1SD) A838461T01(U1SF)	AA004ADU	ABA	SO8 WIDE	<i>Miller clamp option</i>
3	5832X8K (U1SD) A838461T01(U1SF)	AA008AJV	ABA	SO8 WIDE	<i>Miller clamp option</i>
4	5832X8K (U1SD) A930425 (U1SF)	AA037ADS	ACA	SO8 NARROW	<i>Miller clamp option</i>
5	5832X8K (U1SD) A930425 (U1SF)	AA037ADS	ACA	SO8 NARROW	<i>Miller clamp option</i>
6	5832X8K (U1SD) A930425 (U1SF)	AA037ADS	ACA	SO8 NARROW	<i>Miller clamp option</i>
7	5832X8K (U1SD) A930425 (U1SF)	AA022AEA	ACA	SO8 NARROW	<i>Separated Output option</i>

## 3.2 Test plan and results summary

**Table 5 – ACCELERATED LIFETIME SIMULATION TESTS**

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results / Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22 A108	TJ=150°C VH=26V, VDD=5.5V, GNDISO=1700V  Duration= 1000hrs  <input checked="" type="checkbox"/> After PC <input type="checkbox"/> Assy on Chip Board <input checked="" type="checkbox"/> Testing at Room	2	77	154	Lot 1: 0 / 77 Lot 5 : 0 / 77	-
All samples (excluded samples on chipboard) have been submitted at Partial Discharge (Method B) test at ATE before and after reliability stress test with positive results							

**Table 6 – ACCELERATED ENVIRONMENT STRESS TESTS**

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/ Lot Fail/S.S.	Comments: (N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, MSL3 (192h@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	6	-	833	Lot 1: 0 / 211 Lot 2: 0 / 115 Lot 3: 3 / 115 Lot 4: 0 / 135 Lot 5: 0 / 122 Lot 6: 0 / 135	-
THB	JESD22 A101	Ta=85°C, 85%RH, VH=26V, VDD=5.5V, GNDISO=0V (1) Duration= 1000hrs  Ta=85°C, 85%RH VH=26V, VDD=5.5V, GNDISO=1500V (2) Duration= 1000hrs  <input checked="" type="checkbox"/> After PC <input type="checkbox"/> Assy on Chip Board <input checked="" type="checkbox"/> Testing at Room	6	25	150	Lot 1: 0/25 Lot 2: 0/25 Lot 3: 0/25 Lot 4: 0/25 Lot 5: 0/25 Lot 6: 0/25	(1) only wide package option (2) both package options
TC	JESD22-A104	Ta= -55°C to + 150°C Duration= 1000cyc  <input checked="" type="checkbox"/> After PC <input checked="" type="checkbox"/> Testing at Room	5	25	125	Lot 1: 0/25 Lot 2: 0/25 Lot 3: 0/25 Lot 4: 0/45 Lot 6: 0/45	-
uHAST	JESD22-A118	Ta=130°C, RH=85% Duration = 96hrs  <input checked="" type="checkbox"/> After PC <input checked="" type="checkbox"/> Testing at Room	3	25	75	Lot 1: 0/25 Lot 2: 0/25 Lot 3: 0/25	-
AC	JESD22 A102	P=2.08atm Ta=121°C, Duration = 96hrs  <input checked="" type="checkbox"/> After PC <input checked="" type="checkbox"/> Testing at Room	2	25	50	Lot 4: 0/45 Lot 6: 0/45	-
HTSL	JESD22 A103	Ta= 150°C Duration= 1000hrs  <input type="checkbox"/> After PC <input checked="" type="checkbox"/> Testing at Room	5	25	125	Lot 1: 0/25 Lot 2: 0/25 Lot 3: 0/25 Lot 4: 0/45 Lot 6: 0/45	-
All samples (excluded samples on chipboard) have been submitted at Partial Discharge (Method B) test at ATE before and after reliability stress test with positive results							

**Table 7 – ELECTRICAL VERIFICATION TESTS**

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results Fail/S.S.	Comments: (N/A =Not Applicable)
HBM	ANSI/ESDA/JEDEC JS001	HBM=+/-2kV <input checked="" type="checkbox"/> Testing at Room	1	3	3	Lot 1: 0 / 3	
CDM	ANSI/ESDA/JEDEC JS001	CDM=+/-750V on corner pins; +/- 500V all others <input checked="" type="checkbox"/> Testing at Room	2	3	6	Lot 1: 0 / 3 Lot 4: 0 / 3	
LU	JESD78	Current Injection Class II - Level A (+/- 100mA)  Overvoltage Class II - Level A (1,5 x Vmax)  Tdut=125°C <input checked="" type="checkbox"/> Testing at Room	2	6	12	Lot 1: 0 / 6 Lot 7: 0 / 6	

Note: Test method revision reference is the one active at the date of reliability trial execution.

#### 4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
AEC-Q100	Failure Mechanism Based Stress Test Qualification for Integrated Circuits in automotive applications
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
DMS 0061692	Reliability Tests and Criteria for Product Qualification

## 5 GLOSSARY

*List update based on applicable items.*

AC	Autoclave	MR	Multiple Reflow
ACBV	AC Blocking Voltage	MS	Mechanical Shock
ASER	Accelerated Soft Error Rate	MSeq	Mechanical sequence
AST	Adhesion Shear Test	MSL	Moisture Sensitivity Level
BI	Burn-In	NVM	Non Volatile Memory
BT3P	Board 3 points Bending Test	PC	Preconditioning
BT4P	Board 4 points Bending Test	PD	Physical Dimensions
CA	Constant Acceleration	PTC	Power Temperature Cycling
CDM	Electrostatic Discharge – Charged Device Model	RS	Repetitive Surge Test
ConA	Construction Analysis	TSH	Resistance to Solder Heat
CVS	Constant Voltage Stress	RTSER	Real-Time Soft Error Rate
DBT	Dead Bug Test	SAM	Scanning Acoustic Microscopy
DPA	Destructive Physical Analysis	SBP	Solder Ball Pull
DROP	Package drop	SBS	Solder Ball Shear
DS	Die Shear	SC	Short Circuit Characterization
DToB	Drop Test on Board	SCCSS	Smartcard – Constant Supply Stress
EDR	NVM Program/Erase Endurance & Data Retention Stress Test	SCMCMS	Smartcard – MasterCard Mechanical Stress
ELFR	Early Life Failure Rate	SCMF	Smartcard – Magnetic Field Stress
EMC	Electromagnetic Compatibility	SCPOOS	Smartcard – Power Off/On Stress
EOS	Electrical Overstress characterization	SCRFC	Smartcard – RF On/Off Cyclic Stress
ESeq	Environmental sequence	SCRFS	Smartcard – RF On Static Stress
EV	External Visual	ScrT	Screw Test
GFF		SCSA	Smartcard – Salt Atmosphere
GFL	Gross/Fine Leak	SCUV	Smartcard – UV Test
GL	Electro-thermally Induced Gate Leakage	SCXRAY	Smartcard – XRAY Test
GStress	Gate Stress	SD	Solderability
GUN	Electrostatic Discharge – System Level Test	SSOP	Steady State Operational
H3TRB	High Humidity High Temperature Reverse Bias	SToB	Shock Test on Board
HAST	Biased HAST (Highly Accelerated Stress Test)	TC	Temperature Cycling
HBM	Electrostatic Discharge – Human Body Model	TCDT	Temperature Cycling Delamination Test
HER	Hermeticity	TCHT	Temperature Cycling Hot Test
HMM	Electrostatic Discharge – Human Metal Model	TCoB	Temperature Cycling on Board
HTFB	High Temperature Forward Bias	THB	Temperature Humidity Bias
HTGB	High Temperature Gate Bias	THS	Temperature Humidity Storage
HTHHB	High Temperature High Humidity Bias	TLP	Electrostatic Discharge – Transmission Line Pulse
HTOL	High Temperature Operating Life	TS	Thermal Shocks
HTRB	High Temperature Reverse Bias.	TStr	Terminal Strength
HTSL	High Temperature Storage Life	Tumb	Tumbler Test
IOL	Intermittent Operating Life	UHASt	Unbiased HAST (Highly Accelerated Stress Test)
IWV	Internal Water Vapor	VToB	Vibration Test on Board
LF	Lead Free	VFV	Variable Frequency Vibration
LI	Lead Integrity	WAT	Tin (Sn) Whisker Acceptance Testing
LT	Lid Torque	WBI	Wire Bond Integrity
LTOL	Low Temperature Operating Life	WBP	Wire Bond Pull
LTSL	Low Temperature Storage Life	WBS	Wire Bond Shear
LU	Latch-Up	WBSt	Wire Bond Strength
MM	Electrostatic Discharge – Machine model	XRAY	X ray inspection

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