PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	AMS/21/12761
1.3 Title of PCN	Qualification of ST Shenzhen for Assembly of M74HC4060 in SO16 package
1.4 Product Category	See product list
1.5 Issue date	2021-04-30

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Salvatore DI VINCENZO
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	Assembly plant : - ST Shenzhen

4. Description of change		
	Old	New
4.1 Description	Assembly plant : - Subcontractor ASE	Assembly plant : - Subcontractor ASE - ST Shenzhen
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	Service improvement
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	New finished good code

7. Timing / schedule	
7.1 Date of qualification results	2021-04-22
7.2 Intended start of delivery	2021-08-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	12761 SO16SHZ Z460 std final.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-04-30

9. Attachments (additional documentations)
12761 Public product.pdf 12761 SO16SHZ Z460 std final.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	M74HC4060RM13TR	

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Subject to any contractual arrangement in force with you or to any industry standard implemented by us, STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Qualification of ST Shenzhen for Assembly of M74HC4060 in SO16 package

PCN Reference : AMS/21/12761

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

M74HC4060RM13TR		

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Subject to any contractual arrangement in force with you or to any industry standard implemented by us, STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

Reliability Evaluation Report

qualification SO16
ST Shenzhen

General Information	
Product Line	T.V.1:P10B01 T.V.2: R85201 T.V.3.Z460
Product Description	Hex Buffer/Converters Non Inverting Analog Mux With Current Injectiom Effect 14 Stage Binary Counter / Oscillator
P/N	T.V.1: HCF4010YM013TR, T.V.2: M74HC4852YRM13TR, T.V.3: M74HC4060RM13TR
Product Group	AMS
Product division	General Purpose Analog
Package	SO16
Silicon Process technology	TV1:CMOSMG TV2:HCMOS4T T.V3. NHSFII

Locations	
Wafer fab	ST AMK6 Singapore
Assembly plant	ST Shenzhen
Reliability Lab	Catania Reliability LAB SHZ Reliability Lab

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
0061692	Reliability tests and criteria for qualifications

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To perform the qualification for the SO16 produced in ST Shenzhen, based on the JESD47 specification.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

Reliability agreement for qualification.

4 DEVICE CHARACTERISTICS

4.1 Device description

life.augmented

HCF4010

Hex buffer/converter (non-inverting)

Datasheet - production data

SO16

Features

- Propagation delay time
  - t_{PD} = 50 ns (typ.) at V_{DD} = 10 V, C_L = 50 pF
- High to low level logic conversion
- Multiplexer: 1 to 6 or 6 to 1
- High "sink" and "source" current capability
- Quiescent current specified up to 20 V
- 5 V, 10 V and 15 V parametric ratings
- Input leakage current
- I_I = 100 nA (max.) at V_{DD} = 18 V, T_A = 25 °C
  100% tested for quiescent current
- ESD performance
  - CDM: 1 kV
  - HBM: 1 kV
  - MM: 150 V

Applications

- Automotive
- Industrial
- Computer
- Consumer

Description

The HCF4010 device is a monolithic integrated circuit fabricated in MOS (metal oxide semiconductor) technology available in an SO16 package.

It is a non-inverting hex buffer/converter and can be used as a CMOS to TTL logic level converter, as a current "sink" or "source" driver, or as a multiplexer (1 to 6).

It is the preferred replacement of the HCF4050B in buffer applications.

Table 1. Device summary

Order code	Temperature range	Package	Packing	Marking
HCF4010M013TR	–55 °C to +125 °C	SO16	Tape and reel	HCF4010
HCF4010YM013TR(1)	–40 °C to +125 °C	SO16 (automotive grade)		HCF4010Y

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

M74HC4852

Dual 4:1 channel analog MUX/DEMUX with injection current protection

Datasheet – production data

Features

- Low power dissipation
  - I_{CC} = 2 µA (max.) at T_A = 25 °C
- Injection current protection: $V_{\Delta}out$ < 1 mV at V_{CC} = 5 V, I_{IN} = 1 mA, R_S = 3.9 kΩ
- "ON" resistance at T_A = 25 °C
  - 215 Ω typ. (V_{CC} = 3.0 V)
  - 160 Ω typ. (V_{CC} = 4.5 V)
  - 150 Ω typ. (V_{CC} = 6 V)
- Fast switching: t_{pd} = 8.6 ns (typ.) at T_A = 25 °C, V_{CC} = 4.5 V
- Wide operating supply voltage range
  - V_{CC} = 2 V to 6 V
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- Pin and function compatible with series 4052, 4852
- Latch-up performance exceeds 500 mA
  - (JESD 17)
- ESD performance
  - HBM: 2000 V
  - MM: 200 V
  - CDM: 1000 V

Applications

- Automotive
- Computer
- Consumer
- Industrial

SO-16

Description

The M74HC4852 device is a dual four-channel analog multiplexer/demultiplexer manufactured with silicon gate C^2MOS technology.

It features injection current effect control which makes the device particularly suited for use in automotive applications where voltages in excess of normal logic voltage are common. The injection current effect control allows signals at disabled input channels to exceed the supply voltage range or go down to ground without affecting the signal of the enabled analog channel.

This eliminates the need for external diode-resistor networks typically used to keep the analog channel signals within the supply voltage range.

Table 1. Device summary

Order code	Temperature range	Package	Packaging	Marking
M74HC4852RM13TR	-55/+125 °C	SO16	Tape and reel	74HC4852
M74HC4852YRM13TR(1)	-40/+125 °C	SO16 (automotive grade)	Tape and reel	74HC4852Y

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

M74HC4060

14-stage binary counter/oscillator

Datasheet - production data

SO16 TSSOP16

Features

- High speed:
  f_{max} = 65 MHz (typ.) at V_{CC} = 6 V
- Low power dissipation:
  I_{CC} = 4 A (max.) at T_A = 25 °C
- High noise immunity:
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- Symmetrical output impedance:
  $|I_{OH}| = I_{OL}$ = 4 mA (min.)
- Balanced propagation delays: $T_{PLH} \equiv T_{PHL}$
- Wide operating voltage range:
  V_{CC} (opr.) = 2 V to 6 V
- Pin and function compatible with 74 series 4060
- ESD performance
  - HBM: 2 kV
  - MM: 200 V
  - CDM: 1 kV

Applications

- Automotive
- Industrial
- Computer
- Consumer

Description

The M74HC4060 device is a high speed CMOS 14-stage binary counter/oscillator fabricated with silicon gate C^2MOS technology.

The oscillator configuration allows design of either RC or crystal oscillator circuits. A high level on the CLEAR accomplishes the reset function, i.e. all counter outputs are made low and the oscillator is disabled.

A negative transition on the clock input increments the counter. Ten kinds of divided output are provided; 4 to 10 and 12 to 14 stage inclusive. The maximum division available at Q12 is 1/16384 of the oscillator frequency.

The $\overline{\text{Ø}}$I input and the CLEAR input are equipped with protection circuits against static discharge and transient excess voltage.

Table 1. Device summary

Order code	Temperature range	Package	Packing	Marking
M74HC4060RM13TR	-55 °C to +125 °C	SO16	Tape and reel	74HC4060
M74HC4060YRM13TR(1)	-40 °C to +125 °C	SO16 (automotive version)		74HC4060Y
M74HC4060TTR	-55 °C to +125 °C	TSSOP16		HC4060
M74HC4060YTTR(1)	-40 °C to +125 °C	TSSOP16 (automotive version)		HC4060Y

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002.

4.2 Construction note

	HCF4010YM013TR	M74HC4852YRM13TR	M74HC4060RM13TR
Wafer/Die fab. information			
Wafer fab manufacturing location	ST AMK6 Singapore	ST AMK6 Singapore	ST AMK6 Singapore
Technology	CMOS metal gate	HCMOS4	High speed CMOS
Process family	CMOS	Bicmos4	CMOS
Die finishing back side	Lapped Silicon	Lapped Silicon	Lapped Silicon
Die size	1294x1088µm²	1300x1212µm²	2284x1794µm²
Bond pad metallization layers	AlSi	AlSiCu	AlSi
Passivation type	P-VAPOX (Si glass)	PSG + NITRIDE	P-VAPOX(SiO2) / NITRIDE
Wafer Testing (EWS) information			
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K
Assembly information			
Assembly site	ST Shenzhen	ST Shenzhen	ST Shenzhen
Package description	SO16	SO16	SO16
Molding compound	Sumitomo EME-G630AY	Sumitomo EME-G630AY	Sumitomo EME-G630AY
Frame material	Cu	Cu	Cu
Die attach process	Glue	Glue	Glue
Die attach material	ABLESTICK 8601S-25	ABLESTICK 8601S-25	ABLESTICK 8601S-25
Die pad size	94x150	94x150	94x150
Wire bonding process	Wire	Wire	Wire
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	Preplated	Preplated	Preplated
Lead finishing/bump solder material	NiPdAgAu	NiPdAgAu	NiPdAgAu
Final testing information			
Testing location	ST Shenzhen	ST Shenzhen	ST Shenzhen
Tester	ASL1K	ASL1K	ASL1K

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Techno/package	Product Line	Comments
1	CMOS MG/SO16	P10B	
2	HCMOS4/SO16	R852	
3	HSPEED CMOS/SO16	Z460	

Detailed results in below chapter will refer to P/N and Lot #.

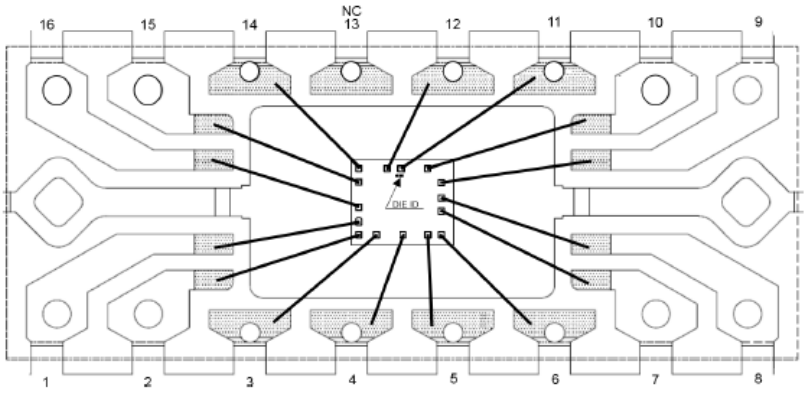
5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1 P10B	Lot 2 R852	Lot 3 Z460	
Die Oriented Tests									
HTOL	N	JESD22 A-108	Ta= 125°C TV1 Vbias=+22V; TV2&TV3 Vbias=+7V		168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/45	0/45	0/45	
					500h	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	
PC		JESD22 A-113	Drying 24 H @ 125°C Store 40h @Ta=60°C Rh60% Oven Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H	0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	
					1000 cy	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS 30V		168 H	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	
ESD	N		CDM	3	1 kV			PASS	

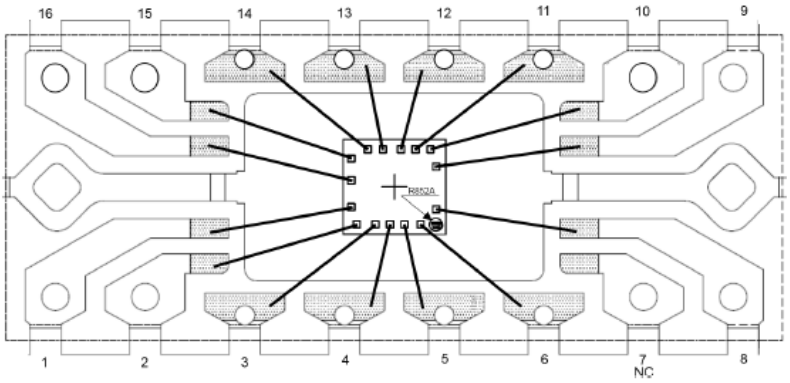
6 ANNEXES

6.1.1 Bonding diagram

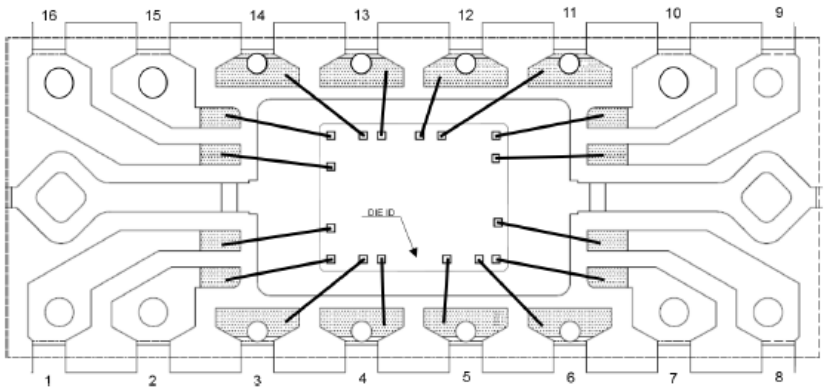
P10B



R852



Z460



6.1.2 Package outline

CP	Unit / dim	A	A1	A2	b	D	E	E1	L
ULQ2003D1013TRY	**1**	1.69	0.15	1.54	0.43	9.86	5.98	3.89	0.62
	2	1.71	0.15	1.49	0.42	9.86	5.97	3.90	0.61
	3	1.69	0.15	1.55	0.40	9.84	5.97	3.90	0.61
	4	1.71	0.17	1.52	0.41	9.86	5.98	3.89	0.62
	5	1.69	0.15	1.55	0.42	9.85	5.99	3.90	0.61
	6	1.69	0.18	1.53	0.40	9.84	5.99	3.90	0.63
	7	1.69	0.19	1.50	0.43	9.85	5.96	3.89	0.63
	8	1.67	0.19	1.52	0.41	9.86	5.97	3.90	0.63
	9	1.71	0.19	1.50	0.43	9.86	5.98	3.89	0.61
	10	1.69	0.15	1.57	0.41	9.85	5.95	3.89	0.63
HCF4010YM013TR	**11**	1.67	0.17	1.50	0.41	9.87	5.94	3.89	0.62
	12	1.68	0.19	1.50	0.41	9.85	5.95	3.90	0.62
	13	1.69	0.19	1.51	0.41	9.83	5.96	3.90	0.62
	14	1.67	0.16	1.50	0.42	9.85	5.95	3.90	0.62
	15	1.69	0.19	1.51	0.41	9.84	5.95	3.90	0.63
	16	1.70	0.19	1.50	0.42	9.86	5.97	3.90	0.62
	17	1.70	0.17	1.57	0.43	9.84	5.99	3.89	0.62
	18	1.69	0.18	1.50	0.41	9.84	5.96	3.89	0.62
	19	1.71	0.20	1.54	0.42	9.84	5.98	3.90	0.63
	20	1.68	0.17	1.57	0.42	9.84	5.95	3.90	0.62
M74HC4852YRM13TR	**21**	1.68	0.20	1.51	0.42	9.84	5.99	3.90	0.61
	22	1.68	0.18	1.56	0.43	9.84	5.98	3.90	0.62
	23	1.69	0.16	1.52	0.42	9.86	5.95	3.89	0.63
	24	1.68	0.16	1.51	0.41	9.86	5.97	3.89	0.63
	25	1.68	0.19	1.52	0.42	9.84	5.95	3.90	0.61
	26	1.69	0.19	1.52	0.40	9.84	5.98	3.89	0.61
	27	1.70	0.17	1.56	0.42	9.85	5.97	3.89	0.62
	28	1.69	0.17	1.53	0.41	9.86	5.96	3.89	0.61
	29	1.70	0.16	1.52	0.42	9.85	5.98	3.90	0.62
	30	1.68	0.18	1.57	0.43	9.86	5.98	3.90	0.63
	mean	**1.7**	**0.2**	**1.5**	**0.4**	**9.8**	**6.0**	**3.9**	**0.6**
	stddev	**0.01**	**0.02**	**0.02**	**0.01**	**0.01**	**0.01**	**0.00**	**0.01**
	Cpk	**1.8**	**1.6**	**1.7**	**3.2**	**1.6**	**3.9**	**9.0**	**11.8**

6.1.3 Bonding strength (WBS/WBP)

Pull test summary

Unit / TV	P10B	R852	Z460
1	11.48	12.78	12.78
2	12.28	12.67	12.67
3	10.72	13.50	13.50
4	9.00	13.46	13.46
5	12.57	13.31	13.31
6	14.23	18.30	18.30
7	12.71	15.03	15.03
8	11.27	14.46	14.46
9	12.23	18.14	14.14
10	8.39	18.08	14.08
11	11.59	13.70	13.70
12	10.04	14.02	14.02
13	12.06	17.88	17.88
14	14.72	12.45	12.45
15	11.96	14.20	14.20
16	10.69	10.85	13.85
17	10.97	12.38	12.38
18	12.39	13.58	13.58
19	13.93	13.80	13.80
20	12.14	14.71	14.71
21	12.32	12.95	12.95
22	12.88	13.30	13.30
23	13.78	14.14	14.14
24	9.95	12.75	12.75
25	13.08	14.89	14.89
26	12.39	16.78	16.78
27	11.74	14.40	14.40
28	13.08	14.89	14.89
29	12.39	16.78	16.78
30	11.74	14.40	14.40
31	13.82	13.10	13.10
32	11.24	16.73	16.73
33	10.27	17.62	17.62
mean	**11.9**	**14.5**	**14.4**
stddev	**1.42**	**1.91**	**1.57**
Cpk	**1.87**	**1.84**	**2.20**

Shear test summary

Unit / TV	P10B	R852	Z460
1	35.48	35.85	35.85
2	36.46	34.81	34.81
3	36.03	35.33	35.33
4	34.47	35.33	35.33
5	36.47	35.79	35.79
6	35.53	38.65	38.65
7	35.87	38.49	38.49
8	36.48	36.6	36.6
9	34.68	37.22	37.22
10	34.48	34.41	34.41
11	38.72	37.88	37.88
12	35.36	36.76	36.76
13	34.28	39.92	39.92
14	33.07	41.28	41.28
15	38.03	35.76	35.76
16	35.6	39.94	39.94
17	35.85	37.72	37.72
18	35.48	36.16	36.16
19	37.01	38.4	38.4
20	36.84	36.9	36.9
21	33.61	33.24	33.24
22	33.37	35.54	35.54
23	34.54	35.06	35.06
24	36.13	36.21	36.21
25	37.71	36.8	36.8
26	34.21	33.66	33.66
27	35.19	35.54	35.54
28	37.71	36.8	36.8
29	34.21	33.66	33.66
30	35.19	35.54	35.54
31	34.02	34.72	34.72
32	34.27	34.93	34.93
33	36.86	39.11	39.11
mean	**35.6**	**36.5**	**36.5**
stddev	**1.38**	**1.90**	**1.90**
Cpk	**3.69**	**2.85**	**2.85**

1.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL Higt Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled of moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.