PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	AMS/21/12663
1.3 Title of PCN	Power Management BU: ST1PS01 datasheet modification
1.4 Product Category	See product list
1.5 Issue date	2021-09-22

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Salvatore DI VINCENZO
2.1.3 Quality Manager	Giuseppe LISI

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General (Test Program)	SBL or PAT criteria or Scrap limit relaxation in case initially agreed with the customer	Final test : ST Shenzhen

4. Description of change		
	Old	New
4.1 Description	Electrical Parameter ILIM1 | a) High-side MOSFET switch current limit:580mA (min),700mA(typ),820mA(MAX) b) Low-side MOSFET switch current limit: 500mA(typ)	Electrical Parameter ILIM1 | High-side MOSFET switch current limit: 500mA(min), 1150mA(MAX)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	Yield Improvements. No impact on Quality and Reliability Characteristics on final product	

5. Reason / motivation for change	
5.1 Motivation	Following Divisional Commitments towards a continuous improvement philosophy, the Power Management BU implemented electrical specification changes on ST1PS01 product. In particular ILIM1 values range have been modified as follow ILIM1: 500mA(min), 1150mA(MAX). This is translated in a better service and an augmented product quality.
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	The traceability of the new parts will be ensured by different internal codification and QA number

7. Timing / schedule	
7.1 Date of qualification results	2021-09-05
7.2 Intended start of delivery	2021-12-20
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	12663 W6337_381-18- ST1PS01-UBA5_Flip_Chip_1000h.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-09-22

9. Attachments (additional documentations)
12663 Public product.pdf 12663 W6337_381-18- ST1PS01-UBA5_Flip_Chip_1000h.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	ST1PS01AJR	
	ST1PS01DJR	
	ST1PS01EJR	

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PCN Title : Power Management BU: ST1PS01 datasheet modification

PCN Reference : AMS/21/12663

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

ST1PS01DJR	ST1PS01EJR	ST1PS01AJR

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Reliability Evaluation Report

New Product Qualification

On

ST1PS01 (UBA501)
In
Flip Chip 8 bumps

General Information	
Product Lines	UBA501
Product Description	400mA Nano-Quiescent™ Synchronous step-down converter with voltage selection and power good
P/N	ST1PS01EJR
Product Group	AMS
Product division	General Purpose Analog & RF Power Management
Package	Flip Chip 8 bumps (M0) 1.14x1.44mm 400um pitch
Silicon Process technology	BCD8SP 3Metals option with thick passivation

Locations	
Wafer fab	Catania CTM8
Assembly plant	ASE (UBM + BUMPING) STS (back grinning+ Testing + sawing)
Reliability Lab	CATANIA
Reliability assessment	Pass

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	October-2018	7	Lucio Costa	Giuseppe Giacopello	Final Report

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

New Product qualification: **ST1PS01EJR** in Flip Chip on 1st Lot

The **ST1PS01EJR**.use the technology **BCD8SP** 3 Metal option with thick passivation and will be available on Flip Chip

FE:
BCD8sP 3M Thick Al/Thick Passivation is at Mat 20. In order to complete the FE option validation (with reference to 3M Thick Al) a total of 3 different Diffusion Lots are requested.

BE
The product is assembled in flip chip 8 bumps (M0) 1.14x1.44mm 400um pitch, with the following flow:

- ASE (UBM + BUMPING)
- STS (back grinning+ Testing + sawing)

It is part of the "WLCSP Transfer to STS - GPA DIV Project".

3 assy lots are requested

Product mission profile
Product life duration: 5 years with a median value of Junction temperature of 50°C and Duty Cycle 50%.
In order to guarantee the product life duration (Arrhenius derating) the Equivalent reliability stress will be reduced to 500h.
However, in order to cover possible different mission profile, the reliability verification will continue until 1000h.

3.2 Conclusion

The evaluation plan has been fulfilled without exception.

Final Reliability Evaluation Report is positive.

4 DEVICE CHARACTERISTICS

4.1 Device description

The ST1PS01 is a Nano-Quiescent™ miniaturized synchronous step-down converter able to provide up to 400mA output current from an input voltage from 1.8 to 5.5V.
This converter is specifically designed for applications where high efficiency and small application area are the key factors.

4.2 Construction note

	P/N ST1PS01EJR
Wafer/Die fab. information	
Wafer fab manufacturing location	CT8
Technology	BCD8
Process family	BCD8SP 3Metals option with thick passivation
Die finishing back side	RAW SILICON
Die size	1140 x 1440 micron
Assembly information	
Assembly site	ST SHENZHEN -CHINA
Package description	CSPS0.4 7-10
Final testing information	
Testing location	SHENZHEN
Tester	Teradyne (ETS364)
Test program	ST1PS01E_CUT2_1/2/3

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Commercial Product	Assy Lot	Package	Line	Raw Line
1	ST1PS01EJR	GK7510WM	Flip Chip 8 bumps (M0) 1.14x1.44mm 400um pitch	UBA5	EZM0*UBA5BBE
2		GK82415D			EZM0*UBA5BC5
3		GK8291GL			EZM0*UBA5BD5

5.2 Test plan and results summary

P/N ST1PS01EJR

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note[1]
						Lot 1	Lot 2	Lot 3	
Die Oriented Tests									
HTOL	Y	JESD22 A-108	Ta = 125°C BIAS =+6.5V		**168h**	0/77	0/77	0/77	
					500 h	0/77	0/77	0/77	
					1000 h	0/77	0/77	0/77	
HTS	Y	JESD22 A-103	Ta = 150°C		**168 h**	0/25	0/25	0/25	
					500 h	0/25	0/25	0/25	
					1000 h	0/25	0/25	0/25	
PC		JESD22 A-113	Oven Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass	Pass	
THS	Y	JESD22 A-101	Ta = 85°C, Rh=85%		**168 h**	0/25	0/25	0/25	
					500 h	0/25	0/25	0/25	
					1000 h	0/25	0/25	0/25	
THB	Y	JESD22 A-101	Ta = 85°C, Rh=85% BIAS=+5,5V		**168 h**	0/25	0/25	0/25	
					500 h	0/25	0/25	0/25	
					1000 h	0/25	0/25	0/25	
TC	Y	JESD22 A-104	Ta = -40°C to 125°C		**100 cy**	0/25	0/25	0/25	
					200 cy	0/25	0/25	0/25	
					500 cy	0/25	0/25	0/25	
Other Tests									
ESD	N	JESD22-A114	HBM +/-1KV	3		PASS (EZM0*UBA5BD5)			
		JESD22-C101	CDM +/-500V	3		PASS (EZM0*UBA5BD5)			
LU	N	JESD78	Current Inj.Overvoltage +/- 100mA	6		PASS (EZM0*UBA5BD5)			

[1] All The samples have been assembled on chip boards according to IPC /JEDEC J-STD 020D

6 ANNEXES

6.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices	As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance.
THS Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CDM**: Charged Device Model **HBM**: Human Body Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.