PRODUCT / PROCESS CHANGE INFORMATION

1. PCI basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCI No.	AMS/23/13973
1.3 Title of PCI	Qualification of UTL3 in UTAC Thailand for the assembly
1.4 Product Category	See product list
1.5 Issue date	2023-09-18

2. PCI Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Marcello SAN BIAGIO
2.1.2 Marketing Manager	Salvatore DI VINCENZO
2.1.3 Quality Manager	Jean-Marc BUGNARD

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	Assembly : UTAC Calamba

4. Description of change		
	Old	New
4.1 Description	Assembly line : - UTL1 in UTAC Thailand (using ASM Aero as WB machine and FT in UTL1)	Assembly line : - UTL1 in UTAC Thailand (using ASM Aero as WB machine and FT in UTL1) - UTL3 in UTAC Thailand (using ASM Aero as WB machine and FT in UTL1)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	ST will increase the production capacity and provide a better delivery support to our customers. UTL3 is another plant of UTAC Thailand. The change is considered minor and announced through a PCI because the qualification on UTL3 is an exact copy-paste from UTL1 assembly process.
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	New Finished good codes

7. Timing / schedule	
7.1 Date of qualification results	2023-08-28
7.2 Intended start of delivery	2023-11-30
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13973 preliminary-ReliabilityEvaluationReport_UL1to3-v2.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2023-09-18

9. Attachments (additional documentations)
13973 Public product.pdf 13973 preliminary-ReliabilityEvaluationReport_UL1to3-v2.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STG3856QTR	
	STG3692QTR	
	LD59150PUR	
	LDLN050PU33R	
	TSB572IQ2T	

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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCI Title : Qualification of UTL3 in UTAC Thailand for the assembly

PCI Reference : AMS/23/13973

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

LD59150PUR	TSB572IQ2T	STG3692QTR
LDLN050PU33R	STG3856QTR	

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Internal Reliability Evaluation Report

Capacity expansion from UTL1 to UTL3

General Information	
Product Description	Low Low pow. 36V RtoR Dual OpAmplifiers, IO-LINK IC Device
P/N	TSB572, L6364Q
Product Group	AMG
Product division	GPA&RF, IPC
Package	FPN 3X3, FPN 4X4
Silicon Process technology	BICMOS40, SOIBCD6SV2

Locations	
Wafer fab	ST Singapore, ST Agrate
Assembly plant	UTAC THAI LIMITED UTL3
Reliability Lab	UTAC
Reliability assessment	In progress

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this qualification is to qualify UTAC UTL3 , Capacity expansion from UTL1, on the selected above described products , standard version, in FPN 3X3, 4X4, 2.2X1.4 packages.
The qualification plan is based on the similarity and based on the JESD47 specification.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Low-power, 2.5 MHz, RR IO, 36 V BiCMOS operational amplifier

Features

- Low-power consumption: 380 µA typ.
- Wide supply voltage: 4 V - 36 V
- Rail-to-rail input and output
- Gain bandwidth product: 2.5 MHz
- Low input bias current: 30 nA max.
- No phase reversal
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- Automotive grade
- Small SMD packages
- 40 V BiCMOS technology
- Enhanced stability vs. capacitive load

Applications

- Active filtering
- Audio systems
- Automotive
- Power supplies
- Industrial
- Low/high side current sensing

Maturity status link
TSB571, TSB572

Related products	
TSB611	For below 100 µA solution
TSB711	For a higher precision
TSB712	

Description

The TSB571 (single) and TSB572 (dual) operational amplifiers offer an extended voltage operating range from 4 V to 36 V and rail-to-rail input/output.

The TSB571 and TSB572 give a very good speed/power consumption ratio with a 2.5 MHz gain bandwidth product and a consumption of 380 µA typically only at 36 V supply voltage.

Stability and robustness of these devices make them an ideal solution for a wide voltage range of applications.

Dual channel transceiver IC for SIO and IO-Link sensor applications

QFN20L (4x4 mm)

CSP19 (2.5x2.5 mm)

Product status link
L6364

Product summary		
Order code	L6364Q	L6364W
Package	QFN 20L	CSP 19
Packing	Tape & Reel	Tape & Reel

SUSTAINABLE TECHNOLOGY

Features

- Supply voltage from 5 V to 35 V
- 2.5 V to 5 V compatible I/Os
- 3.3 V and 5 V, 50 mA linear regulators
- 50 mA DC-DC regulator with configurable frequency (0.5 MHz to 2 MHz) & voltage (5 V to 10.5 V)
- Low dissipative (5 Ω) CQ and DIO output stages configurable in high side, low side, push/pull
- Configurable reporting threshold (0.11 A to 0.25 A) of current limitation for CQ and DIO lines
- Configurable reporting threshold (0.22 A to 0.5 A) of current limitation for CQ//DIO line (Join Mode)
- Fully protected:
  - Embedded reverse polarisation diode (D_{OUT} pin)
  - Full zero current reverse polarity between V_{PLUS}, CQ, DIO and PGND pins
  - Configurable (up to 216°C) thermal shutdown threshold
  - 7-bit, calibrated, temperature measurement
  - Configurable (6.0 V to 15 V) V_{PLUS} undervoltage detection
  - CQ and DIO short-circuit current limit and reporting
- -40 to +150°C operating temperature
- Suitable to drive L, C and R loads
- Quartz-free IO-Link clock extraction and timing generation at COM2 (38.4k Baud) and COM3 (230.4k Baud)
- Integrated UART peripheral with M-sequence handling (inc. checksum) for all IO-Link sequences according to specification v1.1
- Multi octet UART mode for M-sequence size up to 15 octets
- Single octet UART mode for unlimited M-sequence size and continuous data transfer
- Transparent UART mode for special applications
- CQ and DIO switching time = 100 ns (2 kΩ//2.2 nF load)
- 8 V Zener limits for fast demagnetization of inductive loads
- Two LED drivers with configurable (up to 8 mA) current
- Design to meet application requirements:
  - ESD IEC 61000-4-2 protection to 4 kV
  - EMC protection against surge (500 Ω coupling) above ±2A/50 µs
- Smart format QFN-20L 4x4 mm and CSP-19 2.5x2.5 mm packages

Application

- Industrial sensors
- Factory automation
- Process control

4.2 Construction note

	Extention Qualification	
	P/N TSB572	**P/N L6364Q**
Wafer/Die fab. information		
Wafer fab manufacturing location	ST Singapore	ST Agrate
FE Process family	BICMOS40	SOIBCD6SV2
Die finishing back side	Raw Silicon	Raw Silicon
Die size	1070 x 1010 µm²	2577x2577 µm²
Bond pad metallization layers	AlSiCu 1.350 µm	Ti/AlCu/TiN 3.025 µm
Passivation type	SiN (nitride)	TEOS/SiN/Polyimide
Assembly information		
Assembly site		
Package description	FPN 3X3	FPN 4X4
Molding compound	Sumitomo G770HCD	Sumitomo EME G700LTD
Frame material	DFN 3x3/0.65mm Pitch	L/F 4x4x1 pitch 0.5 Cu/alloy/Ag
Die attach material	Ablestick 8006NS non-conductive	Ablebond 8200T
Wires bonding materials/diameters	Gold 1.0mils	Gold 1.0 mil Au
Lead finishing process	Sn plating	Sn plating

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product	Comments
1	FPN 3X3	TSB572IQ2T	
2	FPN 3X3	TSB572IQ2T	
3	FPN 3X3	TSB572IQ2T	
1	FPN 4X4	L6364Q	
2	FPN 4X4	L6364Q	
3	FPN 4X4	L6364Q	

Detailed results in below chapter will refer to P/N and Lot #.

5.2 Test plan and results summary

P/N TSB572, L6364Q)

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS						Note
						A236			U1MD			
						Lot 1	Lot 2	Lot 3	Lot 1	Lot 2	Lot 3	
Package Oriented Tests												
PC		JESD22 A-113	Drying 24 H @ 125°C		Final	**160**	**160**	**160**	**160**	**160**	**160**	
			Store 168h @ 85°C / 85% RH			**160**	**160**	**160**	**160**	**160**	**160**	
			Over Reflow @ Tpeak=260°C 3 times			**160**	**160**	**160**	**160**	**160**	**160**	
uHAST	Y	JESD22 A-118	T°=130°C; Pressure=2.3 atm; HR=85%		96 H	**80**	**80**	**80**	**80**	**80**	**80**	
HTSL	Y	JESD22 A-103	Ta = 150°C		500 H	**80**	**80**	**80**	**80**	**80**	**80**	
					1000 H	**80**	**80**	**80**	**80**	**80**	**80**	
TC	Y	JESD22 A-104	Ta = -55°C to 150°C		500 cy	**80**	**80**	**80**	**80**	**80**	**80**	
					1000 cy	**80**	**80**	**80**	**80**	**80**	**80**	
Other Tests												
SD		J-STD 002	solderability		5 units	**5**	**5**	**5**	**5**	**5**	**5**	
BPS	N	MIL – STD683	Bond Pull Strength	5	30 bonds / 5 devices	**30**	**30**	**30**	**30**	**30**	**30**	
BS	N	AECQ100 - 001	Bond shear strength	5	30 bonds / 5 devices	**30**	**30**	**30**	**30**	**30**	**30**	

In case of rejects include a short description of the failure analysis and corrective actions.

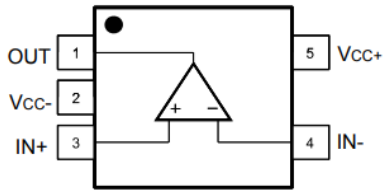
6 ANNEXES

6.1 Device details

6.1.1 Pin connection

P/N TSB572:

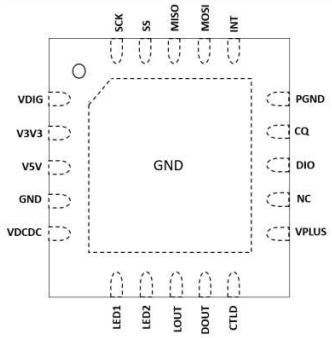
Figure 1. **Pin connections (top view)**



SOT23-5

P/N L6364A

Figure 2. **Package and pin-out - QFN**

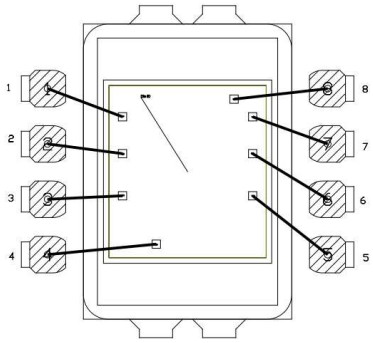


TOP THROUGH VIEW

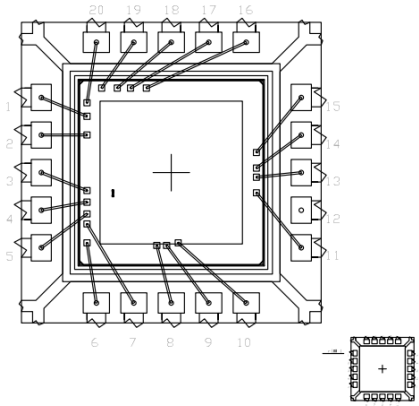
N.B. GND pin and Exposed pad to be shorted on PCB

6.1.2 Bonding diagram

P/N TSB572 :



P/N L6364A



Package outline/Mechanical data

P/N TSB572:

TITLE: POA DFN 3x3x0.80 8L PITCH 0.65 A.G. Side Wall Plate
PACKAGE TYPE: Plastic no-lead
PACKAGE CODE: A03Y
PACKAGE WEIGHT: 21.2 mg/unit
PLANT CODE: 997G
JEDEC REFERENCE NUMBER: MO-229

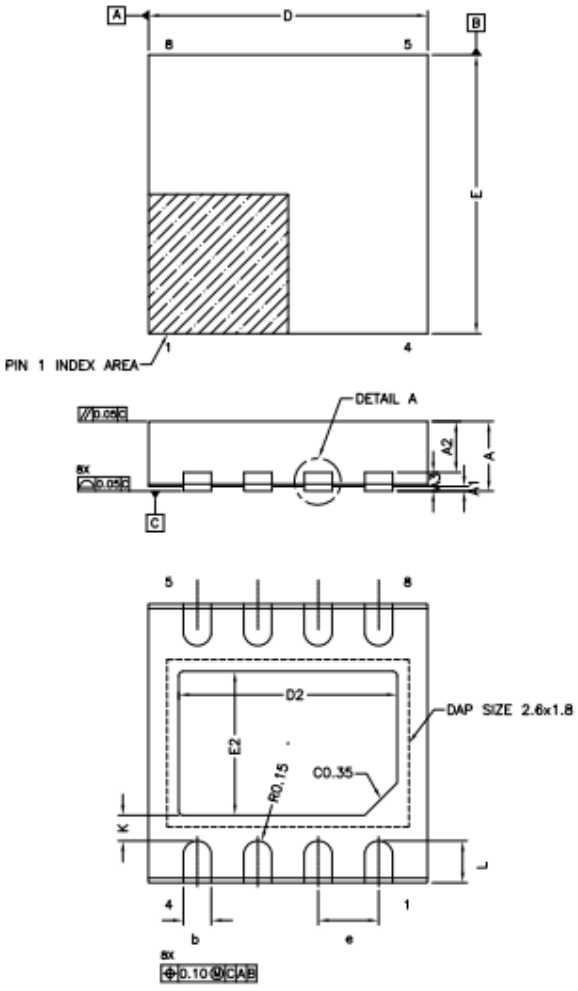
PACKAGE DIMENSIONS

DATABOOK				
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	0.70	0.75	0.80	
A1	0.0		0.05	
A3		0.20 Ref.		
b	0.25	0.30	0.35	
D	2.95	3.00	3.05	
D2	2.25	2.35	2.45	
e		0.65 BSC		
E	2.95	3.00	3.05	
E2	1.45	1.55	1.65	
L	0.35	0.45	0.55	
K		0.275 Ref.		
N		8		

SYMBOL	TOLERANCE OF FORM AND POSITION	
	DATABOOK	
aaa	0.15	
bbb	0.10	
ccc	0.10	
ddd	0.05	
eee	0.08	

PLANT CODE: 997G

DFN 8L 3X3X0.80 PITCH 0.65



P/N L6364A:

TITLE: VFQFPN 4x4x1.0 20L PITCH 0.50

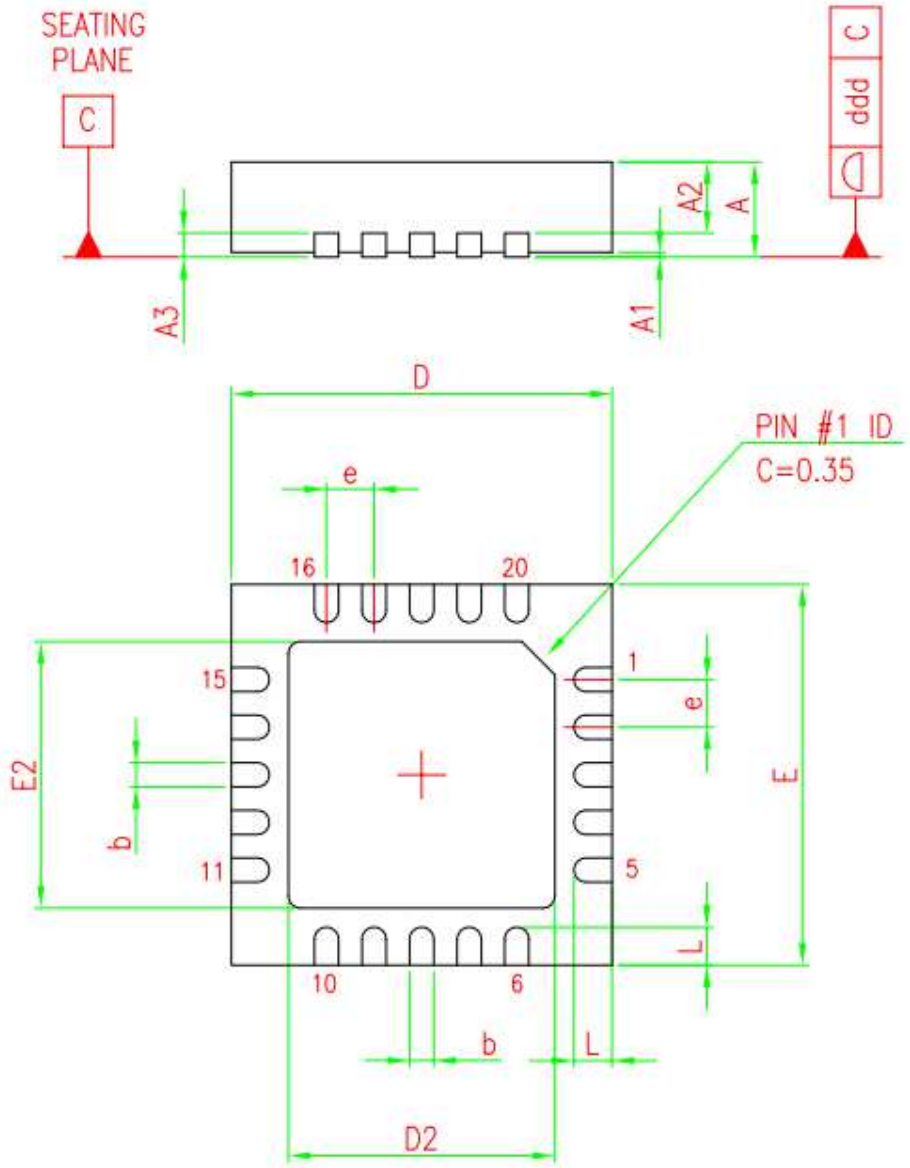
PACKAGE CODE: ZU

JEDEC/EIAJ REFERENCE NUMBER: MO-220 – VARIATION VGGD-11

TABLE.2 / FIGURE.2: ASSEMBLY PLANT 997G

	DIMENSIONS					
	DATABOOK (mm)			DRAWING (mm)		
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	0.80	0.85	0.90
A1		0.02	0.05	0.00		0.05
A2		0.65	1.00		0.65	
A3		0.25			0.20	
b	0.18	0.23	0.30	0.20	0.25	0.30
D	3.85	4.00	4.15	3.90	4.00	4.10
D2	SEE EXPOSED PAD VARIATIONS			SEE EXPOSED PAD VARIATIONS		
E	3.85	4.00	4.15	3.90	4.00	4.10
E2	SEE EXPOSED PAD VARIATIONS			SEE EXPOSED PAD VARIATIONS		
e	0.45	0.50	0.55	0.45	0.50	0.55
L	0.30	0.40	0.50	0.30	0.40	0.50
ddd			0.08			0.08

	EXPOSED PAD VARIATIONS					
	D2			E2		
VARIATION	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.70	2.80	2.90	2.70	2.80	2.90
B	2.60	2.70	2.80	2.60	2.70	2.80



Test name	Description	Purpose
Die Oriented		
HTOL Higt Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.