



## **PRODUCT/PROCESS CHANGE NOTIFICATION**

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**PCN AMS-APD/12/7204**  
**Dated 04 Oct 2012**

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**Front end HCMOS5 & HF5CMOS technologies additional  
capacity in ST Crolles (France)**

**Table 1. Change Implementation Schedule**

Forecasted implementation date for change	27-Sep-2012
Forecasted availability date of samples for customer	27-Sep-2012
Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability	27-Sep-2012
Estimated date of changed product first shipment	03-Jan-2013

**Table 2. Change Identification**

Product Identification (Product Family/Commercial Product)	See attached
Type of change	Waferfab additional location
Reason for change	To improve ST customer service and increase front end capacity
Description of the change	Progressing on the activities related to HCMOS5 and HF5CMOS technologies manufacturing expansion, ST is glad to announce additional production site in ST Crolles (France). Current process is UMC Taiwan. Regarding samples availability: pieces from V63201 product line will be available end of October 2012; others products only upon customers request. Please enter a non-standard samples order in the system mentioning in comment "PCN7204 qualification" & send the SO# to Angelique DUCHENE, then she will manage to have this order confirmed.
Change Product Identification	On the label of the packaging WX code will change from LE to VJ
Manufacturing Location(s)	

### Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



## DOCUMENT APPROVAL

Name	Function
Camiolo, Jean	Marketing Manager
De marco, Alberto	Product Manager
Bugnard, Jean-Marc	Q.A. Manager

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**PRODUCT/PROCESS  
CHANGE NOTIFICATION**

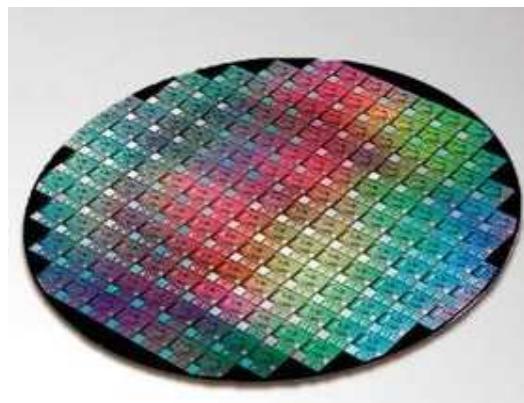
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PCN AMS-APD/12/7204

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***Analog, MEMS and Sensor Group***

**Additional site for HCMOS5/HF5CMOS technologies for Hirel&standard products in ST Crolles**



**WHAT:**

Progressing on the activities related to HCMOS5 and HF5CMOS technologies manufacturing expansion, ST is glad to announce additional production site in ST Crolles (France)

Material	Current process	Modified process
Assembly location	UMC Taiwan	ST Crolles

For the complete list of the part numbers affected by the change, please refer to the attached Products list.

**WHY:**

To improve service to ST Customers and increase capacity for the affected technologies.

**HOW:**

The change that covers additional hirel&standard products, is already qualified through attached report.

Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

**WHEN:**

Production in ST Crolles France for AMS is forecasted end of November 2012.

**Marking and traceability:**

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by marking on label as per below description:

**STMicroelectronics**

Manufactured under patents or patents pending	
Assembled in: <b>COUNTRY</b>	
PbFree	Second level interconnect
MSL: <b>X</b>	Bag sealed date: XX XXX XXXX
PBT: <b>XXX°C</b>	Category: ECOPACK/Rohs
<b>TYPE</b>	Commercial product Finished good
<b>Total Qty: XXXX</b>	
<b>Trace codes</b> PPYWWLLL WX TF PPYWWLLL WX TF PPYWWLLL WX TF	
<b>Marking</b>	<b>MARKING</b>
<b>Bulk Id Number</b>	
<b>Bar code</b>	
Please provide the bulk Id for any inquiry	

WX code will change  
from LE to VJ

MSL: Moisture sensitivity level as per Jedec J-std-020C

PBT: Peak body temperature (maximum temperature for reflow soldering)

ECOPACK: present if leadfree component

TYPE: product name

Trace codes: PP: assembly plant code

Y: last digit of the year of assembly

WW: Week of assembly

LL1: lot number

WX: Diffusion plant code

TF : Test&finishing plant code

Bulk ID number: 1: Product level (T for tested product)

Y: last digit of the year

P: Plant code

WW: Week of labeling

LOT: Sequential number for lot

BOXX: Sequential number for box

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.

There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

In any case, first shipments may start earlier with customer's written agreement.

## Reliability Report

*H5/HF5 Technologie Additional Front End plant  
Qualification to CRO200 plant*

General Information		Locations
Product Line	3021 & V632	CRO200
Product Description	Rail to rail high speed comparator & Dual Rail to rail operational amplifier	
P/N	TS3021ILT & TSV632IDT	
Product Group	AMS	
Product division	Analog	
Package	SOT23-5 & SO8	Carsem (SOT23-5) & BSK (SO8)
Silicon Process technology	HF5 & H5	
Production mask set rev.	1	
Maturity level step	from 10 to 30	Grenoble

## DOCUMENT INFORMATION

Report ID 2012-W16 H5/HF5

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	16-Apr-2012	24	X. Gagnard		First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.  
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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## **1 APPLICABLE AND REFERENCE DOCUMENTS**

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD46	Customer notification of product process changes by semiconductors suppliers

## **2 GLOSSARY**

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

## **3 RELIABILITY EVALUATION OVERVIEW**

### **3.1 Objectives**

Through this qualification plan, the H5 & HF5 technology transfer is evaluated, to be diffused at CROLLES 200mm plant instead of UMC subcontractor.

This qualification plan is divided in 3 steps:

- 1<sup>st</sup> step: qualification of standard technology
- 2<sup>nd</sup> step: H5 automotive technology qualification
- 3<sup>rd</sup> step: HF5 automotive technology qualification

This report concerns the 1<sup>st</sup> step, concerning the qualification of the standard uses of the H5 & HF5 technology.

Based on similarity analysis, linked to qualification plan, 2 tests vehicles are used:

- 3021 line for HF5 technology
- V632 line for H5 technology

These 2 lines are also evaluated for automotive market, and will be considered for 2<sup>nd</sup> step.

### **3.2 Conclusion**

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

The H5 & HF5 technology are qualified to address standard market.

## 4 DEVICE CHARACTERISTICS

### 4.1 Device description



TS3021

Rail-to-rail 1.8 V high-speed comparator

#### Features

- Propagation delay: 38 ns
- Low current consumption: 73  $\mu$ A
- Rail-to-rail inputs
- Push-pull outputs
- Supply operation from 1.8 to 5 V
- Wide temperature range: -40° C to +125° C
- High ESD tolerance: 5 kV HBM / 300 V MM
- Latch-up immunity: 200 mA
- SMD packages

#### Applications

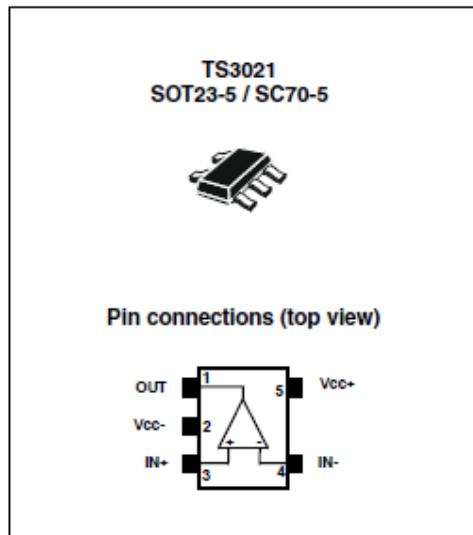
- Telecom
- Instrumentation
- Signal conditioning
- High-speed sampling systems
- Portable communication systems

#### Description

The TS3021 single comparator features high-speed response time with rail-to-rail inputs. With a supply voltage specified from 2 to 5 V, this comparator can operate over a wide temperature range: -40° C to +125° C.

The TS3021 comparator offers micropower consumption as low as a few tens of microamperes thus providing an excellent ratio of power consumption current versus response time.

The TS3021 includes push-pull outputs and is available in small packages (SOT23-5 and SC70-5).





# TSV632, TSV632A, TSV633, TSV633A TSV634, TSV634A, TSV635, TSV635A

Dual and quad rail-to-rail input/output  
60  $\mu$ A 880 kHz operational amplifiers

## Features

- Rail-to-rail input and output
- Low power consumption: 60  $\mu$ A typ at 5 V
- Low supply voltage: 1.5 V - 5.5 V
- Gain bandwidth product: 880 kHz typ
- Unity gain stability
- Low power shutdown mode: 5 nA typ
- Low offset voltage: 800  $\mu$ V max (A version)
- Low input bias current: 1 pA typ
- EMI hardened op-amps
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40° C to +125° C

## Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

## Description

The TSV63x series of dual and quad operational amplifiers offers low voltage operation and rail-to-rail input and output.

This family features an excellent speed/power consumption ratio, offering a 880 kHz gain-bandwidth product while consuming only 60  $\mu$ A at 5 V supply voltage. The devices also feature an ultra-low input bias current and have a shutdown mode (TSV633, TSV635).

These features make the TSV63x family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

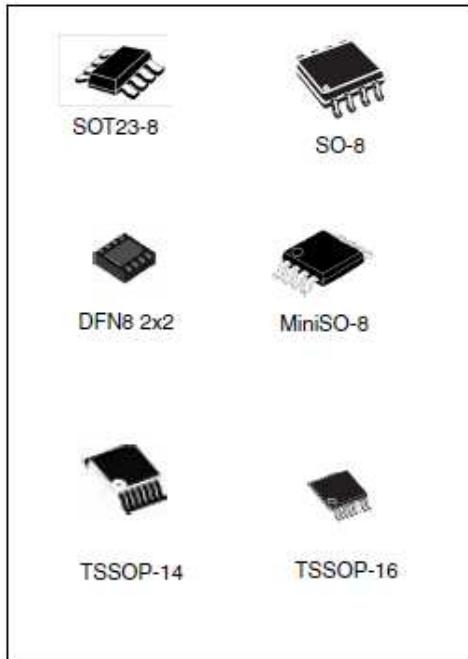


Table 1. Device summary

Reference	Dual version		Quad version	
	Without standby	With standby	Without standby	With standby
TSV63x	TSV632	TSV633	TSV634	TSV635
TSV63xA	TSV632A	TSV633A	TSV634A	TSV635A

## 4.2 Construction note

Site Xfer AMJ9		
	P/N TS3021ILT	P/N TSV632IDT
<b>Wafer/Die fab. information</b>		
Wafer fab manufacturing location	CROLLES 200mm	
Technology	HF5CMOS	HCMOS5LA
Process family	HF5	H5
Die finishing back side	Lapped Silicon	Raw Silicon
Die size	720 x 820 $\mu\text{m}^2$	1020 x 1090 $\mu\text{m}^2$
Bond pad metallization layers	AlCu	AlCu
Passivation type	PSG + Nitride	PSG+Nitride+PIX
Poly silicon layers	NA	NA
<b>Wafer Testing (EWS) information</b>		
Electrical testing manufacturing location	Singapore	Singapore
Tester	ASL1000	ASL1000
Test program	T3021AW1	TV632PW2
<b>Assembly information</b>		
Assembly site	CARSEM	BSK
Package description	SOT23-5	SO8
Molding compound	CEL8240HF	EME-G700K
Frame material	Cu	Cu
Die attach process	Glue	Glue
Die attach material	QMI519	8601S-25
Die pad size	75 x 75 $\mu\text{m}^2$	75 x 75 $\mu\text{m}^2$
Wire bonding process	Wire	Wire
Wires bonding materials/diameters	Au 1mil	Cu 1mil
Lead finishing process	Pre metallised	Pre metallised
Lead finishing/bump solder material	NiPdAu	NiPdAu
Substrate supplier for BGA	NA	NA
<b>Final testing information</b>		
Testing location	CARSEM	BSK
Tester	ASL1000	ASL1000
Test program	T3021AF3	TV632BF

## 5 TESTS RESULTS SUMMARY

### 5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	J135BPT	CA1145N60	1146ZRY	SOT23-5	3021	RL: IYWY*3021BTJ
2	J131MAC	CA1146N30	CZ1480EB	SO8	V632	RL: ID07*V632BTJ
3						

Detailed results in below chapter will refer to P/N and Lot #.

### 5.2 Test plan and results summary

P/N TS3021ILT & TSV632IDT

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1	Lot 2	Lot 3	
<b>Die Oriented Tests</b>									
HTB	N	JESD22 A-108	T <sub>j</sub> = 125°C, BIAS	156	168 H 1000 H	0/78 0/78	0/78 0/78		
HTSL	N	JESD22 A-103	T <sub>a</sub> = 150°C	156	168 H 1000 H	0/78 0/78	0/78 0/78		
ELFR	N	AEC Q100 - 008	T <sub>j</sub> = 125°C, BIAS	1000	48H	0/800	0/200		
<b>Package Oriented Tests</b>									
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	Pass	Pass		
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	234	96 H 168 H	0/78 0/78	0/156 0/78		
TC	Y	JESD22 A-104	T <sub>a</sub> = -65°C to 150°C	156	100 cy 1000 cy	0/78 0/78	0/78 0/78		
THB	Y	JESD22 A-101	T <sub>a</sub> = 85°C, RH = 85%, BIAS	156	168 H 1000 H	0/80 0/80	0/78 0/78		
<b>Other Tests</b>									
ESD	N	AEC Q101-001, 002 and 005	HBM CDM MM	6		2kV	4kV		
				6		1500V	tbd		(2)
				6		200V	300V		
LU	N	AEC Q100 - 004	Current Inj. Overvoltage	12	+200mA	In progress	Pass		(1)

Note (1): Stress in progress, should be done by Hot stress for Automotive qualification

Note (2): CDM stress performed at Catania ST Plant

In case of rejects include a short description of the failure analysis and corrective actions.

## **6 ANNEXES**

### **6.1 Device details**

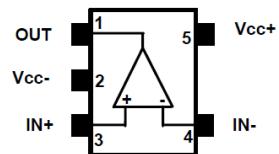
#### **6.1.1 Pin connection**

SOT23-5

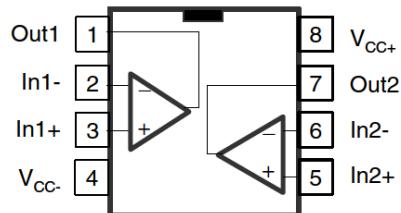
**TS3021**  
**SOT23-5 / SC70-5**



**Pin connections (top view)**



SO8



**TSV632IDT/IST/ILT/IQ2T**  
**SO8/Mini-SO8/SOT23-8/DFN8**

### 6.1.2 Block diagram

Not available

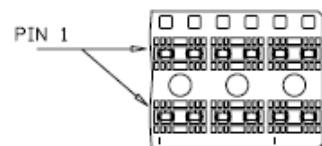
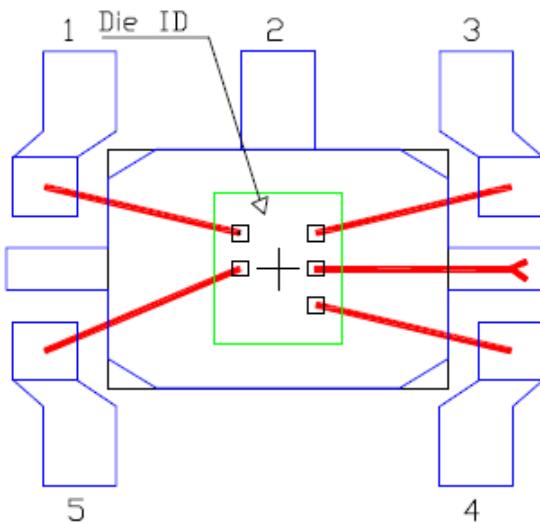
### 6.1.3 Bonding diagram

For SOT23-5 package

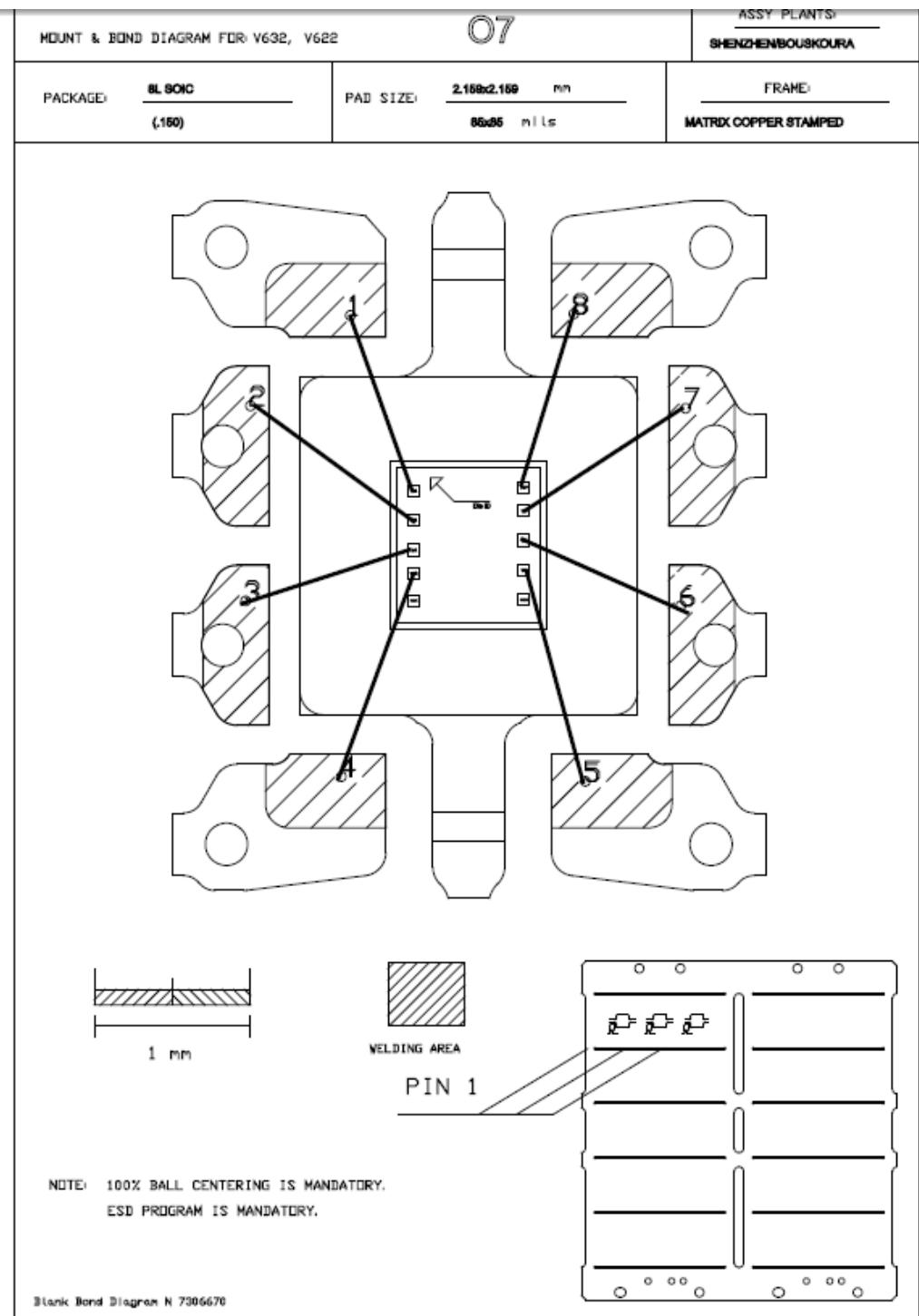
BONDING DIAGRAM FOR LINE : 3021

PACKAGE : W Y

FRAME PAD :  $.064 \times .045$  inch  
 $1,626 \times 1,143$  mm



SOT23 5L  
BLANK BOND. DIAG. REF. : SFT1848



### 6.1.4 Package outline/Mechanical data

For SOT23-5 :

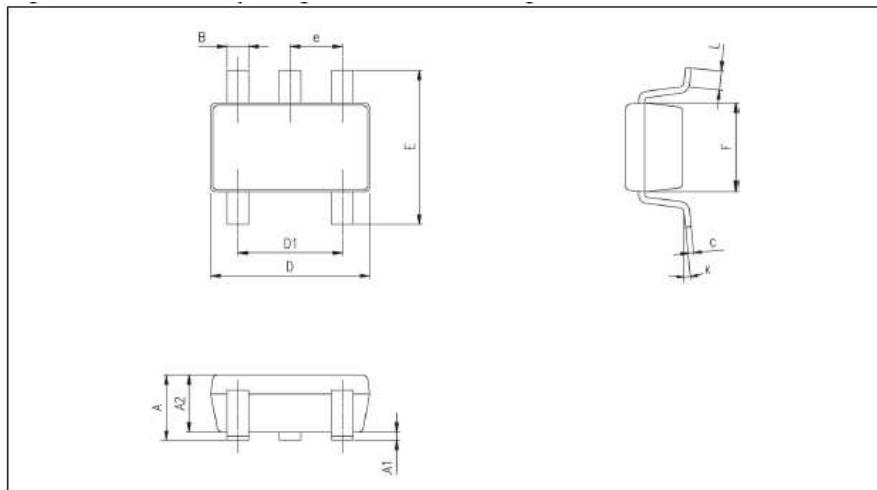


Table 6. SOT23-5L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0 degrees		10 degrees			

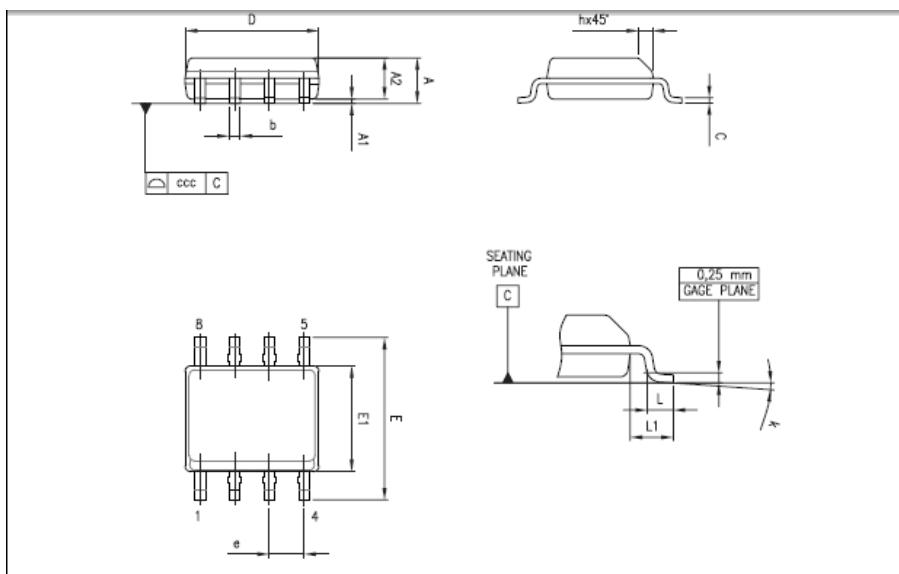


Table 11. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	

## 6.2 Tests Description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTOL</b> High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
<b>HTB</b> High Temperature Bias		
<b>HTRB</b> High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way.
<b>HTFB / HTGB</b> High Temperature Forward (Gate) Bias		To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
<b>HTSL</b> High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
<b>ELFR</b> Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
<b>Package Oriented</b>		
<b>PC</b> Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
<b>AC</b> Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>TC</b> Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>TF / IOL</b> Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
<b>THB</b> Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
<b>Other</b>		
<b>ESD</b> Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
<b>LU</b> Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

This qualification follow announcement done in 2010 (PCN APM/MHD/10/5340), see on following page qualification results raised at that time.



# Qualification Report

*On HCMOS5 Products*

General Information		Locations	
Product Line	201201	Wafer fabrication location	CROLLES 8"
Product Description	3W filter-free class D stereo audio power amplifier	UBM plant location	Tours France
Commercial Product	TS2012EIJT	Assembly plant location	Shenzhen China
Product Group	LINEAR & INTERFACE	Final test plant location	Shenzhen China
Product Division	IMS - APM GROUP		
Package Description	CSP500 (flip chip)		
Silicon Process Technology	HCMOS5		

General Information		Locations	
Product Line	496201	Wafer fabrication location	CROLLES 8"
Product Description	3W filter-free class D mono audio power amplifier	UBM plant location	Tours France
Commercial Product	TS4962MEIJT	Assembly plant location	Shenzhen China
Product Group	LINEAR & INTERFACE	Final test plant location	Shenzhen China
Product Division	IMS - APM GROUP		
Package Description	CSP500 (flip chip)		
Silicon Process Technology	HCMOS5		

## DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
0.1	January 2010	6	F.Murillon O. Girard F. Paccard	Original document

Reliability is the attitude of element to satisfy required function in fixed conditions during established time.

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.  
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

## 1 RELIABILITY EVALUATION OVERVIEW

### 1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on 2012 device used as test vehicle in order to qualify HCMOS5 diffused in Crolles 8". And to present product performances comparison for 4962. These products are assembled as flip chip in ST plant in Shenzhen (China)

### 1.2 Conclusion

The final reliability results are positive for all stressed lots.  
All product performances comparisons are compliant with ST rules.

## 2 DEVICE CHARACTERISTICS

### 2.1 Device description

\* The TS2012 is a differential Class-D BTL stereo power amplifier. It is able to drive up to 2.3W into a 4 Ohms load and 1.4W into a 8 Ohms load at 5V. It achieves outstanding efficiency (88%typ.) compared to classical Class-AB audio amps.

The gain of the device can be controlled via two external gain-setting resistors. Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms. A standby function (active low) allows the reduction of current consumption to 10nA typ.

\* The TS4962M is a differential Class-D BTL mono power amplifier. It is able to drive up to 2.3W into a 4 Ohms load and 1.4W into a 8 Ohms load at 5V. It achieves outstanding efficiency (88%typ.) compared to classical Class-AB audio amps.

The gain of the device can be controlled via two external gain-setting resistors. Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms. A standby function (active low) allows the reduction of current consumption to 10nA typ.

### 2.2 Traceability

#### 2.2.1 Wafer fabrication information

- Wafer fabrication manufacturing location: Crolles 8" in France
- Technology: HCMOS5
- Die size 4962 : 1.63 mm x 1.63 mm
- Die size 2012 : 2.15 mm x 2.15 mm
- Passivation type: PSG / SiN



## 2.2.2 Assembly information

Assembly site	Shenzen China
Package description	CSP 500 (flip chip)
Bumps material	SnAgCu 300 microns / pitch 500 microns

## 3 RELIABILITY TESTS RESULTS

### 3.1 Bump shear test results

	Ball shear : mean lot	Ball diameter : mean lot	Tearing out : Mode 1
J920FZJ_2012	361g	309µm	OK
J924BKE_2012	351g	309µm	OK
J935CAW_4962	358g	311µm	OK
	Min spec 240g	Min spec 284µm	
	Max spec 520g	Max spec 334µm	

### 3.2 Electrical performances comparison

#### TS2012EIJT

Test parameter	Mean Comparison (J920FZJ)				Cpk comparison	
	UMC	CROLLES	Shift	Datas sheet	UMC	Crolles
Iccstby(nA)	508	520	2%	< 2µA	12.3	9.7
Fpwm(kHz)	290	289	0%	< 370 kHz	2.7	3.4
Icc(mA)	3.1	3.0	2%	< 5.5mA	4.9	4.4
VooL(mV)	1.4	2.1	0.7mV	< 25mV	3.7	3.9
VooR(mV)	1.7	1.8	0.1mV		3.7	2.1
ZinLp(Ohms)	27.4	29.7	8%	< 36 Ohms	2.0	2.6
ZinLn(Ohms)	27.5	30.0	9%		2.0	3.9
THD(%)	0.3	0.4	19%	typ 0.35	2.1	1.6
Gain6dB	6.1	6.0	0%	typ 6dB	14.1	12.2
Po4R(mW)	484	491	1%	typ 450mW	12.5	8.0
Po8R(mW)	296	298	1%	typ 300mW	6.8	7.2
CmrrR(dB)	68.6	68.1	1%	typ 62dB	1.5	2.2

TS4962MEIJT

Mean Comparison (J935CAW)				
Test parameter	UMC	CROLLES	Shift	Datas sheet
Iccstby(µA)	0.021	0.017	19.0%	< 0.5µA
Rstby(kOhms)	153	150	1.8%	typ 150 kOhms
Fpwm(kHz)	239	242	1.3%	< 370 kHz
Icc(mA)	1.63	1.57	3.7%	< 2.4mA
Voo(mV)	0.84	1.40	0.56 mV	< 25mV
THD(%)	0.6	0.6	0.0%	< 1%
Gain6dB	5.8	5.6	4.0%	typ 6dB
Po8R(mW)	0.33	0.32	3.0%	typ 400mW

Icc standby current is 20% lower which is an improvement.

### 3.3 Reliability test plan and results summary

#### Die oriented test

HTB	Test short description : High Temperature Bias				
	Batch_product	Conditions	Sample size	Duration	Fail/ tested
	J920FZJ_2012	Tj=150°C Vs=absolute max rating	78 x 1 Lot	1000 H	0/78
	J935CAW_4962	Tj=150°C Vs=absolute max rating	78 x 1 Lot	1000 H	0/78

#### Package oriented test

TMC	Test short description : Thermal Cycle				
	Batch_product	Conditions	Sample size	Duration	Fail/ tested
	J920FZJ	Ta =-65°C to 150°C thermal cycle	78 x 1 Lot	1000 cycles	0/78

#### ESD tests

ESD Model	Batch_product	Stress voltage (V)	Fail / tested
HBM	J920FZJ_2012	2000	0 / 3
	J935CAW_4962	2000	0 / 3
MM	J920FZJ_2012	200	0 / 3
	J935CAW_4962	200	0 / 3
CDM	J920FZJ_2012	750	0 / 3

All test above are compliant with below standards:

- MIL883C
- JEDEC JESD22
- ANSI ESD STM 5.1



**ESD** results on samples from receiving plant are aligned with results obtained on sending plant samples.

### 3.4 Bench test :

All below curves are conform to curves reported in TS2012EIJT datasheet.

<b>REJECTION</b>	
CMRR VS Common Mode Voltage	X
CMRR VS Frequency	X
PSRR VS Common Mode Voltage	X
PSRR VS Frequency	X
<b>CONSUMPTION</b>	
Current Consumption VS Power Supply Voltage	X
Output Power VS Power Supply Voltage	X
Efficiency VS Output Power	X
<b>ELECTRICAL CHARACTERISTICS</b>	
Input Impedance	X
Noise VN	X
Offset Output Voltage	X
Gain VS Frequency	X
PWM Frequency	X
<b>DISTORSION</b>	
THD+N VS Frequency	X
THD+N	X
<b>TIME</b>	
Rise-Fall Time	X
<b>CROSSTALK</b>	
Crosstalk VS Frequency	X
<b>SHORTCUT</b>	
Shortcut without Inductor VoH-Gnd	X
Shortcut without Inductor VoH-VoL	X
Shortcut with Inductor VoH-VoL 33µH	X
Shortcut with Inductor VoH-Gnd 33µH	X
<b>TEMPERATURE TEST</b>	
150°C	X



### **3.5 Die oriented tests**

These tests are performed in order to demonstrate the quality and reliability of devices subjected to an elevated temperature and reverse biased.

The purpose of this test is to detect surface defects such as poor passivation, presence of contaminants, metal corrosion, etc

### **3.6 Package oriented tests**

These tests are performed in order to check device life in various environmental conditions in an accelerated way.

Detectable failure mechanisms are metal corrosion and molding defect, cracking of die, breaking of wire bonding, and mechanical damage to the device case.

## **4 APPLICABLE AND REFERENCE DOCUMENTS**

Document reference	Short description
AEC-Q100	Stress test qualification for integrated circuits
SOP 2610	General product qualification procedure
Internal ST specification	Reliability Tests and criteria for qualifications (Corporate Q&R rules)
...	

## **5 GLOSSARY**

ESD	Electro Static Discharge
HTB	High Temperature Bias
T.C.	Thermal Cycle

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## Public Products List

PCN Title : Front end HCMOS5 & HF5CMOS technologies additional capacity in ST Crolles (France)

PCN Reference : AMS-APD/12/7204

PCN Created on : 16-NOV-2012

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

### ST COMMERCIAL PRODUCT

TS3021ICT	TS3021ILT	TS3021IYLT
TSV631AICT	TSV631AILT	TSV631ICT
TSV631ILT	TSV632AIDT	TSV632AILT
TSV632AIST	TSV632IDT	TSV632ILT
TSV632IQ2T	TSV632IST	TSV634AIPT
TSV634IPT	TSV634IQ4T	

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