PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/24/14639
1.3 Title of PCN	Additional capacity for SMLVT3V3 at same subcontractor in China
1.4 Product Category	SMLVT3V3
1.5 Issue date	2024-03-20

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Stephane CHAMARD
2.1.2 Marketing Manager	Philippe LEGER
2.1.3 Quality Manager	Jean-Paul REBRASSE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Machines	(Not Defined)	Subcontractor in China

4. Description of change		
	Old	New
4.1 Description	Assembly line in China	Assembly line in China with additional capacity
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No	

5. Reason / motivation for change	
5.1 Motivation	Standardization of assembly process and method for all TVS parts in SMB package. STMicroelectronics will increase its production capacity to better serve its customers through service improvement and lead time reduction.
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change	
6.1 Description	New Finished Good/Type print on carton labels

7. Timing / schedule	
7.1 Date of qualification results	2024-03-18
7.2 Intended start of delivery	2024-06-18
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	14639 24010QRP.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2024-03-20

9. Attachments (additional documentations)
14639 Public product.pdf 14639 SMLVT3V3 HD conversion.pdf 14639 24010QRP.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
SMLVT3V3	SMLVT3V3	

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Qualification Report

SMLVT3V3

General Information	
Product Line	*Protection*
Product Description	*Transil diode designed to protect sensitive 3.3 V equipment against transient overvoltages*
Product Perimeter	*SMLVT3V3*
Product Group	*APMS*
Product Division	*Discrete & Filter*
Packages	*SMB*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST TOURS – FRANCE*
Assembly Plant	*SUBCONTRACTOR – CHINA*
Reliability Lab	*ST TOURS – FRANCE*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	13/03/2024	13	Aurore KHEDIM		Initial release: SMLVT3V3 qualification with HD leadframe

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

Alt	Alternative test
GD	Generic Data
H3TRB	High Humidity High Temperature Reverse Bias
HTRB	High Temperature Reverse Bias
IPP	Peak Pulse current
PC	Preconditioning
PD	Physical Dimensions
PV	Parametric Verification
RS	Repetitive Surges
RSH	Resistance to Soldering Heat
SS	Sample Size
TC	Temperature Cycling
UHAST	Unbiased Highly Accelerated Stress Test

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify SMLVT3V3 product, Transil diode designed to protect sensitive 3.3 V equipment against transient overvoltages embedded in SMB package. This qualification report is dedicated to the change from 6R to HD leadframe.

The changed product does not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet.

The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged.

The footprint recommended by ST remains the same.

There is neither change in the packing mode nor the standard

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.
- RSH to check compatibility of package with customer assembly.
- Functional test such as Repetitive IPP to verify robustness of device submitted to rated Ipp (as per data sheet).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The SMLVT3V3 is a transil diode designed specifically to protect sensitive equipment against transient overvoltages.
Transil diodes provide high overvoltage protection by clamping action.Their instantaneous response to transient overvoltages make them particularly suited to protect voltage sensitive devices such as MOS technology and low voltage supplied IC's.

life.augmented

SMLVT3V3

Low voltage Transil™

Datasheet - production data

SMB

Description

This is a Transil diode designed specifically to protect sensitive 3.3 V equipment against transient overvoltages.

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous response to transient overvoltages make them particularly suited to protect voltage sensitive devices such as MOS technology and low voltage supplied ICs.

TM: Transil is a trademark of STMicroelectronics

Features

- Peak pulse power 600 W (10/1000 µs)
- Stand-off voltage 3.3 V
- Unidirectional type
- Low clamping factor
- Fast response time
- JEDEC registered package outline

4.2 Construction Note

	SMLVT3V3
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	Transil
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS – FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR - CHINA
Package description	SMB
Molding compound	ECOPACK®2 molding compound
Lead finishing material	Lead free (pure Tin)
Final testing information	
Testing location	SUBCONTRACTOR - CHINA

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	SMLVT3V3	SMB	1st Qualification lot

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.			X
MSL research	MSL	J-STD-020			Not applicable for PTH and WLCSP without coating	
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L1	30		X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L1	77		X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A			Required for Thyristor only. Alternative to HTRB	
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for PowerMOSFET - IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104	L1	77		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET - IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET - IGBT only. Alternative to TCHT	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101	L1	77		X
Autoclave	AC	JESD22A-102			Alternative to UHAST	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB (same failure mechanisms activation).	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1	77	Alternative to HAST	X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	X
Power and Temperature Cycle	PTC	JED22A-105	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if $\Delta Tj>100°C$ cannot be achieved with IOL Alternative to IOL	X
ESD Characterization	ESD HBM	AEC Q101-001 and 005	Lx or GDx	xx		X
ESD Characterization	ESD CDM	AEC Q101-001 and 005	Lx or GDx	xx		X
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4				
Physical Dimension	PD	JESD22B-100	See annex 6.2			X
Terminal Strength	TS	MIL-STD-750 Method 2036			Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	L1	30		X
Solderability	SD	J-STD-002 JESD22B102				
Dead Bug Test	DBT	ST Internal specification			Mandatory for SMD package Data collection for PTH package	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate			Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037			Covered during workability trials	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Bond Shear	BS	AEC-Q101-003			Covered during workability trials	
Die Shear	DS	MIL-STD-750 Method 2017			Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET - IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201				
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,...)	FT	Internal specification				
Repetitive Surge	RS	Internal specification	L1	20		X

Low Temperature Storage	LTS	JESD-22 A119: 209			AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104			AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037			AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037			AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27			AQG324 test for Modules	
Vibration	V	IEC60068-2-6			AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS
						L1
Pre- and Post-Electrical Test		ST datasheet	Ir, Vf,parameters following product datasheet	-		0/388
External Visual		JESD22 B-101	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process			
Parametric Verification		ST datasheet	Over part temperature range (note 1)		30	Refer to paragraph 6.1 in Annexes
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=175°C VR=3.3V	1Khrs	77 (1*77)	0/77
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	100cy	77 (1*77)	0/77
UHAST	Y	JESD22 A-118	130°C; 85% RH 2.3bar	96hrs	77 (1*77)	0/77
H3TRB	Y	JESD22 A-101	85°C; 85% RH VR=3.3V	1Khrs	77 (1*77)	0/77
PD		JESD22 B-100	Refer to paragraph 6.2 in Annexes			
RSH	N	JESD22 A-111	THS 85%RH / 85°C 168hrs Dipping 260°C-10s	-	30	0/30
Functional Tests						
RS	Y	0060282 (ST internal)	IPP=50A Pulse delay=0.01ms Time between surges = 60s	10000 surges	20	0/20

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

6 ANNEXES

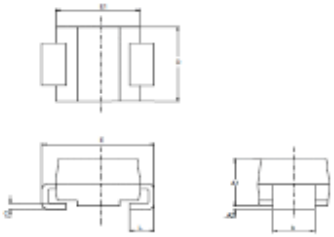
6.1 Parametric Verification

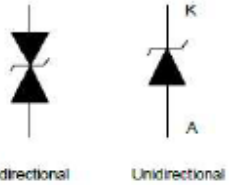
Ref: 22783A

Lab: ST Tours Characterization Lab

TEST	VBR	VBR	VBR	IR	IR	IR
EQUIPMENT	TSA_491	TSA_491	TSA_491	TSA_491	TSA_491	TSA_491
Condition 1	-40°C	25°C	175°C	-40°C	25°C	175°C
Condition 2	IR=1mA	IR=1mA	IR=1mA	VR=3.3V	VR=3.3V	VR=3.3V
Min. Datasheet		4.1V				
Typ. Datasheet						
Max. Datasheet					200uA	
Commentaires						
N	30	30	30	30	30	30
Min	4.61	4.481	4.16	15.2	23.16	56.17
Max	4.711	4.606	4.306	21.88	33.78	83.25
Moy.	4.666	4.550	4.240	18.047	27.612	67.412

6.2 Physical Dimensions





Ref.	Dimensions			
	Millimeters		Inches[1]	
	Min.	Max.	Min.	Max.
A1	1.90	2.45	0.0748	0.0965
A2	0.05	0.20	0.0020	0.0079
b	1.95	2.20	0.0768	0.0867
c	0.15	0.40	0.0059	0.0157
D	3.30	3.95	0.1299	0.1556
E	5.10	5.60	0.2008	0.2205
E1	4.05	4.60	0.1594	0.1811
L	0.75	1.50	0.0295	0.0591

Cote	A1	A2	b	c	D	E	E1	L
1	2.18	0.16	2.04	0.28	3.52	5.34	4.55	1.09
2	2.14	0.17	2.03	0.29	3.51	5.38	4.51	1.11
3	2.18	0.17	2.03	0.28	3.51	5.35	4.55	1.08
4	2.17	0.16	2.01	0.29	3.52	5.38	4.53	1.10
5	2.11	0.16	2.03	0.29	3.51	5.35	4.51	1.12
6	2.14	0.14	2.02	0.29	3.53	5.34	4.55	1.10
7	2.16	0.15	2.02	0.28	3.47	5.33	4.51	1.09
8	2.17	0.16	2.02	0.28	3.50	5.35	4.53	1.06
9	2.17	0.16	2.02	0.27	3.51	5.36	4.51	1.09
10	2.17	0.15	2.01	0.28	3.49	5.34	4.51	1.11
11	2.17	0.16	2.03	0.28	3.50	5.36	4.52	1.07
12	2.17	0.16	2.03	0.28	3.51	5.37	4.54	1.07
13	2.16	0.15	2.04	0.28	3.52	5.36	4.51	1.08
14	2.18	0.16	2.02	0.29	3.51	5.39	4.54	1.07
15	2.17	0.14	2.02	0.28	3.50	5.38	4.53	1.09
16	2.17	0.16	2.02	0.29	3.53	5.36	4.52	1.10
17	2.17	0.16	2.05	0.27	3.52	5.38	4.51	1.10
18	2.18	0.15	2.03	0.28	3.53	5.37	4.50	1.11
19	2.15	0.15	2.02	0.27	3.50	5.37	4.52	1.11
20	2.17	0.16	2.02	0.28	3.53	5.37	4.53	1.11
21	2.16	0.16	2.01	0.28	3.56	5.34	4.50	1.10
22	2.17	0.16	2.03	0.28	3.56	5.41	4.52	1.07
23	2.16	0.15	2.02	0.28	3.55	5.37	4.50	1.11
24	2.18	0.16	2.03	0.29	3.52	5.33	4.53	1.11
25	2.17	0.14	2.03	0.29	3.55	5.35	4.52	1.11
26	2.17	0.15	2.02	0.28	3.50	5.37	4.52	1.09
27	2.18	0.15	2.02	0.29	3.55	5.36	4.51	1.08
28	2.17	0.16	2.02	0.28	3.56	5.34	4.51	1.09
29	2.17	0.16	2.02	0.28	3.56	5.38	4.49	1.08
30	2.17	0.15	2.04	0.28	3.54	5.33	4.50	1.10
LSL	1.90	0.05	1.95	0.15	3.30	5.10	4.05	0.75
USL	2.45	0.20	2.20	0.40	3.95	5.60	4.60	1.50
MIN	2.11	0.14	2.01	0.27	3.47	5.33	4.49	1.06
MAX	2.18	0.17	2.05	0.29	3.56	5.41	4.55	1.12
AVG	2.17	0.16	2.02	0.28	3.52	5.36	4.52	1.09

6.3 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations. Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
RSH Resistance to Solder Heat	Package is dipped by the leads in a solder bath after initial wet ageing (for SMDs only). Assessment by electrical test + no external crack	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
Functional Tests		
RS Repetitive Surges	The device is submitted to a reverse current peak: Ipp, which depends of the current holding of the product.	To evaluate the holding of the component to a high electrical field. Short circuit or hot point is expected as failure mechanism.

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Additional capacity for SMLVT3V3 at same subcontractor in China

PCN Reference : ADG/24/14639

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

SMLVT3V3		

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PCN
Product/Process Change Notification

Additional capacity for SMLVT3V3 at same subcontractor in China

Notification number:	ADG/24/14639	**Issue Date**	18-Mar-2024
Issued by	Isabelle BALLON		
Product series affected by the change		SMLVT3V3	
Type of change		Backend Realization	

Description of the change

STMicroelectronics is qualifying SMLVT3V3 production on existing assembly line with additional capacity at same subcontractor in China.
This line is already qualified and used for mass production on other TVS parts since year 2017.

In addition to back-end capacity expansion, STMicroelectronics is also taking the opportunity to rationalize wafer manufacturing process with additional passivation layer.

Reason for change

With this qualification, STMicroelectronics will increase its production capacity to better serve its customers through service improvement and lead time reduction.

These changes are in the frame, for standardization of assembly process and method for all TVS parts in SMB package, and global production homogenization of die manufacturing process (passivation layer addition) developed on new products released.

Former versus changed product:	The changed product does not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet. The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is neither change in the packing mode nor the standard delivery quantities. The product remains in full compliance with the ST ECOPACK®2 grade (so called “halogen-free”).

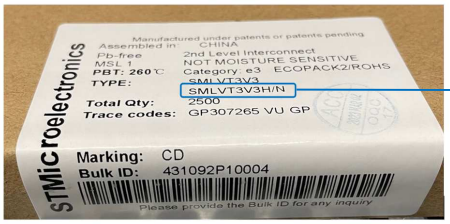
Disposition of former product

STMicroelectronics will continue to deliver the former product until stock depletion.

Marking and traceability

Traceability of the change will be ensured by new Finished Good/Type print on carton labels.

Commercial part number/Order code	Former Finished Good/Type	New Finished Good/Type
SMLVT3V3	SMLVT3V3H/N	SMLVT3V3H/NH

Former Label	New Label
	SMLVT3V3H/NH

Qualification completion date	18-Mar-2024

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
PROTECTION	SMB	SMLVT3V3	Week 12-2024

For sample(s) request, please inform FSE (Field Sales Engineer) in order to insert corresponding **Non-Standard Samples Order** (a single Commercial Product for each request) with **PCN reference** as additional information.

Change implementation schedule

Sales-type	Estimated production start	Estimated first shipments
SMLVT3V3	**Week 14-2024**	**Week 25-2024**

Comments:	With early PCN acceptance, possible shipments starting Week 18-2024.

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change.
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change.

Qualification program and results	24010QRP Attached

Qualification Report

SMLVT3V3

General Information	
Product Line	*Protection*
Product Description	*Transil diode designed to protect sensitive 3.3 V equipment against transient overvoltages*
Product Perimeter	*SMLVT3V3*
Product Group	*APMS*
Product Division	*Discrete & Filter*
Packages	*SMB*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST TOURS – FRANCE*
Assembly Plant	*SUBCONTRACTOR – CHINA*
Reliability Lab	*ST TOURS – FRANCE*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	13/03/2024	13	Aurore KHEDIM	Timothée PINGAULT Digitally signed by Timothée PINGAULT Date: 2024.03.13 17:57:02 +01'00'	Initial release: SMLVT3V3 qualification with HD leadframe

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

Alt	Alternative test
GD	Generic Data
H3TRB	High Humidity High Temperature Reverse Bias
HTRB	High Temperature Reverse Bias
IPP	Peak Pulse current
PC	Preconditioning
PD	Physical Dimensions
PV	Parametric Verification
RS	Repetitive Surges
RSH	Resistance to Soldering Heat
SS	Sample Size
TC	Temperature Cycling
UHAST	Unbiased Highly Accelerated Stress Test

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify SMLVT3V3 product, Transil diode designed to protect sensitive 3.3 V equipment against transient overvoltages embedded in SMB package. This qualification report is dedicated to the change from 6R to HD leadframe.

The changed product does not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet.

The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged.

The footprint recommended by ST remains the same.

There is neither change in the packing mode nor the standard

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.
- RSH to check compatibility of package with customer assembly.
- Functional test such as Repetitive IPP to verify robustness of device submitted to rated Ipp (as per data sheet).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

The SMLVT3V3 is a transil diode designed specifically to protect sensitive equipment against transient overvoltages.
Transil diodes provide high overvoltage protection by clamping action.Their instantaneous response to transient overvoltages make them particularly suited to protect voltage sensitive devices such as MOS technology and low voltage supplied IC's.

life.augmented

SMLVT3V3

Low voltage Transil™

Datasheet - production data

SMB

Description

This is a Transil diode designed specifically to protect sensitive 3.3 V equipment against transient overvoltages.

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous response to transient overvoltages make them particularly suited to protect voltage sensitive devices such as MOS technology and low voltage supplied ICs.

TM: Transil is a trademark of STMicroelectronics

Features

- Peak pulse power 600 W (10/1000 µs)
- Stand-off voltage 3.3 V
- Unidirectional type
- Low clamping factor
- Fast response time
- JEDEC registered package outline

4.2 Construction Note

	SMLVT3V3
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	Transil
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS – FRANCE
Assembly information	
Assembly site	SUBCONTRACTOR - CHINA
Package description	SMB
Molding compound	ECOPACK®2 molding compound
Lead finishing material	Lead free (pure Tin)
Final testing information	
Testing location	SUBCONTRACTOR - CHINA

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	SMLVT3V3	SMB	1st Qualification lot

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.			X
MSL research	MSL	J-STD-020			Not applicable for PTH and WLCSP without coating	
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L1	30		X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L1	77		X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A			Required for Thyristor only. Alternative to HTRB	
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for PowerMOSFET - IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104	L1	77		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET - IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET - IGBT only. Alternative to TCHT	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101	L1	77		X
Autoclave	AC	JESD22A-102			Alternative to UHAST	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB (same failure mechanisms activation).	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1	77	Alternative to HAST	X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	X
Power and Temperature Cycle	PTC	JED22A-105	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if $\Delta Tj>100°C$ cannot be achieved with IOL Alternative to IOL	X
ESD Characterization	ESD HBM	AEC Q101-001 and 005	Lx or GDx	xx		X
ESD Characterization	ESD CDM	AEC Q101-001 and 005	Lx or GDx	xx		X
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4				
Physical Dimension	PD	JESD22B-100	See annex 6.2			X
Terminal Strength	TS	MIL-STD-750 Method 2036			Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	L1	30		X
Solderability	SD	J-STD-002 JESD22B102				
Dead Bug Test	DBT	ST Internal specification			Mandatory for SMD package Data collection for PTH package	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate			Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037			Covered during workability trials	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Bond Shear	BS	AEC-Q101-003			Covered during workability trials	
Die Shear	DS	MIL-STD-750 Method 2017			Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET - IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201				
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,...)	FT	Internal specification				
Repetitive Surge	RS	Internal specification	L1	20		X

Low Temperature Storage	LTS	JESD-22 A119: 209			AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104			AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037			AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037			AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27			AQG324 test for Modules	
Vibration	V	IEC60068-2-6			AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS
						L1
Pre- and Post-Electrical Test		ST datasheet	Ir, Vf,parameters following product datasheet	-		0/388
External Visual		JESD22 B-101	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process			
Parametric Verification		ST datasheet	Over part temperature range (note 1)		30	Refer to paragraph 6.1 in Annexes
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=175°C VR=3.3V	1Khrs	77 (1*77)	0/77
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	100cy	77 (1*77)	0/77
UHAST	Y	JESD22 A-118	130°C; 85% RH 2.3bar	96hrs	77 (1*77)	0/77
H3TRB	Y	JESD22 A-101	85°C; 85% RH VR=3.3V	1Khrs	77 (1*77)	0/77
PD		JESD22 B-100	Refer to paragraph 6.2 in Annexes			
RSH	N	JESD22 A-111	THS 85%RH / 85°C 168hrs Dipping 260°C-10s	-	30	0/30
Functional Tests						
RS	Y	0060282 (ST internal)	IPP=50A Pulse delay=0.01ms Time between surges = 60s	10000 surges	20	0/20

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

6 ANNEXES

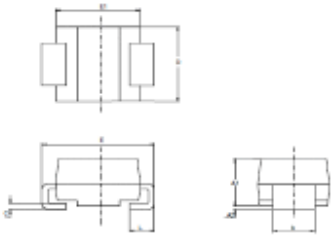
6.1 Parametric Verification

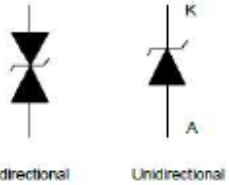
Ref: 22783A

Lab: ST Tours Characterization Lab

TEST	VBR	VBR	VBR	IR	IR	IR
EQUIPMENT	TSA_491	TSA_491	TSA_491	TSA_491	TSA_491	TSA_491
Condition 1	-40°C	25°C	175°C	-40°C	25°C	175°C
Condition 2	IR=1mA	IR=1mA	IR=1mA	VR=3.3V	VR=3.3V	VR=3.3V
Min. Datasheet		4.1V				
Typ. Datasheet						
Max. Datasheet					200uA	
Commentaires						
N	30	30	30	30	30	30
Min	4.61	4.481	4.16	15.2	23.16	56.17
Max	4.711	4.606	4.306	21.88	33.78	83.25
Moy.	4.666	4.550	4.240	18.047	27.612	67.412

6.2 Physical Dimensions





Ref.	Dimensions			
	Millimeters		Inches[1]	
	Min.	Max.	Min.	Max.
A1	1.90	2.45	0.0748	0.0965
A2	0.05	0.20	0.0020	0.0079
b	1.95	2.20	0.0768	0.0867
c	0.15	0.40	0.0059	0.0157
D	3.30	3.95	0.1299	0.1556
E	5.10	5.60	0.2008	0.2205
E1	4.05	4.60	0.1594	0.1811
L	0.75	1.50	0.0295	0.0591

Cote	A1	A2	b	c	D	E	E1	L
1	2.18	0.16	2.04	0.28	3.52	5.34	4.55	1.09
2	2.14	0.17	2.03	0.29	3.51	5.38	4.51	1.11
3	2.18	0.17	2.03	0.28	3.51	5.35	4.55	1.08
4	2.17	0.16	2.01	0.29	3.52	5.38	4.53	1.10
5	2.11	0.16	2.03	0.29	3.51	5.35	4.51	1.12
6	2.14	0.14	2.02	0.29	3.53	5.34	4.55	1.10
7	2.16	0.15	2.02	0.28	3.47	5.33	4.51	1.09
8	2.17	0.16	2.02	0.28	3.50	5.35	4.53	1.06
9	2.17	0.16	2.02	0.27	3.51	5.36	4.51	1.09
10	2.17	0.15	2.01	0.28	3.49	5.34	4.51	1.11
11	2.17	0.16	2.03	0.28	3.50	5.36	4.52	1.07
12	2.17	0.16	2.03	0.28	3.51	5.37	4.54	1.07
13	2.16	0.15	2.04	0.28	3.52	5.36	4.51	1.08
14	2.18	0.16	2.02	0.29	3.51	5.39	4.54	1.07
15	2.17	0.14	2.02	0.28	3.50	5.38	4.53	1.09
16	2.17	0.16	2.02	0.29	3.53	5.36	4.52	1.10
17	2.17	0.16	2.05	0.27	3.52	5.38	4.51	1.10
18	2.18	0.15	2.03	0.28	3.53	5.37	4.50	1.11
19	2.15	0.15	2.02	0.27	3.50	5.37	4.52	1.11
20	2.17	0.16	2.02	0.28	3.53	5.37	4.53	1.11
21	2.16	0.16	2.01	0.28	3.56	5.34	4.50	1.10
22	2.17	0.16	2.03	0.28	3.56	5.41	4.52	1.07
23	2.16	0.15	2.02	0.28	3.55	5.37	4.50	1.11
24	2.18	0.16	2.03	0.29	3.52	5.33	4.53	1.11
25	2.17	0.14	2.03	0.29	3.55	5.35	4.52	1.11
26	2.17	0.15	2.02	0.28	3.50	5.37	4.52	1.09
27	2.18	0.15	2.02	0.29	3.55	5.36	4.51	1.08
28	2.17	0.16	2.02	0.28	3.56	5.34	4.51	1.09
29	2.17	0.16	2.02	0.28	3.56	5.38	4.49	1.08
30	2.17	0.15	2.04	0.28	3.54	5.33	4.50	1.10
LSL	1.90	0.05	1.95	0.15	3.30	5.10	4.05	0.75
USL	2.45	0.20	2.20	0.40	3.95	5.60	4.60	1.50
MIN	2.11	0.14	2.01	0.27	3.47	5.33	4.49	1.06
MAX	2.18	0.17	2.05	0.29	3.56	5.41	4.55	1.12
AVG	2.17	0.16	2.02	0.28	3.52	5.36	4.52	1.09

6.3 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations. Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
RSH Resistance to Solder Heat	Package is dipped by the leads in a solder bath after initial wet ageing (for SMDs only). Assessment by electrical test + no external crack	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
Functional Tests		
RS Repetitive Surges	The device is submitted to a reverse current peak: Ipp, which depends of the current holding of the product.	To evaluate the holding of the component to a high electrical field. Short circuit or hot point is expected as failure mechanism.