

PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data

1.1 Company	 STMicroelectronics International N.V
1.2 PCN No.	ADG/24/14612
1.3 Title of PCN	STD105N10F7AG (OD0FA1) Activation of ST Singapore SG8 Plant as Front End Additional Source Location
1.4 Product Category	STD105N10F7AG
1.5 Issue date	2024-03-14

2. PCN Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Mario ASTUTI
2.1.2 Marketing Manager	Anna RANIOLO, Martina GIUFFRIDA
2.1.3 Quality Manager	Daniela FAZIO

3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication	ST SG8 Singapore - receiving plant

4. Description of change

	Old	New
4.1 Description	ST CT8 Catania	ST CT8 Catania and SG8 Singapore
4.2 Anticipated Impact on form, fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change

5.1 Motivation	Capacity Increase
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change

6.1 Description	Dedicated Finished Good Code
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7. Timing / schedule

7.1 Date of qualification results	2024-02-29
7.2 Intended start of delivery	2024-06-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation

8.1 Description	14612 Qualification.zip		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2024-03-14

9. Attachments (additional documentations)

14612 Public product.pdf
14612 Details.pdf
14612 Qualification.zip

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STD105N10F7AG	

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Product/process change notification:

STD105N10F7AG (OD0FA1): Activation of Singapore

SG8 Plant as Front End Additional Location

ADG/24/14612

Product family	Technology	Package
STD105N10F7AG	PMOS	DPAK

(optional)

Description of the change

Activation of SG8 Singapore as additional Front End location beside current CT8 Catania

Reason

Capacity Increase

Date of implementation

From June 2024

Impact of the change

Form	No Impact
Fit	No Impact
Function	No Impact
Reliability	No Impact
Processibility	No Impact

Qualification of the change

According to ZVEI and AECQ101 guidelines

See below details



STD105N10F7AG (OD0FA1) Activation of ST Singapore SG8 Plant as Front End Additional Source Location

CONTENTS

- ST SINGAPORE SG8 PRESENTATION
- STD105N10F7AG CHANGE DESCRIPTION
- STD105N10F7AG PCN QUALIFICATION PLAN



ST SINGAPORE SG8 FAB PRESENTATION

ST SINGAPORE WAFER FAB 8



ST's wafer-fabrication in Singapore have grown into the Company's single largest wafer-fabrication site by volume. The fab now manufactures both six-inch and eight-inch wafers, with an ongoing conversion to eight-inch wafer production.

LV POWER MOSFET has a strong footprint within SG8 Fab with several technologies qualified and running. Specifically, OFT100 Automotive grade family that STD105N10F7AG belong to is already in production with 67 kWafer/yr produced.

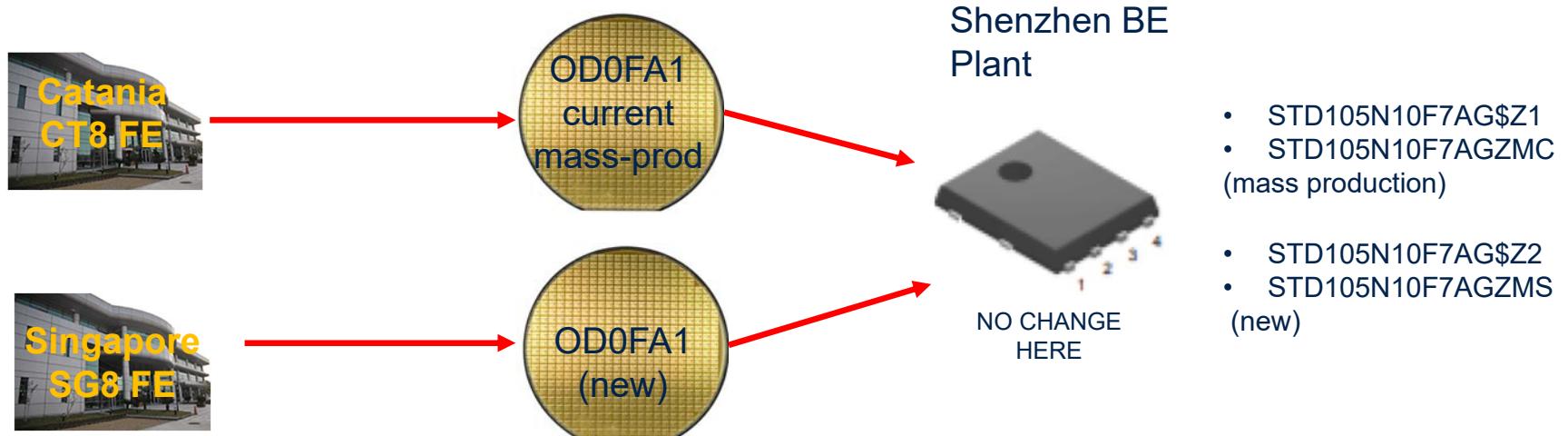


STD105N10F7AG CHANGE DESCRIPTION

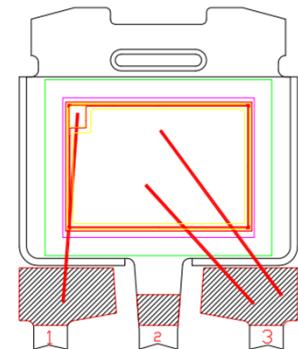
Following the continuous improvement of our service and in order to increase the productivity, we are announcing that the STripFET™ F7 product STD105N10F7AG, currently manufactured and tested in ST Catania (IT) CT8 Diffusion Fab and assembled in ST Shenzhen (CN), will be **also manufactured and tested in ST Singapore SG8**.

The new FE source has been activated following internal Company SOP rules and based on the Copy&Past principal of Technology Process Transfer Methodology and the qualification of the Change was performed based on AEC-Q101 methodology.

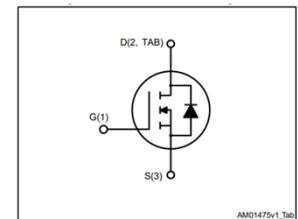
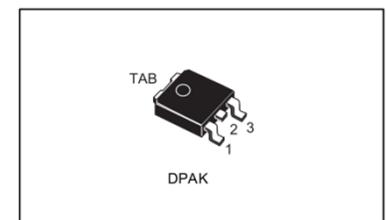
The objective is to get the same process and electrical models centering and same or better process performance (quality, reliability, stability, robustness margin, cost...) to guaranty that the transfer of further products will be qualified on time and without negative impact to our customer.



Commercial Product	Silicon Line	PACKAGE	Techno	Change Description
STD105N10F7AG	OD0FA1	DPAK	OFT1 100V	<ul style="list-style-type: none"> • Silicon Transfer from Catania 8inch to AMK 8inch FAB • Wafer Probing transfer from Catania to AMK



Item	Changed	Current	Proposal
Wafer Production Site	YES	Catania (Italy) - ST 8 inches FAB	AMK – SG8 FAB
Materials	NO		
Production Method	NO		
Layout	NO		
Mask (active area)	NO		
Passivation layer	NO		
Passivation mask	NO		
Wafer Probe Test	YES	ST Catania (Italy) EWS	ST AMK (Singapore) EWS
Package Assembly Site	NO		
Wafer Mount & Sawing	NO	Same Assembly Plant → ST Shenzhen	
Die Attach	NO		
Wire Bonding	NO		
Molding	NO		
Cropping	NO		
Final Testing	NO	Same Testing Plant → ST Shenzhen	





STL105N4LF7HT CHANGE QUALIFICATION PLAN

QUALIFICATION PLAN

Qualification plan report is provided within PCN package

Date:	7-Feb-24			Device evaluation														
PCN number:	PCN/ADG/24/xxxx			MATERIAL PERFORMANCE TEST RESULTS (on the basis of AEC-Q101 Revision D) includes e.g. small signal diodes (bipolar- and Schottky diodes), small signal transistors, MOSFETs, IGBTs, power diodes, ...														
Signature:				AEC-Q101 Revision D														
For integrated circuits or discrete semiconductors select below:	AEC-Q101 Revision D			Evaluation level A / B / C														
				Show Text														
				Values: Show Rows														
				Values: Show Columns														
				Assessment of impact on Supply Chain regarding following aspects														
				- contractual agreements - technical interface of processability/manufacturability of customer - form, fit, function, quality performance, reliability														
				Remaining risks within Supply Chain?														
				A: Application level B: Component level C: Connected Board - Not relevant for qualification matrix														
				Use evaluation table to evaluate by value or condition (checkmarks)														
				ID														
				Type of change														
				Remainin g risks within Supply Chain?														
				A: Application level B: Component level C: Connected Board - Not relevant for qualification matrix														
				Mark change with an 'X'														
				AEC-Q101 Revision D														
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Silicon Line	Die size	Commercial Product	Package	Sample Size	Target	Qualification Plan
OD0FA1	10.47mm ²	STD105N10F7AG	DPAK	1 Lot + Family Data	Full Product Qualification	<ul style="list-style-type: none"> • Full According AEC Q101 (test plan below) • Static and Dynamic parameters - Comparative analysis with Catania

AEC-Q101 Test Plan Table

TEST GROUP	#	Data Type	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
A ACCELERATED ENVIRONMENT STRESS TESTS	A1	1	PC	Preconditioning	Yes
	A2	1	HAST	Highly Accelerated Stress Test	No
	A2 alt	1	H3TRB	High Humidity High Temp. Reverse Bias	Yes
	A3	1	UHAST	Unbiased Highly Accelerated Stress Test	No
	A3 alt	1	AC	Autoclave	Yes
	A4	1	TC	Temperature Cycling	Yes
	A4a	1	TCHT	Temperature Cycling Hot Test	Yes
	A4a alt	1	TCDT	Temperature Cycling Delamination Test	Yes
	A5	1	IOL	Intermittent Operational Life	Yes
	A5alt	1	PTC	Power Temperature Cycling	No
B ACCELERATED LIFETIME SIMULATION TESTS	B1	1	HTRB	High Temperature Reverse Bias	Yes
	B1 a	1	ACBV	AC blocking voltage	Not Applicable
	B1 b	1	SSOP	Steady State Operational	Not Applicable
	B2	1	HTGB	High Temperature Gate Bias	Yes
C PACKAGE ASSEMBLY INTEGRITY TESTS	C1	1	DPA	Destructive Physical Analysis	Yes
	C2	2	PD	Physical Dimension	Not Applicable
	C3	3	WBP	Wire Bond Pull Strength	No
	C4	3	WBS	Wire Bond Shear Strength	Yes
	C5	3	DS	Die Shear	Yes
	C6	2	TS	Terminal Strength	Not Applicable
	C7	2	RTS	Resistance to Solvents	Not Applicable
	C8	2	RSH	Resistance to Solder Heat	Not Applicable
	C9	3	TR	Thermal Resistance	Yes
	C10	2	SD	Solderability	Not Applicable
	C11	3	WG	Whisker Growth Evaluation	Not Applicable
	C12	2	CA	Constant Acceleration	Not Applicable
	C13	2	VVF	Vibration Variable Frequency	Not Applicable
	C14	2	MS	Mechanical Shock	Not Applicable
D DIE FABRICATION RELIABILITY TESTS	C15	2	HER	Hermeticity	Not Applicable
	D1	3	DI	Dielectric Integrity	Yes
E ELECTRICAL VERIFICATION TESTS	E0	1	EV	Eternal Visual	Yes
	E1	1	TEST	Pre- and Post-Stress Electrical Test	Yes
	E2	1	PV	Parametric Verification	Yes
	E3	1	ESDH	ESD HBM Characterization	Yes
	E4	2	ESDC	ESD CDM Characterization	Yes
	E5	3	UIS	Unclamped Inductive Switching	Yes
	E6	3	SC	Short Circuit Characterization	Not Applicable

Reliability Strategy and Test Plan

Ang Mo Kio (Singapore) 8" wafer fab has been already qualified by mean of selected test vehicles for product manufacturing designed in StripFET F7 OFT1 100V Technology in 2020 (ST reference report # RRADGQRCTLGS202006).

The qualification purpose was addressed to verify the failure mode related to the Front-End (Silicon Technology) vs Back-End (Package Topology) interactions, ESD and Electrical Characterization **for one assembly lot** applying the path described in the Test Plan in agreement with ST 0061692 and AEC-Q101 Rev E specification.

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Public Products List

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PCN Title : STD105N10F7AG (OD0FA1) Activation of ST Singapore SG8 Plant as Front End Additional Source Location

PCN Reference : ADG/24/14612

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STD105N10F7AG		
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