PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/24/14538
1.3 Title of PCN	STD120N4F6 (6D4FA1): Double Sourcing Option Activation
1.4 Product Category	STD120N4F6
1.5 Issue date	2024-01-29

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Mario ASTUTI
2.1.2 Marketing Manager	Martina GIUFFRIDA,Anna RANIOLO
2.1.3 Quality Manager	Diego Maria FERRARI

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication	ST CT8 Catania - Italy TFME - China

4. Description of change		
	Old	New
4.1 Description	HHGrace Fab3 - China / TFME - China HHGrace Fab3 - China / ST Shenzhen - China ST CT8 - Italy / ST Shenzhen - China	HHGrace Fab3 - China / TFME - China HHGrace Fab3 - China / ST Shenzhen - China ST CT8 - Italy / ST Shenzhen - China New option ST CT8 Italy / TFME - China
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change	
5.1 Motivation	Dual Source and Capacity Increase
5.2 Customer Benefit	DOUBLE SOURCING

6. Marking of parts / traceability of change	
6.1 Description	Dedicated Finished Good Code

7. Timing / schedule	
7.1 Date of qualification results	2024-01-23
7.2 Intended start of delivery	2024-05-01
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	14538 Qualification_RRLGS210008.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2024-01-29

9. Attachments (additional documentations)
14538 Public product.pdf 14538 Details.pdf 14538 Qualification_RRLGS210008.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STD120N4F6	

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Product/process change notification:

STD120N4F6 (6D4FA1): Double Sourcing Option Activation

ADG/24/14538

Product family	Technology	Package
STD120N4F6	MOSFET	DPAK

(optional)

Description of the change

Activation of additional double sourcing option:
ST CT8 Catania – Italy (diffusion) with subcon. TFME - China (Assembly and Final Testing)

Reason

Dual Source and Capacity Increase

Date of implementation

May 2024

Impact of the change

Form	No Impact
Fit	No Impact
Function	No Impact
Reliability	No Impact
Processibility	No Impact

Qualification of the change

Qualification included in this notification according to ZVEI and AECQ guidelines.

STD120N4F6 assembled in TFME in DPAK package: Activation of Catania as additional diffusion plant.

Agenda

3 Change Description

4 ZVEI Guidelines

5 Test Vehicles and Product lines impacted

6 Conclusions

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Change description

- The product STD120N4F6 is currently manufactured as below:
  - Silicon Line 6D4FA1 produced at HHG 8” diffusion plant.
  - Assembled in package DPAK in Nantong Fujitsu (TFME) .
- A second diffusion plant (Catania 8”) has been activated for package DPAK at Nantong Fujitsu (TFME)
- Dedicated finish good to differentiate diffusion plant:
  - STD120N4F6-FG for HHG 8”
  - STD120N4F6-FC for Catania 8”
- No change of Bill Of Material used for assembly
- All reliability tests have been completed with positive results.

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ZVEI Guidelines

- According to ZVEI recommendations, the notification is required.

		Assessment of impact on Supply Chain regarding following aspects - contractual agreements - technical interface of processability/manufacturability of customer - form, fit, function, quality performance, reliability	Remaining risks within Supply Chain?		Understanding of semiconductors experts	Examples to explain
	ID	Type of change	No	Yes		
		ANY				
		DATA SHEET				
		DESIGN				
		PROCESS - WAFER PRODUCTION				
X	SEM-PW-13	Move all or parts of production to a different wafer fab site.	P	P	Wafer fab transition with additional changes (described above). Includes transfer as well as additional site.	e.g. dual source / fab strategy

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Test Vehicles and Product lines impacted

- Silicon Line 6D4FA1 in DPAK package
  - Commercial Product: STD120N4F6
  - Finish Good: STD120N4F6-FC

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Conclusions

- Detailed qualification activity has been performed in order to qualify the Catania diffusion plant assembled in Nantong Fujitsu (TFME) .
- All reliability tests (AEC-Q101 requirement) have been performed.
- This report shows the positive results achieved, ensuring the same quality and electrical characteristics as the product assembled with HHG diffusion plant.

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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : STD120N4F6 (6D4FA1): Double Sourcing Option Activation

PCN Reference : ADG/24/14538

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STD120N4F6		

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Reliability Evaluation Report
F6 EHD6 and F7 OFT40 Technologies
Package DPAK
Tongfu Microelectronics TFME (China) subcon

General Information	
Commercial Product	**STD80N4F6; STD134N4F7HT, STD120N4F6**
Product Line	**6D44A1, OD4QA1, 6D4FA1**
Silicon process Technology	**F6 EHD6; F7 OFT40**
Package	**DPAK**

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Revision history

Rev.	Changes description	Author	Date
1.0	New release	A. Giuffrida	12th March 2021
2.0	Update Information (typo error) Add HBM/CDM results	A. Giuffrida	2nd March 2022
3.0	To add EHD6 TV for ST CT8 Wafer Fab	A. Giuffrida	18th January 2024

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Catania (Italy)	A. Marmoni	18th January 2024

Table of Contents

1. Reliability Evaluation Overview

1.1. Objective

Aim of this report is to present the results of the reliability evaluations performed on selected test vehicles to release in mass production the PowerMOSFET products intended for Automotive application designed in F6 EHD6 Technology diffused both in HHGrace (China) 8" subcon Wafer Fab and ST CT8 Catania (Italy) 8" Wafer Fab, in F7 OFT40 Technology diffused in ST CT8 Catania (Italy) 8" Wafer Fab, all assembled in package DPAK in Tongfu Microelectronics TFME (China) subcon assembly plant.

Here below the test vehicles list:

Commercial Product	ST Silicon Line	Technology	Diffusion Plant
STD80N4F6	6D44A1	F6 EHD6	HHGrace (China) subcon
STD120N4F6	6D4FA1		ST CT8 Catania (Italy)
STD134N4F7HT	OD4QA1	F7 OFT40	ST CT8 Catania (Italy)

1.2. Reliability Strategy and Test Plan

1.2.1. Reliability strategy

A previous report version released in 2021 addressed the trials performed on F6 EHD6 diffused in HHGrace and on F7 OFT40, the reliability evaluation was in agreement with ST 0061692 and **AEC-Q101 RevD1** specification that was the applicable one at that time.

The present report version now includes the trials performed on 1 lot of F6 EHD6 diffused in ST CT8 Catania (Italy) 8" Wafer Fab, applying a family approach with the activity already did, the reliability evaluation was in agreement with ST 0061692 and **AEC-Q101 RevE** specification that is the one applicable now.

The reliability trials are listed in below Test Plan, for details on test conditions, generic data used and specifications references, refer to test results summary in section 3 (the table was maintained **AEC-Q101 RevD1** complaint).

1.2.2. Test Plan

AEC-Q101 Test Plan Table

#	Data Type	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
1	1	TEST	Pre- and Post- Stress Electrical Test	Yes
2	1	PC	Preconditioning	Yes
3	1	EV	Eternal Visual	Yes
4	1	PV	Parametric Verification	Yes
5	1	HTRB	High Temperature Reverse Bias	Yes
5a	1	ACBV	AC blocking voltage	Not Applicable
5b	1	HTFB	High Temperature Forward Bias	Not Applicable
5c	1	SSOP	Steady State Operational	Not Applicable
6	1	HTGB	High Temperature Gate Bias	Yes
7	1	TC	Temperature Cycling	Yes
7a	1	TCHT	Temperature Cycling Hot Test	Yes
7a alt	1	TCDT	Temperature Cycling Delamination Test	Yes
7b	3	WBI	Wire Bonding Integrity	Yes
8	1	UHAST	Unbiased Highly Accelerated Stress Test	No
8 alt	1	AC	Autoclave	Yes
9	1	HAST	Highly Accelerated Stress Test	No
9 alt	1	H3TRB	High Humidity High Temp. Reverse Bias	Yes
9a	1	HTHHB	High Temperature High Humidity Bias	Not Applicable
10	1	IOL	Intermittent Operational Life	Yes
10alt	1	PTC	Power Temperature Cycling	No
11	1	ESD	ESD Characterization	Yes
12	1	DPA	Destructive Physical Analysis	Yes
13	2	PD	Physical Dimension	Yes
14	2	TS	Terminal Strength	Yes
15	2	RTS	Resistance to Solvents	Not Applicable
16	2	CA	Constant Acceleration	Not Applicable
17	2	VVF	Vibration Variable Frequency	Not Applicable
18	2	MS	Mechanical Shock	Not Applicable
19	2	HER	Hermeticity	Not Applicable
20	2	RSH	Resistance to Soder Heat	Not Applicable
21	2	SD	Solderability	Yes
22	3	TR	Thermal Resistance	Yes
23	3	WBS	Wire Bond Strength	Yes
24	3	BS	Bond Shear	Yes
25	3	DS	Die Shear	Yes
26	3	UIS	Unclamped Inductive Switching	Yes
27	3	DI	Dielectric Integrity	Yes
28	3	SCR	Short Circuit Reliability Characterization	Not Applicable
29	3	LF	Lead Free	Not Applicable

1.3. Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

Based on the overall results obtained, the PowerMOSFET products intended for Automotive application designed in F6 EHD6 Technology diffused both in HHGrace (China) 8" subcon Wafer Fab and ST CT8 Catania (Italy) 8" Wafer Fab, in F7 OFT40 Technology diffused in ST CT8 Catania (Italy) 8" Wafer Fab, all assembled in package DPAK in Tongfu Microelectronics TFME (China) subcon assembly plant, has positively passed reliability evaluation performed in agreement with ST 0061692 and **AEC-Q101 Rev.D1** and **AEC-Q101 Rev.E** specification.

2. Product Characteristics

2.1. Generalities

2.1.1. Test vehicle 1

STD80N4F6, STU80N4F6

N-channel 40 V, 5.5 mΩ typ., 80 A STripFET™ VI DeepGATE™ Power MOSFET in DPAK and IPAK packages

Datasheet – production data

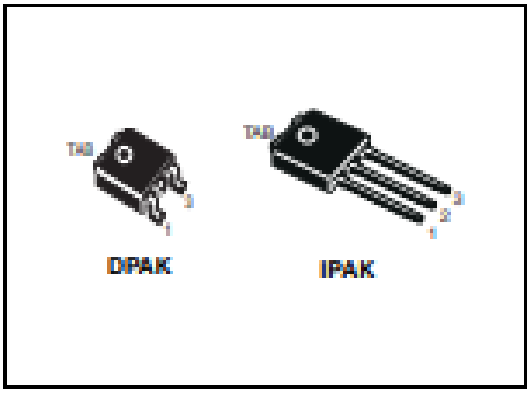
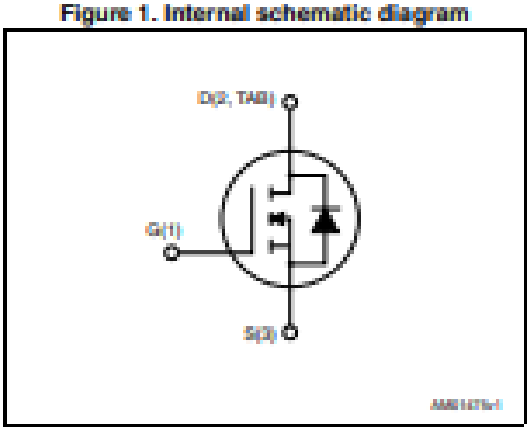


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D
STD80N4F6	40 V	6.0 mΩ	80 A
STU80N4F6		6.3 mΩ	

- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

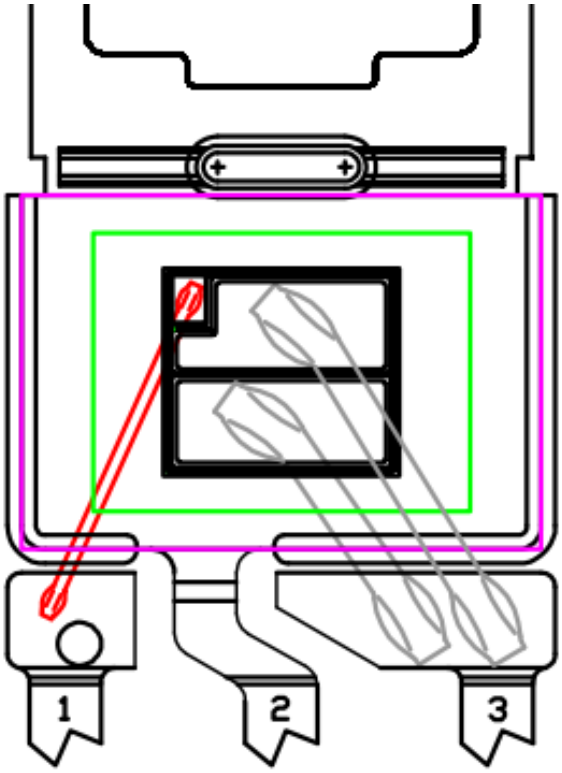
Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFETs exhibits the lowest $R_{DS(on)}$ in all packages.

2.1.2. Pin connection/Bonding Diagram Test vehicle 1



2.1.3. Test vehicle 2

STD134N4F7HT

Automotive-grade N-channel 40 V, 2.5 mΩ typ., 80 A STripFET™ F7 Power MOSFET in a DPAK package

Datasheet - production data

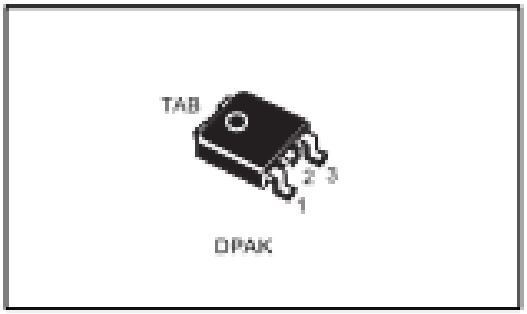
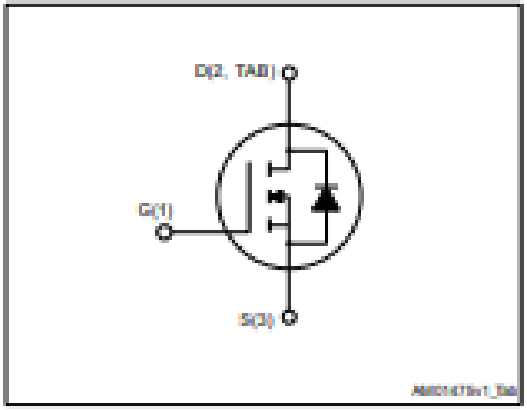


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD134N4F7HT	40 V	3.5 mΩ	80 A	134 W

- AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

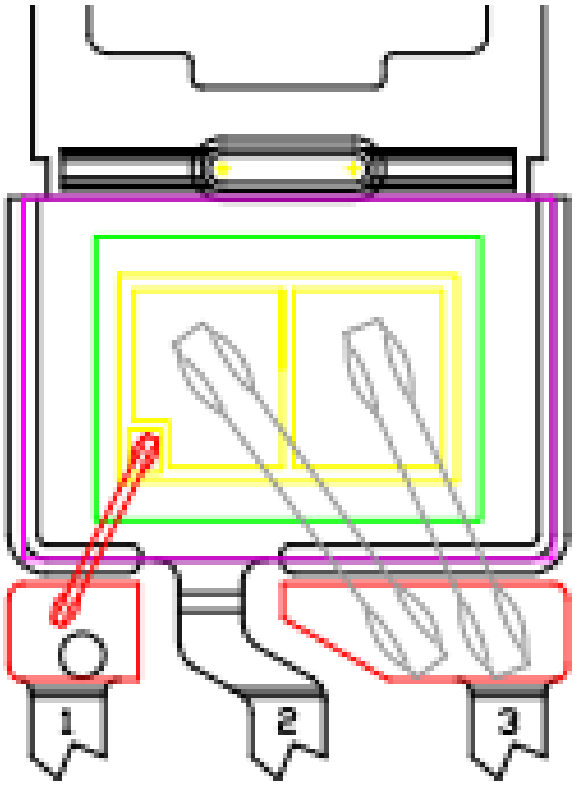
Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STD134N4F7HT	134N4F7	DPAK	Tape and reel

2.1.4. Pin connection/Bonding Diagram Test vehicle 2



2.1.4. Test vehicle 3

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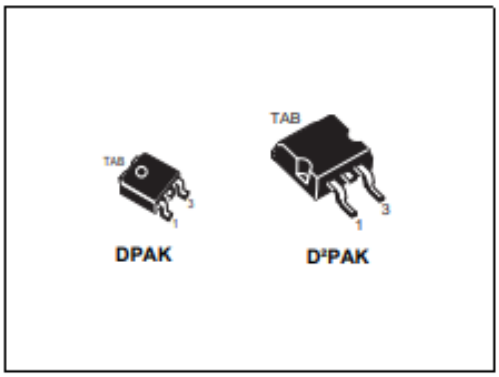
STB120N4F6, STD120N4F6

Automotive-grade N-channel 40 V, 3.5 mΩ typ., 80 A STripFET™ F6 Power MOSFETs in DPAK and D²PAK packages

Datasheet - production data

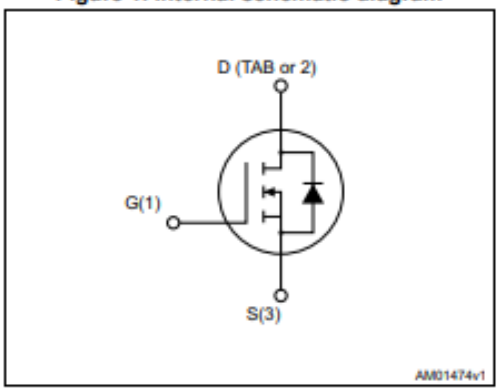


Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D
STB120N4F6	40 V	4 mΩ	80 A
STD120N4F6	40 V	4 mΩ	80 A

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Figure 1. Internal schematic diagram



Application

- Switching applications

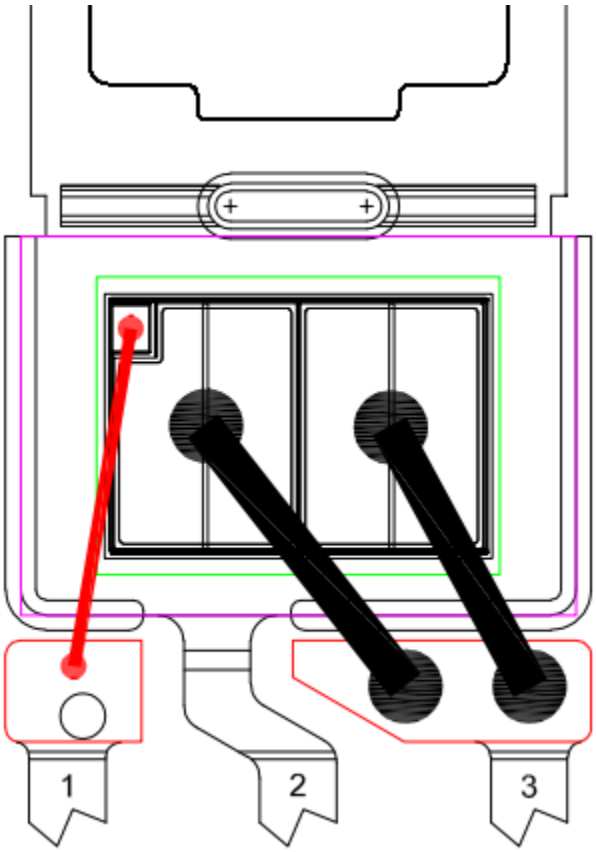
Description

These devices are N-channel Power MOSFETs developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFETs exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB120N4F6	120N4F6	D²PAK	Tape and reel
STD120N4F6		DPAK	

2.1.5. Pin connection/Bonding Diagram Test vehicle 3



2.2. Traceability

2.2.1. Wafer Fab information

Wafer fab name / location	HHGRACE (China) Subcon (6D44A1) ST CT8 Catania (Italy) (OD4QA1) ST CT8 Catania (Italy) (6D4FA1)
Wafer diameter (inches)	8”
Silicon process technology	F6 EHD6 F7 OFT40
Die finishing front side	F6 EHD6: TEOS + Nitride F7 OFT40: TEOS + SiN
Die finishing back side	F6 EHD6: Ti-NiV-Ag F7 OFT40: Ti-NiV-Ag
Die size (micron)	2500 x 2200 (6D44) 3500 x 2150 (OD4Q) 2640 x 3860 (6D4F)
Metal levels/ materials/ thicknesses	F6 EHD6: AlCu (4.0um) F7 OFT40: AlCu (6.0um)

2.2.2. Assembly information

Assembly plant name / location	Tongfu Microelectronics TFME (China) subcon
Package descrition	DPAK
Lead frame/Substrate	TO-252-3Q(IL Ni-NiP) - DWG# TO-LFM-SW017
Die attach material	Soft Solder UMICORE Pb /Sn /Ag (95.5 /2 /2.5)
Wire bonding material/diameter	Al 5 mils Al 15 mils
Molding compound material	SUMITOMO EMEG700HF
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL1

2.2.3. Reliability Testing information

Reliability laboratory location	STM Catania (Italy)

3. Tests Results Summary

3.1. Lot Information

Lot #	Product	Diffusion Lot	Assembly Lot	Diffusion Fab
Lot1	6D44	B1015018	0CO400220101	HHGrace (China) subcon
Lot2			0CO400230101	
Lot3			0CO400240101	
Lot4	OD4Q	5015U5W	0CO400250101	CT8 (Italy)
Lot5			0CO400260101	
Lot6			0CO400270101	
Lot7	6D4F	5309M57	3C0410460101	CT8 (Italy)

3.2. Test results summary (table)

Test method revision reference is the one active at the date of reliability trial execution

Test	#	Reference	AEC-Q101 (Data Type 1) STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/ Lots	Comments
TEST	1		User specification or supplier's standard specification	7	462	3234	0/462/7	All qualification parts
PC	2	-	24h bake@125°C MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	7	308	2156	0/308/7	All parts before TC, H3TRB, AC, IOL
EV	3	JESD22B-101I	All qualification parts submitted for testing	7	462	3234	Passed	
PV	4	-	All parameters according to user specification from 55°C to 150°C	7	25	175	Passed	
HTRB	5	MIL-STD-750-1 M1038 Method A	1000h @ Tj=175°C, Vds=80V	7	77	539	0/77/7	
ACBV	5a	-	-	-	-	-		Not Applicable Thyristors only
HTFB	5b	-	-	-	-	-		Not Applicable LEDs only
SSOP	5c	-	-	-	-	-		Not Applicable Voltage Regulator only
HTGB	6	JESD22 A-108	1000h @ Ta=175°C Vgs= 20V	7	77	539	0/77/7	
TC	7	JESD22A-104	Ta=-55°C /+150°C Duration= 1000cy	7	77	539	0/77/7	

TCHT	7a	JESD22A-104	125°C TEST after TC, followed by decap and wire pull on all wires	7	77	539	0/77/7	
TCDT	7a alt	JESD22A-104	100% C-SAM inspection after TC	7	5	35	Passed	
WBI	7b	MIL-STD-750 Method 2037	-	7	5	35	Passed	
UHAST	8	-	-	-	-	-		NO, covered by AC
AC	8 alt	JESD22 A-102	**ENV. SEQ. (ES) Environmental Sequence** TC (Ta=-55°C / +150°C for 100 cycles) + AC (Ta=121°C, Pa=2atm for 96 hours)	7	77	539	0/77/7	
HAST	9	-	-	-	-	-		NO, covered by H3TRB
H3TRB	9 alt	JESD22A-101	1000h @ Ta=85°C, RH=85% Vds=32V	7	77	539	0/77/7	
HTHHB	9a	-	-	-	-	-		Not Applicable LEDs only
IOL	10	MIL-STD-750 Method 1037	10Kcy @ Ta=25°C with parts powered to insure $\Delta Tj \geq 100°C$ (not to exceed absolute maximum ratings).	7	77	539	0/77/7	
PTC	10alt	-	-	-	-	-		NO, covered by IOL
ESD	11	AEC-Q101-001 and AEC-Q101-005	HBM / CDM	7	30	210	Done	HBM - Class H1C CDM - Class C3 >1000V
DPA	12	AEC-Q101-004 section 4		7			Passed	Devices after TC, H3TRB

Test	#	Reference	AEC-Q101 (Data Type 2) STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
PD	13	JESD22B-100		3	30	90	Passed	From assembly data
TS	14	MIL-STD-750 Method 2036		3	30	90	Passed	From assembly data
RTS	15	-	-	-	-	-	-	Not Applicable
CA	16	-	-	-	-	-	-	Not Applicable
VVF	17	-	-	-	-	-	-	Not Applicable
MS	18	-	-	-	-	-	-	Not Applicable
HER	19	-	-	-	-	-	-	Not Applicable
RSH	20	-	-	-	-	-	-	Not Applicable
SD	21	JEDEC J-STD-002	-	3	10	30	Passed	From assembly data

Test	#	Reference	AEC-Q101 (Data Type 3) STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
TR	22	JESD24-3		7	5	35	Passed	From assembly data
WBS	23	MIL-STD-750 Method 2037	-	7	5	35	Passed	From assembly data
BS	24	AEC-Q101-003		7	5	35	Passed	From assembly data
DS	25	MIL-STD-750 Method 2017		7	5	35	Passed	From assembly data
UIS	26	AEC-Q101-004 Section 2		7	5	35	Done	
DI	27	AEC-Q101-004 Section 3		7	5	35	Done	
SCR	28	-	-	-	-	-	-	Not Applicable
LF	29	-	-	-	-	-	-	Not Applicable

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