PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data

1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/23/14358
1.3 Title of PCN	L5300AH7TR (UN41): New leadframe introduction
1.4 Product Category	L5300AH7TR
1.5 Issue date	2023-11-23

2. PCN Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Vito GRAZIANO
2.1.2 Marketing Manager	Giovanni Luca TORRISI
2.1.3 Quality Manager	Marcello Donato MENCHISE

3. Change

3.1 Category	**3.2 Type of change**	**3.3 Manufacturing Location**
Materials	New direct material part number (same supplier, different supplier or new supplier), Lead frame finishing material / area (internal)	ST Shenzhen - China

4. Description of change

	Old	**New**
4.1 Description	Leadframe Ni/Ag	Leadframe Ni/NiP+Ag
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change

5.1 Motivation	Service Continuity
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change

6.1 Description	Date Code

7. Timing / schedule

7.1 Date of qualification results	2023-10-17
7.2 Intended start of delivery	2024-01-31
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation

8.1 Description	14358 Qualification.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	**Issue Date**	2023-11-23

9. Attachments (additional documentations)

14358 Public product.pdf
14358 detail.pdf
14358 Qualification.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	L5300AH7TR	

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Product/process change notification:

L5300AH7TR (UN41): New leadframe introduction

ADG/23/14358

Product family	Technology	Package
L5300AH7TR	BCD5	HPAK

(optional)

Description of the change
Current leadframe with **Selective Ni/Au** spot on leads, will be replaced by new one with **Selective Ni-NiP/Ag** spot on leads.

Reason
Service continuity

Date of implementation
January 2024

Impact of the change	
Form	No impact
Fit	No impact
Function	No impact
Reliability	No impact
Processibility	No impact

Qualification of the change

Enclosed to this Notification

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PCN Title : L5300AH7TR (UN41): New leadframe introduction
PCN Reference : ADG/23/14358

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

L5300AH7TR		

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Reliability Evaluation Report
New lead frame introduction on HPAK package
L5300AH7 (A695*UN41AA6)
in BCD5 Technology
ST Shenzhen (China) Assembly plant

Test vehicle general information	
Commercial Products:	L5300AH7
Product Lines:	A695*UN41AA6
Package:	HPAK 7L
Silicon Technology:	BCD5

***Note**: this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Revision history

Rev.	Changes description	Author	Date
1	Creation	G. Carlino	13/09/2023

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Castelletto (Italy)	G. Carlino	13/09/2023

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objective

Aim of this report is to present the results of the reliability evaluation performed on L5300AH7 product assembled on HPAK package in ST Shenzhen (China) assembly plant, to qualify a new plating for the frame provided by Mitsui High-Tec. (MHT) supplier designed in Ni/NiP+Ag.

The selected vehicle is:
L5300AH7 (A695*UN41AA6 as ST internal code)
Automotive 5 V low drop voltage regulator

1.2 Reliability Strategy and Test Plan

1.2.1 Reliability strategy

Reliability trials were performed on three lots of **L5300AH7** (A695*UN41AA6) in agreement with ST 0061692 and **AEC-Q100 rev. H Grade 1** requirements in case of plating lead frame material change and are listed in below Test Plan.

For details on test conditions, generic data used, and specifications references refer to test results summary in section 3.

In the below table a comparison between the AEC-Q100 and ZVEI requirements in case of plating lead frame material change vs the applied ST qualification plan is reported:

	Test Group A					Test Group B		Test Group C				Test Group D					Test Group E					
	THB	AC	TC	PTC	HTSL	HTOL	ELFR	WBS	WBP	SD	PD	EM	TDDB	HCI	NBTI	SM	HBM	CDM	LU	ED	EMC	SC
AEC-Q100	x	x	x		x					x												
ZVEI	x	x	x		x					x												
ST	x	x	x		x					x												

No deviation between the requirement and the applied reliability plan

1.2.2 Test Plan

AEC-Q100 TEST PLAN

TEST GROUP	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
A Accelerated Environment Stress Tests	PC (JL3)	Preconditioning (JL3+3 reflows simulation)	Yes
	THB	Temperature Humidity Bias	Yes
	AC	Autoclave at 2atm	Yes
	TC	Temperature Cycling	Yes
	PTC	Power Temperature Cycling	Not Applicable
	HTSL	High Temperature Storage Life	Yes
B Accelerated Lifetime Simulation Tests	HTOL	High Temperature Operating Life	Not Applicable
	ELFR	Early Life Failure Rate	Not Applicable
	EDR	Endurance Data Retention	Not Applicable
C Package Assembly Integrity Tests	WBS	Wire Bond Shear	Not Applicable
	WBP	Wire Bond Pull	Not Applicable
	SD	Solderability	Yes
	PD	Physical Dimension	Not Applicable
	SBS	Solder Ball Shear	Not Applicable
	LI	Lead Integrity	Not Applicable
D Die Fabrication Reliability Tests	Test list is reported in section 5	Performed during process qualification	Not Applicable
E Electrical Verification Tests	ESD (HBM)	Electrostatic Discharge (Human Body Model)	Not Applicable
	ESD (CDM)	Electrostatic Discharge (Charged Device Model)	Not Applicable
	LU	Latch Up	Not Applicable
	ED	Electrical distribution	Not Applicable
	FG	Fault grading	Not Applicable
	CHAR	Characterization	Not Applicable
	EMC	Electromagnetic Compatibility	Not Applicable
	SC	Short Circuit Characterization	Not Applicable
	SER	Soft Error Rate	Not Applicable
	LF	Lead (Pb) Free: (see AEC-Q005)	Not Applicable
F Defect Screening Tests	Test list is reported in section 5	To be implemented starting from first production lot	No
G Cavity Package Integrity Tests	Test list is reported in section 5	N/A: not for plastic packaged devices	Not Applicable

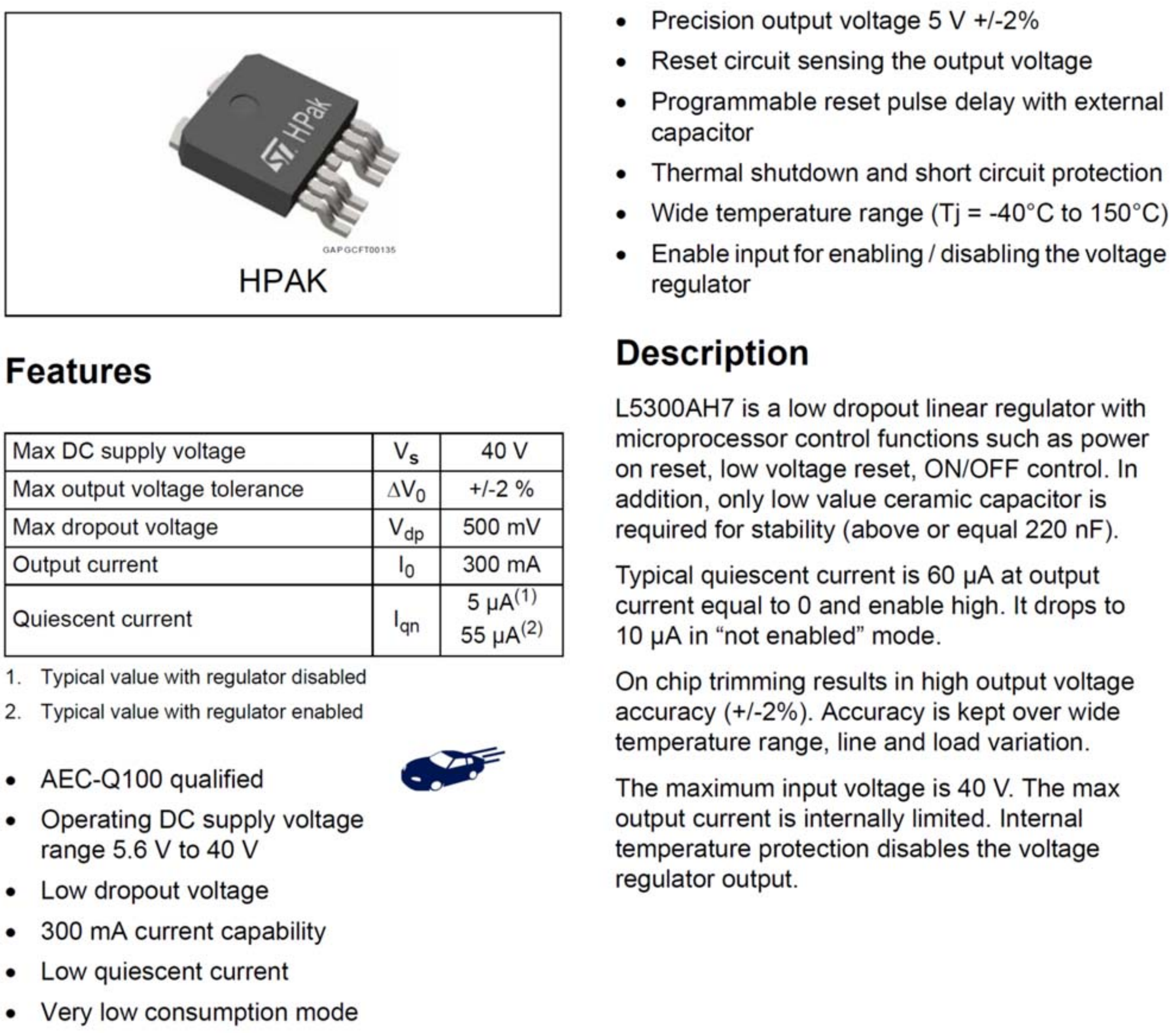
1.3 Conclusion

Reliability tests have been completed with positive results.
Neither functional nor parametric rejects were detected at final electrical testing.

Based on the overall results obtained, L5300AH7 (A695*UN41AA6) assembled on HPAK package in ST Shenzhen (China) assembly plant with the new plating for the frame provided by Mitsui High-Tec. (MHT) supplier designed in Ni/NiP+Ag has positively passed the reliability evaluation performed in agreement to AEC_Q100 Rev. H specification Grade 1.

2. Product Characteristics

2.1. Generalities



HPAK

Features

Max DC supply voltage	V_s	40 V
Max output voltage tolerance	ΔV_0	+/-2 %
Max dropout voltage	V_{dp}	500 mV
Output current	I_0	300 mA
Quiescent current	I_{qn}	5 µA(1) 55 µA(2)

1. Typical value with regulator disabled
2. Typical value with regulator enabled

- AEC-Q100 qualified
- Operating DC supply voltage range 5.6 V to 40 V
- Low dropout voltage
- 300 mA current capability
- Low quiescent current
- Very low consumption mode
- Precision output voltage 5 V +/-2%
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Thermal shutdown and short circuit protection
- Wide temperature range (Tj = -40°C to 150°C)
- Enable input for enabling / disabling the voltage regulator

Description

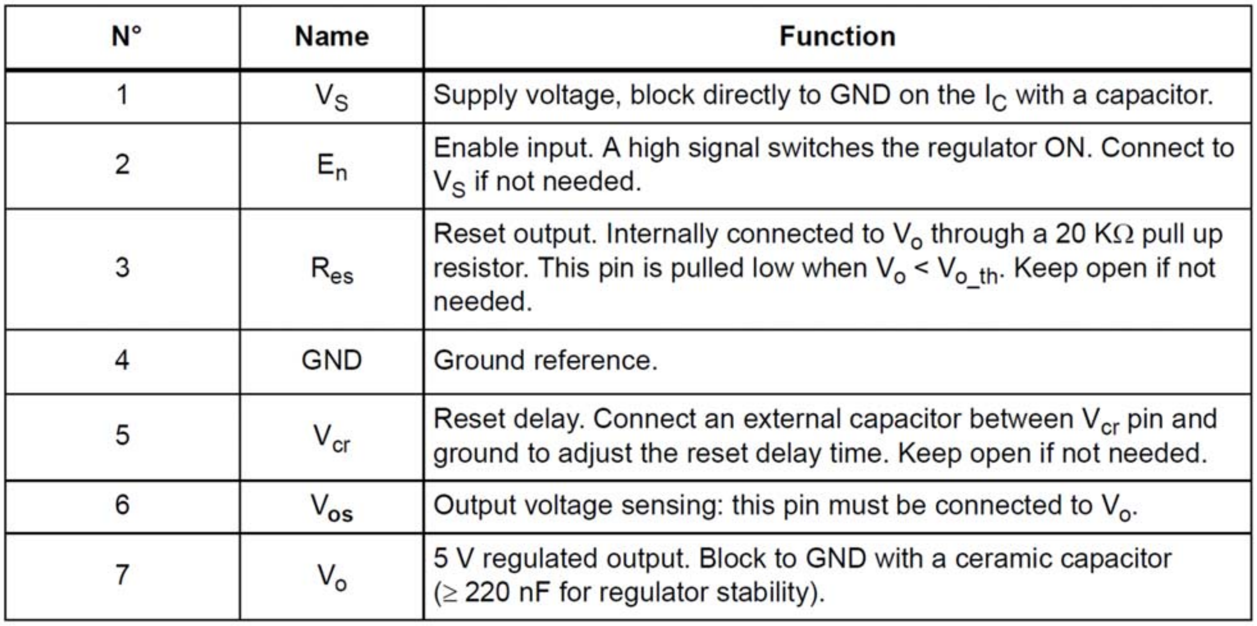
L5300AH7 is a low dropout linear regulator with microprocessor control functions such as power on reset, low voltage reset, ON/OFF control. In addition, only low value ceramic capacitor is required for stability (above or equal 220 nF).

Typical quiescent current is 60 µA at output current equal to 0 and enable high. It drops to 10 µA in “not enabled” mode.

On chip trimming results in high output voltage accuracy (+/-2%). Accuracy is kept over wide temperature range, line and load variation.

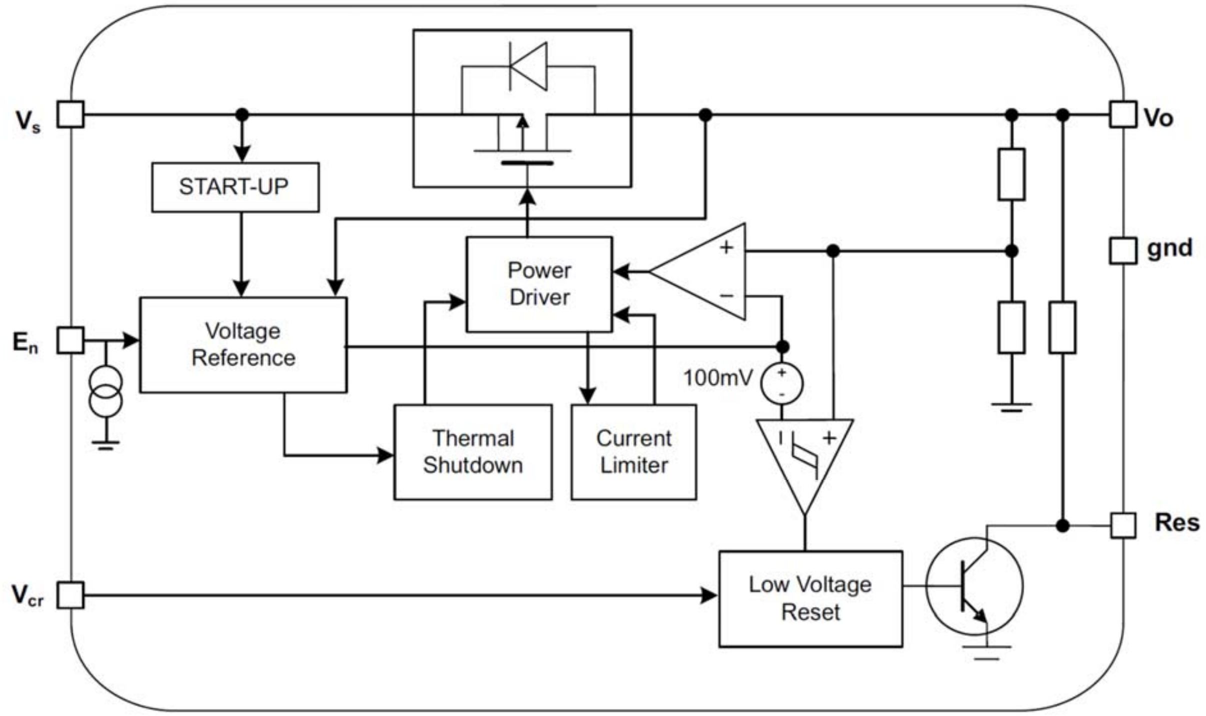
The maximum input voltage is 40 V. The max output current is internally limited. Internal temperature protection disables the voltage regulator output.

2.2. pins connection

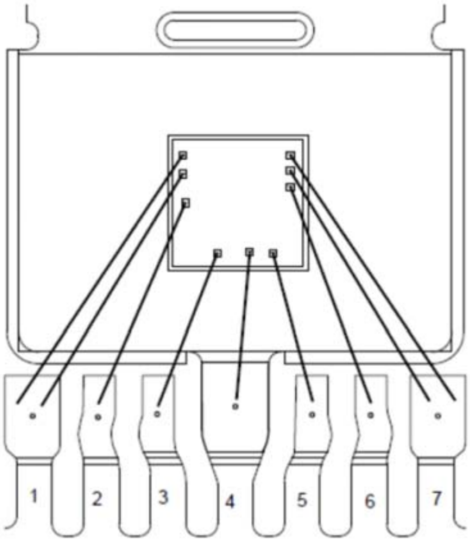


N°	Name	Function
1	V_S	Supply voltage, block directly to GND on the I_C with a capacitor.
2	E_n	Enable input. A high signal switches the regulator ON. Connect to V_S if not needed.
3	R_{es}	Reset output. Internally connected to V_o through a 20 KΩ pull up resistor. This pin is pulled low when $V_o < V_{o\_th}$. Keep open if not needed.
4	GND	Ground reference.
5	V_{cr}	Reset delay. Connect an external capacitor between V_{cr} pin and ground to adjust the reset delay time. Keep open if not needed.
6	V_{os}	Output voltage sensing: this pin must be connected to V_o.
7	V_o	5 V regulated output. Block to GND with a ceramic capacitor (≥ 220 nF for regulator stability).

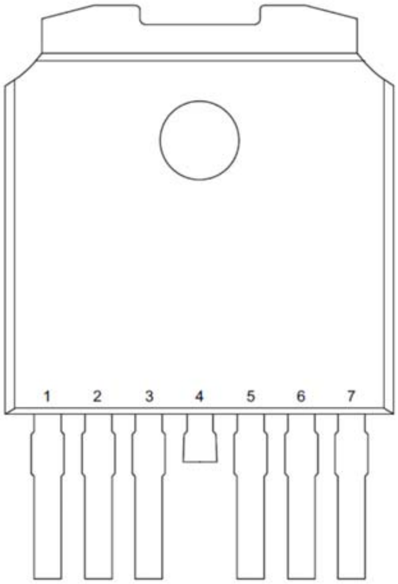
2.3. Block diagram



2.4. Bonding diagram



A695*UN41AA6



HPAK

2.5 Traceability

2.5.1 Wafer Fab information

Commercial Product	L5300AH7
Wafer fab name / location	ST Singapore /SG6
Wafer diameter (inches)	6”
Silicon process technology	BCD5
Line code	UN41
Die finishing front side	Teos + PTeos + SiOn + PIX
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size (micron)	1780 x1730
Metal levels/ materials/ thicknesses	Metal 1 Ti/AlSiCu/TiN 0.400 UM Metal 2 Ti/AlSiCu/TiN 0.800 UM Metal 3 Ti/AlSiCu/TiN 3.000 UM

2.5.2 Assembly information

Commercial Product	L5300AH7
Assembly plant name / location	ST Shenzhen (China)
Package description	TO-252 6 LEADS SMD (HPAK 7L)
Lead frame description (material/thickness)	FRAME HPAK 7L: MHT New LF 5FT00435 with Selective Ni/NiP+Ag Plating.
Die attach material	PREFORM Pb/Ag/Sn 95.5/2.5/2
Wire bonding material/diameter	Au D1.3
Molding compound material	RESIN SUMITOMO EME7026

2.5.3 Reliability Testing information

Reliability laboratory location	ST Shenzhen (China), ST Castelletto (Italy)

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Lot #	Commercial product	Lot
1	L5300AH7 (A695*UN41AA6)	GK04329L02
2	L5300AH7 (A695*UN41AA6)	GK04329LRP
3	L5300AH7 (A695*UN41AA6)	GK04329LRQ

3.2 Test results summary

Test method revision reference is the one active at the date of reliability trial execution.

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
PC	A1	JESD22-A113 J-STD-020	24h bake@125°C, 192hrs@60°C/60% RH 3x Reflow	3	231	683	0/231/3	Before THB/AC/TC
THB	A2	JESD22 A101 JESD22 A110	Ta=85°C, 85%RH, Duration= 1000 hrs	3	77	231	0/77/3	
AC	A3	JESD22 A102 or JESD22 A118 or JESD22-A101	**ENV. SEQ.** **Environmental Sequence** TC (Ta=-55°C / +150°C for 100 cycles) + AC (Ta=121°C, Pa=2atm for 96 hours)	3	77	231	0/77/3	
TC	A4	JESD22 A104	Ta=-55°C /+150 °C Duration=1000 cycles Duration=1500 cycles	3	77	231	0/77/3	
PTC	A5	JESD22 A105	Ta=-40°C /+125 °C Duration=1000 cycles	-	-	-	-	Not Applicable
HTSL	A6	JESD22 A103	Ta= 150°C Duration= 1000 hrs Duration= 1500 hrs	3	77	231	0/77/3	

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
HTOL	B1	JESD22 A108	TJ=150°C Duration= 1000hrs Bias dynamic stress (**OLT**)	-	-	-	-	Not Applicable
HTOL	B1	JESD22 A108	Ta=150°C Duration= 1000hrs Bias static stress (HTB)	-	-	-	-	Not Applicable
ELFR	B2	AEC-Q100-008	Ta max=150°C Duration=24hrs	-	-	-	-	Not Applicable
EDR	B3	AEC-Q100-005	Specific tests and conditions to be defined in case of NVM	-	-	-	-	Not Applicable

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear: (Cpk > 1.67)	-	-	-	-	Not Applicable
WBP	C2	Mil-STD-883, Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67)	-	-	-	-	Not Applicable
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8hr steam aging prior to testing	3	80	240	All measurement within spec limits	
PD	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	-	-	-	-	Not Applicable
SBS	C5	AEC-Q100-010 AEC-Q003	Only for BGA package	-	-	-	-	Not Applicable
LI	C6	JESD22 B105	Not required for Surface Mount Devices	-	-	-	-	Not Applicable

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
EM	D1	JESD61	Data, test method and criteria available upon request	–	–	–	–	Not Applicable
TDDB	D2	JESD35	Data, test method and criteria available upon request	–	–	–	–	
HCI	D3	JESD60 & 28	Data, test method and criteria available upon request	–	–	–	–	
NBTI	D4	JESD90	Data, test method and criteria available upon request	–	–	–	–	
SM	D5	JESD61, 87, & 202	Data, test method and criteria available upon request	–	–	–	–	

GROUP E – ELECTRICAL VERIFICATION

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test	All	All	All	Passed	All parametric and functional tests
HBM	E2	AEC-Q100-002	Target: ±2kV	–	–	–	–	Not Applicable
CDM	E3	AEC-Q100-011	Target: ±750V on corner pins	–	–	–	–	Not Applicable
LU	E4	AEC-Q100-004	Current Injection Class II – Level A (+/-	–	–	–	–	Not Applicable
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where	–	–	–	–	Not Applicable
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	–	–	–	–	Not Applicable
SC	E10	AEC Q100-012	Short Circuit Characterization	–	–	–	–	Not Applicable
SER	E11	JESD89-1 JESD89-2 JESD89-3	Applicable to devices with memory	–	–	–	–	Not Applicable
LF	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	–	–	–	–	Not Applicable

TEST GROUP F – DEFECT SCREENING TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	Not performed on qualification lots. It will be implemented starting from first production lot				
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)					

TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
MS	G1	JESD22 B104	Mechanical Shock	Not Applicable: not for plastic packaged devices				
VFV	G2	JESD22 B103	Variable Frequency Vibration					
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration					
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak					
DROP	G5		Drop Test, Package Drop					
LT	G6	MIL-STD-883 Method 2004	Lid Torque					
DS	G7	MIL-STD-883 Method 2019	Die Shear					
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor					

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