PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/23/14049
1.3 Title of PCN	Transfer of assembly and test line qualification for modules housed in ACEPACKSMIT package
1.4 Product Category	STTH60RQ06-M2Y STTN6050H-12M1Y STTD6050H-12M2Y
1.5 Issue date	2023-07-10

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Stephane CHAMARD
2.1.2 Marketing Manager	Philippe LEGER
2.1.3 Quality Manager	Jean-Paul REBRASSE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	Subcontractor in Philippines STMicroelectronics Shenzhen in China

4. Description of change		
	Old	New
4.1 Description	Subcontractor in Philippines	STMicroelectronics Shenzhen - China
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No	

5. Reason / motivation for change	
5.1 Motivation	In the frame of the discontinuation of subcontractor assembly line, STMicroelectronics has initiated a transfer of ACEPACKSMIT package to ST Shenzhen plant (China).
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change	
6.1 Description	Finished Good/type (ending by 7)

7. Timing / schedule	
7.1 Date of qualification results	2023-06-26
7.2 Intended start of delivery	2023-08-11
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	14049 23015QRP Rev1.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2023-07-10

9. Attachments (additional documentations)

14049 Public product.pdf
14049 PCN Transfer AcePackSmit in STS.pdf
14049 23015QRP Rev1.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STTD6050H-12M2Y	
	STTH60RQ06-M2Y	
	STTN6050H-12M1Y	

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Qualification Report

Transfer qualification of ACEPACK™ SMIT package to Shenzhen plant (China)

General Information	
Product Line	*Rectifiers*
Product Description	*Automotive 600V ultrafast bridge module*
Product Perimeter	*STTH60RQ06-M2Y*
Product Group	*ADG*
Product Division	*Discrete & Filter*
Packages	*ACEPACK™ SMIT*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST Tours - France*
Assembly Plant	*ST Shenzhen - China*
Reliability Lab	*ST Tours – France*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	June 20; 2023	16	Henri VIVANT		Qualification of STTH60RQ06-M2Y

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101 Rev. E	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications
AQG 324	Qualification of Power Modules for Use in Power Electronics Converter Units in Motor Vehicles
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

DBT	Dead Bug Test
H3TRB	High Humidity High Temperature Reverse Bias
HTRB	High Temperature Reverse Bias
LTS	Low Temperature Storage
MS	Mechanical Shocks
PC	Preconditioning
PD	Physical Dimensions
PCmin	Power Cycling (minutes)
PCsec	Power Cycling (seconds)
PV	Parametric Verification
SD	Solderability test
SS	Sample Size
TST	Thermal Shocks Test
TW/WG	Tin Whiskers / Whiskers Growth
V	Vibration

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify the transfer of ACEPAK™ SMIT package to Shenzhen plant (Back End China). Qualification performed on **STTH60RQ06-M2Y** product, Automotive 600 V ultrafast bridge module embedded in ACEPACK SMIT package.

Table of involved products:

Commercial Product	Package	Comment
STTH60RQ06-M2Y	ACEPACK™ SMIT	Automotive Grade

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology » and AQG-324 guidelines. STTH60RQ06 die into the power module is already qualified AECQ101rev E in a discrete package.

The reliability tests ensuing are:

- TST to ensure the mechanical robustness of the product.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, HTS to check the robustness to corrosion and the good package hermeticity.
- Solderability and DBT to check compatibility of package with customer assembly.
- TW/WG to check lead-finishing quality.
- LTS to check the robustness to aging or transport at very low temperature.
- PC min / PC sec to evaluate the robustness of the chip near interconnections (die-attach and top-side contacting).
- V to check suitability of the mechanical structure for use in PCUs.
- MS to simulate the mechanical load of the module in PCUs.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

Based on these results, **STTH60RQ06-M2Y** is compliant with AQG-324.

4 DEVICE CHARACTERISTICS

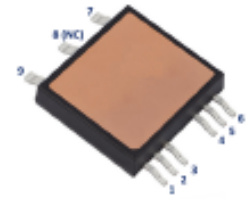
4.1 Device description

life.augmented

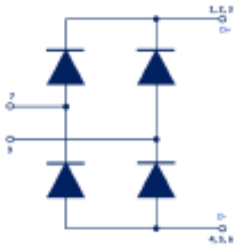
STTH60RQ06-M2Y

Datasheet

Automotive 600 V, 60 A ultrafast bridge module



ACEPACK SMIT



Features

- Operating T_J from -40 °C to +175 °C
- Ultrafast with soft recovery behaviour
- PPAP capable
- SMD with isolated top side cooling
- Low thermal resistance
- Backside in insulated ceramic
- Dice chips on Direct Bond Copper (DBC) substrate
- ECOPACK2 compliant
- MSL: Level 3
- Insulation voltage (UL 1557): V_{RMS} = 4000 V

Applications

- Output rectification
- On board charger
- Charging station

Description

The ultrafast bridge rectifier is a high-performance device, generally used in a full wave rectification of an output stage of a DC/DC converter in automotive applications.

Thanks to the high thermal capability of the ACEPACK SMIT package, this integrated module will increase the power density in the application, through very high thermal performances (top side cooling) and insulation done by an embedded ceramic. Especially suited for use in Charger applications, either integrated in the vehicle or in a charging station, this rectifier will enhance the performance of the targeted application.

Product status link
STTH60RQ06-M2Y

Device summary (per diode)	
$I_{F(AV)}$	30 A
V_{RRM}	600 V
V_F (typ.)	1.45 V
t_{rr} (max.)	30 ns
T_J	-40 °C to +175 °C

4.2 Construction Note

	STTH60RQ06-M2Y
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours- France
Technology / Process family	Automotive 600V Ultrafast bridge module
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours- France
Assembly information	
Assembly site	ST Shenzhen - China
Package description	ACEPACK™ SMIT
Molding compound	ECOPACK®2 compliant component
Lead finishing material	Lead free (pure Tin)
Final testing information	
Testing location	ST Shenzhen - China

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	STTH60RQ06-M2Y	ACEPACK™ SMIT	1st Qualification lot
L2	Dummy of setup	ACEPACK™ SMIT	Lot for whiskers test
L3	RQ Diode MAT10	ACEPACK™ SMIT	Lot for whiskers test
L4	KGFN MAT 10	ACEPACK™ SMIT	Lot for whiskers test
L5	STTH60RQ06-M2Y	ACEPACK™ SMIT	Lot for SD test

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL Not applicable for PTH and WLCSP without coating	X
MSL research	MSL	J-STD-020			Not applicable for PTH and WLCSP without coating	
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	
Parametric Verification	PV	User specification	See annex 6.1			x
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L1	6	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A			Required for Thyristor only. Alternative to HTRB	
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for Power MOSFET – IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104				
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for Power MOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for Power MOSFET – IGBT only. Alternative to TCHT	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101			Required for SCR/TRIAC RECTIFIER and Protection devices	
Autoclave	AC	JESD22A-102			Alternative to UHAST	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB (same failure mechanisms activation).	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1	6	Alternative to HAST	X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037			For power devices. Not required for Transient Voltage Suppressor (TVS) parts	
Power and Temperature Cycle	PTC	JED22A-105			For power devices. Not required for Transient Voltage Suppressor (TVS) parts	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
					Perform PTC if ΔTj>100°C cannot be achieved with IOL Alternative to IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005				
ESD Characterization	ESD CDM	AEC Q101-001 and 005				
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4			After H3TRB and TC	
Physical Dimension	PD	JESD22B-100	See annex 6.2			x
Terminal Strength	TS	MIL-STD-750 Method 2036			Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)			Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102	L5	8		X
Dead Bug Test	DBT	ST Internal specification	L1	30	Mandatory for SMD package Data collection for PTH package	X
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate			Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037			Covered during workability trials	
Bond Shear	BS	AEC-Q101-003			Covered during workability trials	
Die Shear	DS	MIL-STD-750 Method 2017			Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for Power MOSFET – IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201	L2/ L3 /L4	See test method		X
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,…)	FT	Internal specification				
Repetitive Surge	RS	Internal specification			Required for protection devices only.	
Low Temperature Storage	LTS	JESD-22 A119: 209	L1	6	AQG324 test for Modules	X
Thermal shock test	TST	JESD22-A104	L1	6	AQG324 test for Modules	X
Power Cycling (seconds)	PC sec	MIL-STD750-1 Method1037	L1	6	AQG324 test for Modules	X
Power Cycling (minutes)	PC min	MIL-STD750-1 Method1037	L1	6	AQG324 test for Modules	X
Mechanical shock	MS	IEC 600068-2-27	L1	6	AQG324 test for Modules	X
Vibration	V	IEC60068-2-6	L1	6	AQG324 test for Modules	X

5.3 Results summary

Test	PC	Std ref.	Conditions	Step / Duration	SS	Failure / SS				
						L1	L2	L3	L4	L5
Pre-and Post-Electrical Test			Ir, Vf parameters following product datasheet	-	42	0/42				
Parametric Verification			ST datasheet	Refer to paragraph 6.1 in Annexes						
PD			JESD22 B-100	Refer to paragraph 6.3 in Annexes						
V	N	IEC60068-2-6		8hrs	6	0/6				
MS	N	IEC 600068-2-27	Acceleration=50 G	6ms	6	0/6				
TST	Y	JESD22A-104	-55/+150°C 2cy/h	1Kcy	6	0/6				
				3Kcy	6	0/6				
HTRB	N	MIL-STD-750-1 M1038 Method A	Junction Temperature=175°C Temperature=170°C Voltage=480V	1Krs	6	0/6				
H3TRB	Y	JESD22A-101	85°C; 85% RH Voltage=100V	1Krs	6	0/6				
LTS	Y	JESD-22 A-119:2009	Temperature=-65°C	1Khrs	6	0/6				
HTS	Y	IEC 60749-6:2002	Junction Temperature=175°C	1Khrs	6	0/6				
PC min	Y	MIL-STD 750 Method 1037	Delta Tj=100°C Time (off)=15s Time (on)=45s	6720 cy	6	0/6				
PC sec	Y	MIL-STD 750 Method 1037	Delta Tj=100°C Time (off)=45 Time (on)=15s	6720 cy	6	0/6				
PC	Y	JESD22-A113	Humidity (HR)=60% MSL=3 Temperature)30°C	After MSL 3	6	0/6				
SD	N	J-STD-002 JESD22 B-102	Wet ageing SnPb bath 220°C	-						0/2
			Dry ageing SnPb bath 220°C							0/2
			Wet ageing SnAgCu bath 245°C							0/2
			Dry ageing SnAgCu bath 245°C							0/2
Tin Whiskers	N	AEC-Q005 JESD201	Pb free reflow TC -40°C/85°C	1500 cy		0/9 (3 lots)	0/3	0/3	0/3	
			Pb free reflow THS 55°C / RH = 85%	4000 hrs		0/9 (3 lots)	0/3	0/3	0/3	

			No reflow THS 30°C / RH = 60%	4000 hrs		0/9 (3 lots)	0/3	0/3	0/3	
			SnPb reflow TC -40°C/85°C	1500 cy		0/9 (3 lots)	0/3	0/3	0/3	
			SnPb reflow THS 55°C / RH = 85%	4000 hrs		0/9 (3 lots)	0/3	0/3	0/3	

* On 6 units all the current paths have been tested (2diodes / path)

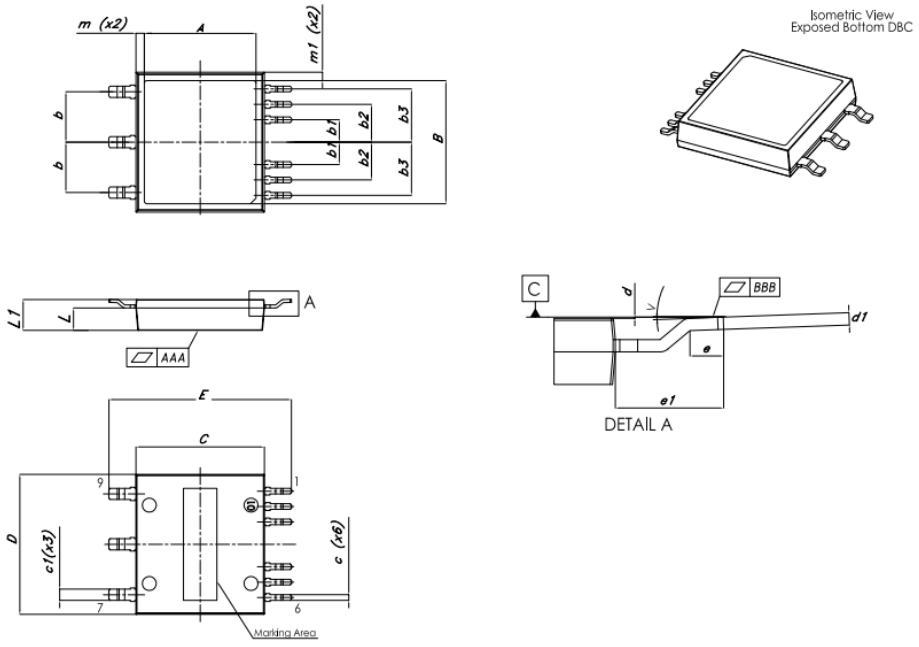
6 ANNEXES

6.1 Parametric Verification

TEST	IR (µA)	VR (V)	VF 15A (V)	VF 30A (V)	IR (µA)	VR (V)	VF 15A (V)	VF 30A (V)	IFSM (A)
EQUIPMENT	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	ASTEEL_2000A
Condition 1	**25°C**	**25°C**	**25°C**	**25°C**	**150°C**	**150°C**	**150°C**	**150°C**	**25°C**
Condition 2	VAK=600V	IAK=40uA	IAK=15A	IC=30A	VAK=600V	IAK=1mA	IAK=15A	IC=30A	TP=10ms
Condition 3	Ar=1		Ar=1	Ar=1	Ar=1	VMAX=900V	Ar=1	Ar=1	
Condition 4	TIME=100ms	Ar=1	TIME=380us	Rv=1	TIME=50ms	Ar=1	TIME=380us	Rv=1	
Condition 5		TIME=100ms		TIME=380us		TIME=20ms		TIME=380us	
Condition 6									
Min. Datasheet		600V				600V			180A
Typ. Datasheet									
Max. Datasheet	40µA		2.45V	2.95V	800uA		1.45V	1.85V	
N	***24***	***24***	***24***	***24***	***24***	***24***	***24***	***24***	***6***
Min	0.035	683.3	1.37	1.585	138.5	743.5	0.967	1.184	385
Max	0.080	700	1.486	1.746	176.20	761.9	1.016	1.268	420
Moy.	0.052	691.125	1.423	1.657	151.187	751.850	0.991	1.224	403

6.2 Physical Dimensions

ACEPAK™ SMIT package outline:



Dimensional Report for ACEPAK™ SMIT at Shenzhen in China:

Dimensions	Parameters									
	A	B	C	D	E	b	b1	b2	b3	c
1	19.740	21.829	23.000	24.941	32.720	8.698	3.274	5.914	8.592	1.028
2	19.888	21.848	23.031	25.002	32.778	8.660	3.304	5.904	8.593	1.035
3	19.817	21.984	23.001	24.951	32.758	8.722	3.314	5.943	8.677	1.065
4	19.929	21.880	23.017	25.003	32.790	8.710	3.386	6.042	8.709	1.041
5	19.857	21.890	23.009	24.992	32.791	8.839	3.116	5.790	8.990	1.045
6	19.811	21.871	23.078	24.934	32.775	8.687	3.097	5.804	8.510	1.037
7	19.842	21.882	23.001	24.964	32.785	8.692	3.845	5.493	8.165	1.043
8	19.877	21.812	22.997	24.963	32.797	8.742	3.828	6.424	9.120	1.030
9	19.844	21.747	23.001	24.998	32.792	8.750	3.681	6.259	8.941	1.035
10	19.875	21.754	22.995	24.938	32.779	8.774	3.817	6.408	9.088	1.039
11	19.868	21.726	23.005	24.983	32.782	8.824	3.501	6.181	8.914	1.025
12	19.856	21.825	23.152	24.983	32.778	8.785	3.668	6.271	8.923	1.043
13	20.073	21.935	23.005	25.047	32.786	8.748	3.501	6.086	8.796	1.041
14	19.893	21.765	23.001	25.027	32.773	8.769	3.844	6.472	9.233	1.057
15	19.870	21.967	23.003	24.997	32.799	8.996	3.936	6.686	9.436	1.014
16	19.813	21.818	23.002	25.049	32.779	8.995	4.112	6.860	9.615	1.018
17	19.873	21.926	22.997	24.992	32.801	9.012	3.918	6.670	9.428	1.020
18	19.987	21.863	23.082	24.980	32.796	8.994	3.781	6.534	9.282	1.019
19	19.853	21.966	22.996	24.921	32.799	8.998	3.813	6.563	9.316	1.021
20	20.006	21.844	23.004	25.018	32.803	8.998	3.851	6.603	9.358	1.034
21	19.885	21.880	22.998	25.030	32.794	9.002	4.080	6.829	9.589	1.018
22	19.814	21.859	23.085	24.954	32.790	9.003	3.949	6.697	9.452	1.045
23	19.983	21.985	23.004	25.046	32.796	9.005	3.786	6.533	9.285	1.012
24	19.878	21.865	23.022	24.958	32.776	8.998	3.863	6.625	9.379	1.011
25	19.824	21.870	23.055	24.992	32.786	9.003	3.858	6.611	9.364	1.029
26	19.966	21.860	23.008	24.972	32.787	8.994	3.815	6.567	9.308	1.019
27	19.742	21.889	23.005	25.066	32.796	8.995	3.873	6.624	9.375	1.013
28	19.859	21.827	23.002	25.016	32.791	8.998	3.773	6.623	9.270	1.029
29	19.847	21.843	23.012	24.998	32.770	8.994	4.013	6.673	9.523	1.034
30	19.860	21.869	23.013	25.001	32.780	8.999	3.952	6.703	9.442	1.023
Min	19.740	21.726	22.995	24.921	32.720	8.660	8.660	3.097	5.493	1.011
Max	20.073	21.985	23.152	25.066	32.803	9.012	9.012	4.112	6.860	1.065
Avg	19.874	21.863	23.019	24.991	32.784	8.879	8.879	3.718	6.380	1.031

Dimensions	Parameters									
	c1	d	d1	e	e1	L	L1	m	m1	V
1	2.012	0.078	0.546	1.466	4.863	3.993	5.509	1.496	1.497	1.792
2	2.009	0.098	0.549	1.464	4.883	3.996	5.491	1.518	1.498	1.914
3	2.009	0.098	0.537	1.462	4.817	4.010	5.488	1.493	1.496	1.921
4	2.001	0.108	0.541	1.472	4.870	3.993	5.509	1.528	1.485	1.832
5	1.995	0.057	0.539	1.459	4.869	3.992	5.492	1.512	1.527	1.430
6	2.006	0.080	0.521	1.439	4.872	3.996	5.497	1.526	1.491	1.747
7	2.011	0.068	0.539	1.498	4.869	3.987	5.481	1.514	1.502	1.703
8	2.017	0.069	0.545	1.451	4.872	3.995	5.486	1.509	1.549	2.148
9	1.999	0.084	0.537	1.480	4.869	3.989	5.501	1.517	1.498	1.793
10	2.002	0.069	0.561	1.472	4.882	3.995	5.478	1.505	1.495	2.069
11	1.998	0.078	0.560	1.487	4.847	3.994	5.502	1.511	1.505	2.311
12	2.005	0.080	0.551	1.481	4.855	3.992	5.497	1.497	1.494	2.504
13	2.051	0.069	0.518	1.480	4.751	3.999	5.560	1.514	1.502	1.879
14	2.005	0.082	0.526	1.501	4.737	3.992	5.478	1.542	1.519	1.438
15	2.005	0.082	0.553	1.499	4.877	3.997	5.485	1.506	1.550	2.060
16	2.018	0.074	0.548	1.468	4.860	3.995	5.472	1.512	1.513	2.383
17	2.003	0.086	0.547	1.469	4.879	3.990	5.459	1.584	1.541	2.545
18	1.997	0.073	0.534	1.466	4.882	3.998	5.477	1.517	1.505	2.749
19	1.994	0.086	0.539	1.496	4.851	3.992	5.483	1.498	1.510	2.167
20	1.997	0.069	0.518	1.486	4.845	3.993	5.495	1.501	1.551	1.890
21	2.007	0.083	0.516	1.489	4.890	3.991	5.490	1.509	1.509	2.214
22	2.004	0.081	0.517	1.494	4.879	4.001	5.498	1.490	1.571	2.185
23	2.001	0.072	0.511	1.493	4.858	3.991	5.488	1.509	1.522	2.214
24	2.004	0.078	0.521	1.492	4.861	3.998	5.499	1.520	1.531	1.710
25	1.992	0.084	0.522	1.485	4.897	3.991	5.487	1.525	1.522	2.015
26	2.010	0.079	0.511	1.498	4.863	3.995	5.492	1.491	1.509	2.306
27	1.997	0.075	0.534	1.487	4.881	3.997	5.471	1.594	1.564	1.883
28	2.003	0.082	0.543	1.491	4.852	4.000	5.504	1.518	1.542	1.905
29	2.008	0.073	0.555	1.489	4.901	3.993	5.506	1.493	1.495	2.423
30	2.011	0.088	0.553	1.490	4.871	3.996	5.491	1.502	1.490	2.004
Min	1.992	0.057	0.511	1.439	4.737	3.987	5.459	1.490	1.485	1.430
Max	2.051	0.108	0.561	1.501	4.901	4.010	5.560	1.594	1.571	2.749
Avg	2.006	0.079	0.536	1.480	4.860	3.995	5.492	1.515	1.516	2.038

6.3 Thermal Resistance

TEST	RTH(J-C)DC °C/W
EQUIPMENT	RTH(PHASE12)_TEST417
Condition 1	**25°C**
Condition 2	
Condition 3	DT=30us
Condition 4	IM=20mA
Condition 5	IP=20A
Condition 6	SLOPE=-539.6°C/V
Min. Datasheet	°C/W
Typ. Datasheet	1.03°C/W
Max. Datasheet	1.25°C/W
N	***8***
Min	0.97
Max	1.05
Moy.	1.011

6.4 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias / **HTFB** High Temperature Forward Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations. Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
SD Solderability	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
DBT Dead Bug Test	To evaluate the wettability of the package leads. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.
TW/WG Whiskers Growth	Forced growing of Tin Whiskers by various kind of environmental stress: temperature, moisture and temperature cycling.	To ensure no risk of electrical short due to Tin Whisker growth.
AQG 324 specific tests		
LTS Low temperature Storage	The device is stored at low temperature (-40°C)	The purpose of this test is to test or determine the effect of aging or transport at a very low temperature on the power modules. A prolonged influence of low temperatures can cause embrittlement, crack formation and fractures on parts made of rubber and plastic as well as on parts made of metal, substrate, or semiconductor material.

Test name	Description	Purpose
TST Thermal Shocks test	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	This test validates the resistance to mechanical stress from passive temperature changes. Due to a lack of acceleration factors respectively the long cycle times as a result of the test setup, it is not necessary to conduct this test until EOL.
PCmin Power Cycling in minutes	The device is submitted to cycles of current which makes heat the die by cycles. The device must see a difference of temperature of minimum: ΔTvj =100°C The current injected in the test must be >85% In. The time for heating current is >15sec.	This test is the basis for verification of the lifetime model provided by the module manufacturer for the DUTs to be examined. The tests themselves can also be used to support creating the lifetime model. The objective of this test is to generate targeted stress situations in a power electronics module under strongly accelerated conditions which lead to signs of wear-out and degradation on the module. If the time range of the key parameter value ton (on-time of the load current) is expanded to values from ton >15s, this test exerts a different stress on the power electronics modules than the test PCsec. The stress can be applied to the chip-remote interconnection (system soldering) as well as to the chip-near interconnection technology (die-attach, top-side contacting). This test thus enables pro rata simulation of the situation in the module during a cold start. The results of this test are the reliability data for the module-specific connection technology as well as the marking of the data in the numerical representation of the empirical lifetime curve Nf=f(ΔTvj, Tvj,max, ton) which must be provided by the manufacturer.
PCsec Power Cycling in secondes	The device is submitted to cycles of current which makes heat the die by cycles. The device must see a difference of temperature of minimum: ΔTvj=100°C The current injected in the test must be >85% In. The time for heating current is <5sec.	This test is the basis for verification of the lifetime model provided by the module manufacturer for the DUTs to be examined. The tests themselves can also be used to support creating the lifetime model. The objective of this test is to generate targeted stress situations in a power electronics module under strongly accelerated conditions which lead to signs of wear and degradation on the module. By limiting the key parameter ton (on-time of the load current) to a value range of ton <5s, the tests exert targeted stress on the chip-near interconnections (die-attach and top-side contacting). The results of this test are the reliability data for the module-specific, chip-near interconnection technology as well as the marking of the data in the numerical representation of the lifetime curve Nf = f(ΔTvj, Tvj,max, ton) which must be provided by the manufacturer.
MS Mechanical Shocks	Devices are submitted to mechanical shocks with acceleration of 50g and duration 6ms	This test simulates the mechanical load of the module in the PCU, e.g. when driving over curbs or during an accident. It serves to validate the resistance of the PCU to mechanical shock with failure patterns, such as cracks or device detachment.
V Vibration	The test is carried out acc. to IEC 60068-2-6 for sinusoidal vibration excitation and IEC 60068-2-64 for wide-band vibration excitation	The purpose of the test is to show the fundamental suitability of the mechanical structure for use in automotive PCUs. It simulates the vibration load of a module during driving operation and serves to validate the resistance of the module against vibrations with failure patterns, e.g. device detachment and material fatigue.

PCN
Product/Process Change Notification

Transfer of assembly and test line qualification for modules housed in ACEPACK™ SMIT package

Notification number:	ADG/23/14049	**Issue Date**	10-July-2023
Issued by	Isabelle BALLON		
Product series affected by the change		STTH60RQ06-M2Y STTN6050H-12M1Y STTD6050H-12M2Y	
Type of change		Transfer	

Description of the change

The production of ACEPACK™ SMIT package (Assembly, Test & Finishing) currently located at subcontractor in Philippines will be transferred to existing ST Shenzhen plant (China).
ST Shenzhen is already a major production site for ST products.

Reason for change

In the frame of the discontinuation of subcontractor assembly line, STMicroelectronics has initiated a transfer of ACEPACK SMIT package to ST Shenzhen plant (China).

Former versus changed product:	The changed products do not present modified electrical, dimensional, or thermal parameters, leaving unchanged the current information published in the product datasheets. The footprint recommended by ST remains the same. The Moisture Sensitivity Level of the parts (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The standard delivery quantity remains the same. The products remain in full compliance with the ST ECOPACK®2 grade (so called “halogen-free”). ACEPACK™ SMIT package from STMicroelectronics plant in China (Shenzhen) is proposed with improved Marking (ST Unit Level Traceability information), optimized Packing mode: enhanced Carrier tape design keeping unchanged external carrier dimensions.

(1) ADG: Automotive and Discrete Group

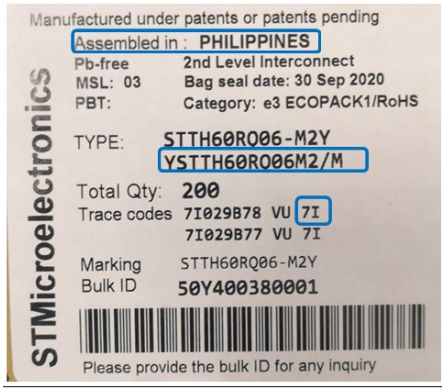
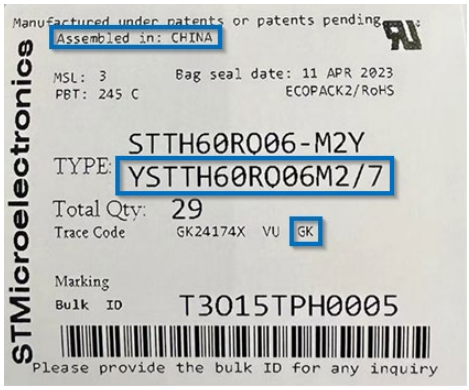
Disposition of former products

Delivery of current products will be done until stock depletion.

Marking and traceability

Traceability of the Back-End plant will be ensured by an internal codification (Finished Good/Type) and by the trace code (printed on device top & bottom sides and on the carton box label).
The first two digits of the trace code indicate the back-end plant origin.

Commercial part number/Order code	Current Finished Good/Type	New Finished Good/Type
STTH60RQ06-M2Y	YSTTH60RQ06M2/M	YSTTH60RQ06M2/7
STTN6050H-12M1Y	YSTTN6050H12M1M	YSTTN6050H12M1/7
STTD6050H-12M2Y	YSTTD6050H12M2M	YSTTD6050H-12M27

Current Label (Example)	**New Label** (Example)
Finished Good/type ending by **M**	Finished Good/type ending by **7**
	

	Current (Example)	**New** (Example)
Top view		

Bottom view		

Qualification completion date	**Week 26-2023**

Forecasted sample availability

Product family	Commercial part Number	Availability date
Rectifier	STTH60RQ06-M2Y	Week 32-2023
SCR	STTN6050H-12M1Y	Upon request
Rectifier / SCR	STTD6050H-12M2Y	Upon request

For sample(s) request, please inform FSE (Field Sales Engineer) to insert corresponding **Non-Standard Samples Order** (a single Commercial Product for each request) with **PCN reference** as additional information.

Change implementation schedule

Sales-types	Estimated production start	Estimated first shipments
STTH60RQ06-M2Y	W32-2023	W36-2023
STTN6050H-12M1Y	Q4-2023	Q4-2023
STTD6050H-12M2Y	Q4-2023	Q4-2023

Comments:	

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change.
Absence of additional response within 180 days of receipt of this PCN will constitute acceptance of the change.

Qualification program and results	23015QRP Attached

Qualification Report

Transfer qualification of ACEPACK™ SMIT package to Shenzhen plant (China)

General Information	
Product Line	*Rectifiers*
Product Description	*Automotive 600V ultrafast bridge module*
Product Perimeter	*STTH60RQ06-M2Y*
Product Group	*ADG*
Product Division	*Discrete & Filter*
Packages	*ACEPACK™ SMIT*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST Tours - France*
Assembly Plant	*ST Shenzhen - China*
Reliability Lab	*ST Tours – France*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	June 20; 2023	16	Henri VIVANT	Julien Michelon Digitally signed by Julien Michelon Date: 2023.07.07 10:54:05 +02'00'	Qualification of STTH60RQ06-M2Y

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101 Rev. E	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications
AQG 324	Qualification of Power Modules for Use in Power Electronics Converter Units in Motor Vehicles
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

DBT	Dead Bug Test
H3TRB	High Humidity High Temperature Reverse Bias
HTRB	High Temperature Reverse Bias
LTS	Low Temperature Storage
MS	Mechanical Shocks
PC	Preconditioning
PD	Physical Dimensions
PCmin	Power Cycling (minutes)
PCsec	Power Cycling (seconds)
PV	Parametric Verification
SD	Solderability test
SS	Sample Size
TST	Thermal Shocks Test
TW/WG	Tin Whiskers / Whiskers Growth
V	Vibration

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify the transfer of ACEPAK™ SMIT package to Shenzhen plant (Back End China). Qualification performed on **STTH60RQ06-M2Y** product, Automotive 600 V ultrafast bridge module embedded in ACEPACK SMIT package.

Table of involved products:

Commercial Product	Package	Comment
STTH60RQ06-M2Y	ACEPACK™ SMIT	Automotive Grade

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology » and AQG-324 guidelines. STTH60RQ06 die into the power module is already qualified AECQ101rev E in a discrete package.

The reliability tests ensuing are:

- TST to ensure the mechanical robustness of the product.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, HTS to check the robustness to corrosion and the good package hermeticity.
- Solderability and DBT to check compatibility of package with customer assembly.
- TW/WG to check lead-finishing quality.
- LTS to check the robustness to aging or transport at very low temperature.
- PC min / PC sec to evaluate the robustness of the chip near interconnections (die-attach and top-side contacting).
- V to check suitability of the mechanical structure for use in PCUs.
- MS to simulate the mechanical load of the module in PCUs.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

Based on these results, **STTH60RQ06-M2Y** is compliant with AQG-324.

4 DEVICE CHARACTERISTICS

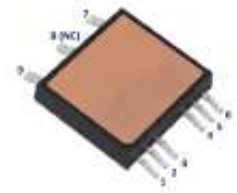
4.1 Device description

life.augmented

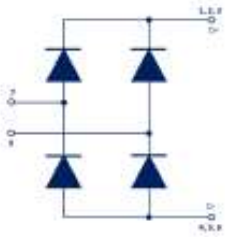
STTH60RQ06-M2Y

Datasheet

Automotive 600 V, 60 A ultrafast bridge module



ACEPACK SMIT



Features

- Operating T_J from -40 °C to +175 °C
- Ultrafast with soft recovery behaviour
- PPAP capable
- SMD with isolated top side cooling
- Low thermal resistance
- Backside in insulated ceramic
- Dice chips on Direct Bond Copper (DBC) substrate
- ECOPACK2 compliant
- MSL: Level 3
- Insulation voltage (UL 1557): V_{RMS} = 4000 V

Applications

- Output rectification
- On board charger
- Charging station

Description

The ultrafast bridge rectifier is a high-performance device, generally used in a full wave rectification of an output stage of a DC/DC converter in automotive applications.

Thanks to the high thermal capability of the ACEPACK SMIT package, this integrated module will increase the power density in the application, through very high thermal performances (top side cooling) and insulation done by an embedded ceramic. Especially suited for use in Charger applications, either integrated in the vehicle or in a charging station, this rectifier will enhance the performance of the targeted application.

Product status link
STTH60RQ06-M2Y

Device summary (per diode)	
$I_{F(AV)}$	30 A
V_{RRM}	600 V
V_F (typ.)	1.45 V
t_{rr} (max.)	30 ns
T_J	-40 °C to +175 °C

4.2 Construction Note

	STTH60RQ06-M2Y
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours- France
Technology / Process family	Automotive 600V Ultrafast bridge module
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours- France
Assembly information	
Assembly site	ST Shenzhen - China
Package description	ACEPACK™ SMIT
Molding compound	ECOPACK®2 compliant component
Lead finishing material	Lead free (pure Tin)
Final testing information	
Testing location	ST Shenzhen - China

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	STTH60RQ06-M2Y	ACEPACK™ SMIT	1st Qualification lot
L2	Dummy of setup	ACEPACK™ SMIT	Lot for whiskers test
L3	RQ Diode MAT10	ACEPACK™ SMIT	Lot for whiskers test
L4	KGFN MAT 10	ACEPACK™ SMIT	Lot for whiskers test
L5	STTH60RQ06-M2Y	ACEPACK™ SMIT	Lot for SD test

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL Not applicable for PTH and WLCSP without coating	X
MSL research	MSL	J-STD-020			Not applicable for PTH and WLCSP without coating	
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	
Parametric Verification	PV	User specification	See annex 6.1			x
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L1	6	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A			Required for Thyristor only. Alternative to HTRB	
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for Power MOSFET – IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104				
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for Power MOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for Power MOSFET – IGBT only. Alternative to TCHT	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101			Required for SCR/TRIAC RECTIFIER and Protection devices	
Autoclave	AC	JESD22A-102			Alternative to UHAST	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB (same failure mechanisms activation).	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1	6	Alternative to HAST	X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037			For power devices. Not required for Transient Voltage Suppressor (TVS) parts	
Power and Temperature Cycle	PTC	JED22A-105			For power devices. Not required for Transient Voltage Suppressor (TVS) parts	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
					Perform PTC if ΔTj>100°C cannot be achieved with IOL Alternative to IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005				
ESD Characterization	ESD CDM	AEC Q101-001 and 005				
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4			After H3TRB and TC	
Physical Dimension	PD	JESD22B-100	See annex 6.2			x
Terminal Strength	TS	MIL-STD-750 Method 2036			Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)			Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102	L5	8		X
Dead Bug Test	DBT	ST Internal specification	L1	30	Mandatory for SMD package Data collection for PTH package	X
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate			Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037			Covered during workability trials	
Bond Shear	BS	AEC-Q101-003			Covered during workability trials	
Die Shear	DS	MIL-STD-750 Method 2017			Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for Power MOSFET – IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201	L2/ L3 /L4	See test method		X
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,…)	FT	Internal specification				
Repetitive Surge	RS	Internal specification			Required for protection devices only.	
Low Temperature Storage	LTS	JESD-22 A119: 209	L1	6	AQG324 test for Modules	X
Thermal shock test	TST	JESD22-A104	L1	6	AQG324 test for Modules	X
Power Cycling (seconds)	PC sec	MIL-STD750-1 Method1037	L1	6	AQG324 test for Modules	X
Power Cycling (minutes)	PC min	MIL-STD750-1 Method1037	L1	6	AQG324 test for Modules	X
Mechanical shock	MS	IEC 600068-2-27	L1	6	AQG324 test for Modules	X
Vibration	V	IEC60068-2-6	L1	6	AQG324 test for Modules	X

5.3 Results summary

Test	PC	Std ref.	Conditions	Step / Duration	SS	Failure / SS				
						L1	L2	L3	L4	L5
Pre-and Post-Electrical Test			Ir, Vf parameters following product datasheet	-	42	0/42				
Parametric Verification			ST datasheet	Refer to paragraph 6.1 in Annexes						
PD			JESD22 B-100	Refer to paragraph 6.3 in Annexes						
V	N	IEC60068-2-6		8hrs	6	0/6				
MS	N	IEC 600068-2-27	Acceleration=50 G	6ms	6	0/6				
TST	Y	JESD22A-104	-55/+150°C 2cy/h	1Kcy	6	0/6				
				3Kcy	6	0/6				
HTRB	N	MIL-STD-750-1 M1038 Method A	Junction Temperature=175°C Temperature=170°C Voltage=480V	1Krs	6	0/6				
H3TRB	Y	JESD22A-101	85°C; 85% RH Voltage=100V	1Krs	6	0/6				
LTS	Y	JESD-22 A-119:2009	Temperature=-65°C	1Khrs	6	0/6				
HTS	Y	IEC 60749-6:2002	Junction Temperature=175°C	1Khrs	6	0/6				
PC min	Y	MIL-STD 750 Method 1037	Delta Tj=100°C Time (off)=15s Time (on)=45s	6720 cy	6	0/6				
PC sec	Y	MIL-STD 750 Method 1037	Delta Tj=100°C Time (off)=45 Time (on)=15s	6720 cy	6	0/6				
PC	Y	JESD22-A113	Humidity (HR)=60% MSL=3 Temperature)30°C	After MSL 3	6	0/6				
SD	N	J-STD-002 JESD22 B-102	Wet ageing SnPb bath 220°C	-						0/2
			Dry ageing SnPb bath 220°C							0/2
			Wet ageing SnAgCu bath 245°C							0/2
			Dry ageing SnAgCu bath 245°C							0/2
Tin Whiskers	N	AEC-Q005 JESD201	Pb free reflow TC -40°C/85°C	1500 cy		0/9 (3 lots)	0/3	0/3	0/3	
			Pb free reflow THS 55°C / RH = 85%	4000 hrs		0/9 (3 lots)	0/3	0/3	0/3	

			No reflow THS 30°C / RH = 60%	4000 hrs		0/9 (3 lots)	0/3	0/3	0/3	
			SnPb reflow TC -40°C/85°C	1500 cy		0/9 (3 lots)	0/3	0/3	0/3	
			SnPb reflow THS 55°C / RH = 85%	4000 hrs		0/9 (3 lots)	0/3	0/3	0/3	

* On 6 units all the current paths have been tested (2diodes / path)

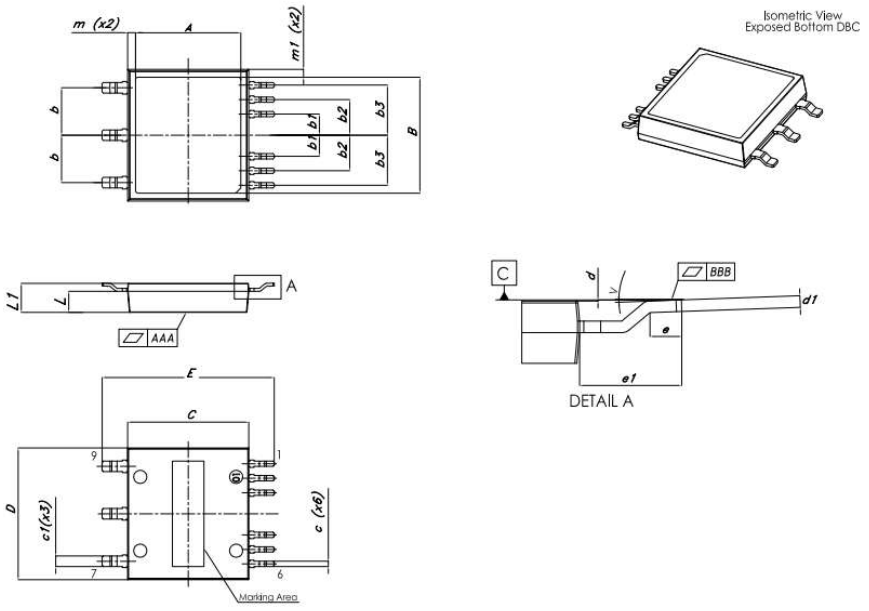
6 ANNEXES

6.1 Parametric Verification

TEST	IR (µA)	VR (V)	VF 15A (V)	VF 30A (V)	IR (µA)	VR (V)	VF 15A (V)	VF 30A (V)	IFSM (A)
EQUIPMENT	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	TESEC_881TT_TEST292	ASTEEL_2000A
Condition 1	25°C	25°C	25°C	25°C	150°C	150°C	150°C	150°C	25°C
Condition 2	VAK=600V	IAK=40uA	IAK=15A	IC=30A	VAK=600V	IAK=1mA	IAK=15A	IC=30A	TP=10ms
Condition 3	Ar=1		Ar=1	Ar=1	Ar=1	VMAX=900V	Ar=1	Ar=1	
Condition 4	TIME=100ms	Ar=1	TIME=380us	Rv=1	TIME=50ms	Ar=1	TIME=380us	Rv=1	
Condition 5		TIME=100ms		TIME=380us		TIME=20ms		TIME=380us	
Condition 6									
Min. Datasheet		600V				600V			180A
Typ. Datasheet									
Max. Datasheet	40µA		2.45V	2.95V	800uA		1.45V	1.85V	
N	24	24	24	24	24	24	24	24	6
Min	0.035	683.3	1.37	1.585	138.5	743.5	0.967	1.184	385
Max	0.080	700	1.486	1.746	176.20	761.9	1.016	1.268	420
Moy.	0.052	691.125	1.423	1.657	151.187	751.850	0.991	1.224	403

6.2 Physical Dimensions

ACEPAK™ SMIT package outline:



Dimensional Report for ACEPAK™ SMIT at Shenzhen in China:

Dimensions	Parameters									
	A	B	C	D	E	b	b1	b2	b3	c
1	19.740	21.829	23.000	24.941	32.720	8.698	3.274	5.914	8.592	1.028
2	19.888	21.848	23.031	25.002	32.778	8.660	3.304	5.904	8.593	1.035
3	19.817	21.984	23.001	24.951	32.758	8.722	3.314	5.943	8.677	1.065
4	19.929	21.880	23.017	25.003	32.790	8.710	3.386	6.042	8.709	1.041
5	19.857	21.890	23.009	24.992	32.791	8.839	3.116	5.790	8.990	1.045
6	19.811	21.871	23.078	24.934	32.775	8.687	3.097	5.804	8.510	1.037
7	19.842	21.882	23.001	24.964	32.785	8.692	3.845	5.493	8.165	1.043
8	19.877	21.812	22.997	24.963	32.797	8.742	3.828	6.424	9.120	1.030
9	19.844	21.747	23.001	24.998	32.792	8.750	3.681	6.259	8.941	1.035
10	19.875	21.754	22.995	24.938	32.779	8.774	3.817	6.408	9.088	1.039
11	19.868	21.726	23.005	24.983	32.782	8.824	3.501	6.181	8.914	1.025
12	19.856	21.825	23.152	24.983	32.778	8.785	3.668	6.271	8.923	1.043
13	20.073	21.935	23.005	25.047	32.786	8.748	3.501	6.086	8.796	1.041
14	19.893	21.765	23.001	25.027	32.773	8.769	3.844	6.472	9.233	1.057
15	19.870	21.967	23.003	24.997	32.799	8.996	3.936	6.686	9.436	1.014
16	19.813	21.818	23.002	25.049	32.779	8.995	4.112	6.860	9.615	1.018
17	19.873	21.926	22.997	24.992	32.801	9.012	3.918	6.670	9.428	1.020
18	19.987	21.863	23.082	24.980	32.796	8.994	3.781	6.534	9.282	1.019
19	19.853	21.966	22.996	24.921	32.799	8.998	3.813	6.563	9.316	1.021
20	20.006	21.844	23.004	25.018	32.803	8.998	3.851	6.603	9.358	1.034
21	19.885	21.880	22.998	25.030	32.794	9.002	4.080	6.829	9.589	1.018
22	19.814	21.859	23.085	24.954	32.790	9.003	3.949	6.697	9.452	1.045
23	19.983	21.985	23.004	25.046	32.796	9.005	3.786	6.533	9.285	1.012
24	19.878	21.865	23.022	24.958	32.776	8.998	3.863	6.625	9.379	1.011
25	19.824	21.870	23.055	24.992	32.786	9.003	3.858	6.611	9.364	1.029
26	19.966	21.860	23.008	24.972	32.787	8.994	3.815	6.567	9.308	1.019
27	19.742	21.889	23.005	25.066	32.796	8.995	3.873	6.624	9.375	1.013
28	19.859	21.827	23.002	25.016	32.791	8.998	3.773	6.623	9.270	1.029
29	19.847	21.843	23.012	24.998	32.770	8.994	4.013	6.673	9.523	1.034
30	19.860	21.869	23.013	25.001	32.780	8.999	3.952	6.703	9.442	1.023
Min	19.740	21.726	22.995	24.921	32.720	8.660	8.660	3.097	5.493	1.011
Max	20.073	21.985	23.152	25.066	32.803	9.012	9.012	4.112	6.860	1.065
Avg	19.874	21.863	23.019	24.991	32.784	8.879	8.879	3.718	6.380	1.031

Dimensions	Parameters									
	c1	d	d1	e	e1	L	L1	m	m1	V
1	2.012	0.078	0.546	1.466	4.863	3.993	5.509	1.496	1.497	1.792
2	2.009	0.098	0.549	1.464	4.883	3.996	5.491	1.518	1.498	1.914
3	2.009	0.098	0.537	1.462	4.817	4.010	5.488	1.493	1.496	1.921
4	2.001	0.108	0.541	1.472	4.870	3.993	5.509	1.528	1.485	1.832
5	1.995	0.057	0.539	1.459	4.869	3.992	5.492	1.512	1.527	1.430
6	2.006	0.080	0.521	1.439	4.872	3.996	5.497	1.526	1.491	1.747
7	2.011	0.068	0.539	1.498	4.869	3.987	5.481	1.514	1.502	1.703
8	2.017	0.069	0.545	1.451	4.872	3.995	5.486	1.509	1.549	2.148
9	1.999	0.084	0.537	1.480	4.869	3.989	5.501	1.517	1.498	1.793
10	2.002	0.069	0.561	1.472	4.882	3.995	5.478	1.505	1.495	2.069
11	1.998	0.078	0.560	1.487	4.847	3.994	5.502	1.511	1.505	2.311
12	2.005	0.080	0.551	1.481	4.855	3.992	5.497	1.497	1.494	2.504
13	2.051	0.069	0.518	1.480	4.751	3.999	5.560	1.514	1.502	1.879
14	2.005	0.082	0.526	1.501	4.737	3.992	5.478	1.542	1.519	1.438
15	2.005	0.082	0.553	1.499	4.877	3.997	5.485	1.506	1.550	2.060
16	2.018	0.074	0.548	1.468	4.860	3.995	5.472	1.512	1.513	2.383
17	2.003	0.086	0.547	1.469	4.879	3.990	5.459	1.584	1.541	2.545
18	1.997	0.073	0.534	1.466	4.882	3.998	5.477	1.517	1.505	2.749
19	1.994	0.086	0.539	1.496	4.851	3.992	5.483	1.498	1.510	2.167
20	1.997	0.069	0.518	1.486	4.845	3.993	5.495	1.501	1.551	1.890
21	2.007	0.083	0.516	1.489	4.890	3.991	5.490	1.509	1.509	2.214
22	2.004	0.081	0.517	1.494	4.879	4.001	5.498	1.490	1.571	2.185
23	2.001	0.072	0.511	1.493	4.858	3.991	5.488	1.509	1.522	2.214
24	2.004	0.078	0.521	1.492	4.861	3.998	5.499	1.520	1.531	1.710
25	1.992	0.084	0.522	1.485	4.897	3.991	5.487	1.525	1.522	2.015
26	2.010	0.079	0.511	1.498	4.863	3.995	5.492	1.491	1.509	2.306
27	1.997	0.075	0.534	1.487	4.881	3.997	5.471	1.594	1.564	1.883
28	2.003	0.082	0.543	1.491	4.852	4.000	5.504	1.518	1.542	1.905
29	2.008	0.073	0.555	1.489	4.901	3.993	5.506	1.493	1.495	2.423
30	2.011	0.088	0.553	1.490	4.871	3.996	5.491	1.502	1.490	2.004
Min	1.992	0.057	0.511	1.439	4.737	3.987	5.459	1.490	1.485	1.430
Max	2.051	0.108	0.561	1.501	4.901	4.010	5.560	1.594	1.571	2.749
Avg	2.006	0.079	0.536	1.480	4.860	3.995	5.492	1.515	1.516	2.038

6.3 Thermal Resistance

TEST	RTH(J-C)DC °C/W
EQUIPMENT	RTH(PHASE12)_TEST417
Condition 1	25°C
Condition 2	
Condition 3	DT=30us
Condition 4	IM=20mA
Condition 5	IP=20A
Condition 6	SLOPE=-539.6°C/V
Min. Datasheet	°C/W
Typ. Datasheet	1.03°C/W
Max. Datasheet	1.25°C/W
N	8
Min	0.97
Max	1.05
Moy.	1.011

6.4 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias / **HTFB** High Temperature Forward Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations. Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
SD Solderability	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
DBT Dead Bug Test	To evaluate the wettability of the package leads. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.
TW/WG Whiskers Growth	Forced growing of Tin Whiskers by various kind of environmental stress: temperature, moisture and temperature cycling.	To ensure no risk of electrical short due to Tin Whisker growth.
AQG 324 specific tests		
LTS Low temperature Storage	The device is stored at low temperature (-40°C)	The purpose of this test is to test or determine the effect of aging or transport at a very low temperature on the power modules. A prolonged influence of low temperatures can cause embrittlement, crack formation and fractures on parts made of rubber and plastic as well as on parts made of metal, substrate, or semiconductor material.

Test name	Description	Purpose
TST Thermal Shocks test	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	This test validates the resistance to mechanical stress from passive temperature changes. Due to a lack of acceleration factors respectively the long cycle times as a result of the test setup, it is not necessary to conduct this test until EOL.
PCmin Power Cycling in minutes	The device is submitted to cycles of current which makes heat the die by cycles. The device must see a difference of temperature of minimum: ΔTvj =100°C The current injected in the test must be >85% In. The time for heating current is >15sec.	This test is the basis for verification of the lifetime model provided by the module manufacturer for the DUTs to be examined. The tests themselves can also be used to support creating the lifetime model. The objective of this test is to generate targeted stress situations in a power electronics module under strongly accelerated conditions which lead to signs of wear-out and degradation on the module. If the time range of the key parameter value ton (on-time of the load current) is expanded to values from ton >15s, this test exerts a different stress on the power electronics modules than the test PCsec. The stress can be applied to the chip-remote interconnection (system soldering) as well as to the chip-near interconnection technology (die-attach, top-side contacting). This test thus enables pro rata simulation of the situation in the module during a cold start. The results of this test are the reliability data for the module-specific connection technology as well as the marking of the data in the numerical representation of the empirical lifetime curve Nf=f(ΔTvj, Tvj,max, ton) which must be provided by the manufacturer.
PCsec Power Cycling in secondes	The device is submitted to cycles of current which makes heat the die by cycles. The device must see a difference of temperature of minimum: ΔTvj=100°C The current injected in the test must be >85% In. The time for heating current is <5sec.	This test is the basis for verification of the lifetime model provided by the module manufacturer for the DUTs to be examined. The tests themselves can also be used to support creating the lifetime model. The objective of this test is to generate targeted stress situations in a power electronics module under strongly accelerated conditions which lead to signs of wear and degradation on the module. By limiting the key parameter ton (on-time of the load current) to a value range of ton <5s, the tests exert targeted stress on the chip-near interconnections (die-attach and top-side contacting). The results of this test are the reliability data for the module-specific, chip-near interconnection technology as well as the marking of the data in the numerical representation of the lifetime curve Nf = f(ΔTvj, Tvj,max, ton) which must be provided by the manufacturer.
MS Mechanical Shocks	Devices are submitted to mechanical shocks with acceleration of 50g and duration 6ms	This test simulates the mechanical load of the module in the PCU, e.g. when driving over curbs or during an accident. It serves to validate the resistance of the PCU to mechanical shock with failure patterns, such as cracks or device detachment.
V Vibration	The test is carried out acc. to IEC 60068-2-6 for sinusoidal vibration excitation and IEC 60068-2-64 for wide-band vibration excitation	The purpose of the test is to show the fundamental suitability of the mechanical structure for use in automotive PCUs. It simulates the vibration load of a module during driving operation and serves to validate the resistance of the module against vibrations with failure patterns, e.g. device detachment and material fatigue.

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Transfer of assembly and test line qualification for modules housed in ACEPACKSMIT package

PCN Reference : ADG/23/14049

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STTN6050H-12M1Y	STTD6050H-12M2Y	STTH60RQ06-M2Y

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