

## PRODUCT / PROCESS CHANGE NOTIFICATION

### 1. PCN basic data

1.1 Company	 STMicroelectronics International N.V
1.2 PCN No.	ADG/23/13931
1.3 Title of PCN	Qualification of new assembly line for SMB Flat 3 leads wire package at ST Bouskoura in Morocco
1.4 Product Category	TS110-7UF TS110-8SUF TS110-8UF X0115MUF X0202NUF Z0103MUF Z0107MUF Z0109MUF TS110-7UF TS110-8SUF TS110-8UF
1.5 Issue date	2023-03-16

### 2. PCN Team

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2.2 Change responsibility	
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2.1.2 Marketing Manager	Philippe LEGER
2.1.3 Quality Manager	Jean-Paul REBRASSE

### 3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Machines	(Not Defined)	ST Bouskoura in Morocco

### 4. Description of change

	Old	New
4.1 Description	Assembly line in ST Bouskoura (Morocco)	New assembly line for SMB Flat 2 leads wire at same Back-End plant (ST Bouskoura) in Morocco. With this new line, the manufacturing process will be enhanced with conversion to Pb-free based Die-attach material and with package outline optimization.
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No	

### 5. Reason / motivation for change

5.1 Motivation	With this additional line investment, STMicroelectronics will increase its production capacity to better serve its customers through service improvement and lead time reduction. To ease report on boards at customers side, ST is proposing package outline optimization with notch on package back side.
5.2 Customer Benefit	CAPACITY INCREASE

### 6. Marking of parts / traceability of change

6.1 Description	Traceability of the change will be ensured by Finished Good/Type print on carton labels.
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### 7. Timing / schedule

7.1 Date of qualification results	2023-03-07
7.2 Intended start of delivery	2023-06-30

<b>7.3 Qualification sample available?</b>	Upon Request
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<b>8. Qualification / Validation</b>			
<b>8.1 Description</b>	13931 23006QRP Rev1.pdf		
<b>8.2 Qualification report and qualification results</b>	Available (see attachment)	<b>Issue Date</b>	2023-03-16

<b>9. Attachments (additional documentations)</b>			
13931 Public product.pdf 13931 SMB Flat 3L wire in BSK.pdf 13931 23006QRP Rev1.pdf			

<b>10. Affected parts</b>			
<b>10.1 Current</b>		<b>10.2 New (if applicable)</b>	
<b>10.1.1 Customer Part No</b>	<b>10.1.2 Supplier Part No</b>	<b>10.1.2 Supplier Part No</b>	
	TS110-7UF		
	TS110-8UF		
	X0115MUF		
	X0202NUF		
	Z0103MUF		
	Z0107MUF		
	Z0109MUF		

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# Qualification Report

## Qualification of new assembly line SMB Flat 3 leads wire package at ST Bouskoura

General Information		Locations	
<b>Product Line</b>	<i>Triac – ASD Thyristor - Thyristor</i>	<b>Wafer Fab</b>	<i>ST TOURS - FRANCE</i>
<b>Product Description</b>	<i>High surge voltage 1.25A SCR for circuit breaker (TS110-7UF – TS110-8UF- TS110-8SUF)    1.25A sensitive gate SCR (X0202NUF)    1A sensitive gate SCR thyristor (X0115MUF)    Standard 1A Triacs (Z0103MUF- Z0107MUF-Z0109MUF)</i>	<b>Assembly Plant</b>	<i>ST BOUSKOURA - MOROCCO</i>
<b>Product Perimeter</b>	<i>TS110-7UF    TS110-8SUF    TS110-8UF    X0115MUF    X0202NUF    Z0103MUF    Z0107MUF    Z0109MUF</i>	<b>Reliability Lab</b>	<i>ST TOURS – FRANCE</i>
<b>Product Group</b>	<i>ADG</i>	<b>Reliability Assessment</b>	<i>Solderability test done at ST SHENZHEN -CHINA</i>
<b>Product Division</b>	<i>Discrete &amp; Filter</i>		
<b>Packages</b>	<i>SMB flat 3L</i>		
<b>Maturity level step</b>	<i>QUALIFIED</i>		<b>PASS</b>

### DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	01-Mar-2023	14	Elisabeth PREVOST		Initial release. Linked to PCN ADG/23/13931

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.

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## 1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
<b>JESD 47</b>	Stress-Test-Driven Qualification of Integrated Circuits
<b>JESD 94</b>	Application specific qualification using knowledge based test methodology
<b>JESD 22</b>	Reliability test methods for packaged devices
<b>MIL-STD-750C</b>	Test method for semiconductor devices

## 2 GLOSSARY

<b>ACBV</b>	Alternative Current Blocking Voltage
<b>DBT</b>	Dead Bug Test
<b>EV</b>	External Visual
<b>GD</b>	Generic Data
<b>H3TRB</b>	High Humidity High Temperature Reverse Bias
<b>MSL</b>	Moisture Sensitivity Level
<b>PC</b>	Preconditioning
<b>PD</b>	Physical Dimensions
<b>RSH</b>	Resistance to Soldering Heat
<b>SD</b>	Solderability test
<b>SS</b>	Sample Size
<b>TC</b>	Temperature Cycling
<b>UHAST</b>	Unbiased Highly Accelerated Stress Test

### **3 RELIABILITY EVALUATION OVERVIEW**

#### **3.1 Objectives**

The objective of this report is to qualify a new assembly line for Triacs and SCR Thyristors housed in SMB Flat 3 Leads package (wire) in ST BOUSKOURA (MORROCO).

The involved products are listed in the table here below:

Product	Description	Package	Assembly Location		
TS110-7UF	ASD Thyristor	SMB Flat 3L	ST BOUSKOURA - MORROCO		
TS110-8SUF					
TS110-8UF					
X0115MUF	Thyristor				
X0202NUF					
Z0103MUF	Triacs				
Z0107MUF					
Z0109MUF					

Item	Before	After
ADG/23/13931	No change	STMicroelectronics will increase its production capacity to better serve its customers through service improvement and lead time reduction.  With this new line, the manufacturing process will be enhanced with conversion to Pb-free based Die-attach material and with package outline optimization.

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology. »

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.
- RSH, Solderability and DBT to check compatibility of package with customer assembly.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

#### **3.2 Conclusion**

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

## 4 DEVICE CHARACTERISTICS

### 4.1 Construction Note

Z01xxMUF	
<b>Wafer/Die fab. information</b>	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	TRIACS
<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	ST TOURS - FRANCE
<b>Assembly information</b>	
Assembly site	ST BOUSKOURA - MORROCO
Package description	SMB FLAT 3L
Molding compound	ECOPACK®3
Lead finishing material	Lead free (pure Tin)
<b>Final testing information</b>	
Testing location	ST BOUSKOURA - MORROCO

TS110-xUF – X0115MUF – X020NUF	
<b>Wafer/Die fab. information</b>	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	SCR Thyristors
<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	ST TOURS - FRANCE
<b>Assembly information</b>	
Assembly site	ST BOUSKOURA - MORROCO
Package description	SMB FLAT 3L
Molding compound	ECOPACK®3
Lead finishing material	Lead free (pure Tin)
<b>Final testing information</b>	
Testing location	ST BOUSKOURA - MORROCO

## 5 TESTS PLAN AND RESULTS SUMMARY

### 5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	Z0109MUF	SMB Flat 3L	Qualification lot 1
L2	Z0109MUF		Qualification lot 2
L3	TS110-8SUF		Qualification lot 3
L4	TS110-8SUF		Qualification lot 4

Detailed results in below chapter will refer to these references.

## 5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL Not applicable for PTH and WLCSP without coating	X
MSL research	MSL	J-STD-020	L1	30	Not applicable for PTH and WLCSP without coating	X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L1 L2	110		X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L2, L3, L4	231 (3*77)	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A	-	-	Required for Thyristor only. Alternative to HTRB	-
High Temperature Forward Bias	HTFB	JESD22 A-108	-	-	Not required, applicable only to LEDs Alternative to HTRB	-
High Temperature Operating Life	HTOL		-	-	Covered by HTRB or ACBV	-
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B	-	-	Required for Voltage Regulator (Zener) only.	-
High Temperature Gate Bias	HTGB	JESD 22A-108	-	-	Required for Power MOSFET – IGBT only.	-
High Temperature Storage Life	HTSL	JESD22 A-103	-	-	Covered by HTRB	-
Temperature Humidity Storage	THS	JESD22 A-118	-	-	Covered by H3TRB	-
Temperature Cycling	TC	JESD22A-104	L1, L2, L3, L4	308 (4*77)		X
Temperature Cycling Hot Test	TCHT	JESD22A-104	-	-	Required for Power MOSFET – IGBT only.	-
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035	-	-	Required for Power MOSFET – IGBT only. Alternative to TCHT	-
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037	-	-	For dissimilar metal bonding systems only	-
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101	L2	77	Required for SCR/TRIAC RECTIFIER and Protection devices	X
Autoclave	AC	JESD22A-102	-	-	Alternative to UHAST	-
Highly Accelerated Stress Test	HAST	JESD22A-110	-	-	Covered by H3TRB (same failure mechanisms activation).	-
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L2	77	Alternative to HAST	X
High Temperature High Humidity Bias	HTHBB	JED22A-101	-	-	Not required, LED only	-
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	-	-	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	-

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Power and Temperature Cycle	PTC	JED22A-105	-	-	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if $\Delta T_j > 100^\circ\text{C}$ cannot be achieved with IOL Alternative to IOL	-
ESD Characterization	ESD HBM	AEC Q101-001 and 005	-	-		-
ESD Characterization	ESD CDM	AEC Q101-001 and 005	-	-		-
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	-	-	After H3TRB and TC	-
Physical Dimension	PD	JESD22B-100	-	60 (2*30)		X
Terminal Strength	TS	MIL-STD-750 Method 2036	-	-	Required for leaded parts only	-
Resistance to Solvents	RTS	JESD22B-107	-	--	Not applicable for Laser Marking	-
Constant Acceleration	CA	MIL-STD-750 Method 2006	-	-	Required for hermetic packaged parts only.	-
Vibration Variable Frequency	VVF	JESD22B-103	-	-	Required for hermetic packaged parts only.	-
Mechanical Shock	MS	JESD22 B-104	-	-	Required for hermetic packaged parts only.	-
Hermeticity	HER	JESD22A-109	-	-	Required for hermetic packaged parts only.	-
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	L1, L2, L3	90 (3*30)	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	X
Solderability	SD	J-STD-002 JESD22B102	L2	60 (4*15)		X
Dead Bug Test	DBT	ST Internal specification	L2	30	Mandatory for SMD package Data collection for PTH package	X
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	-	-	Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	-
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	-	-	Covered during workability trials	-
Bond Shear	BS	AEC-Q101-003	-	-	Covered during workability trials	-
Die Shear	DS	MIL-STD-750 Method 2017	-	-	Not Applicable to parts with solder paste die attach	-
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2	-	-	Required for Power MOS and internally clamped IGBTs only	--
Dielectric Integrity	DI	AEC-Q101-004 section 3	-	-	Required for Power MOSFET – IGBT only.	-
Short Circuit Reliability Characterization	SCR	AEC-Q101-006	-	-	Required for smart power parts only	-
Whisker Growth Evaluation	WG	AEC-Q005 JESD201	-	-		-
Early Life Failure Rate	ELFR	JESD74	-	-	Recommended for new techno development in case of identified failure mechanism	-
Functional Test (in rush, di/dt...)	FT	Internal specification	-	-		-
Repetitive Surge	RS	Internal specification	-	-	Required for protection devices only.	-

Low Temperature Storage	LTS	JESD-22 A119: 209	--	-	AQG324 test for Modules	-
Thermal shock test	TST	JESD22-A104	-	--	AQG324 test for Modules	-
Power Cycling (seconds)	PC sec	MIL-STD750-1 Method1037	--	-	AQG324 test for Modules	-
Power Cycling (minutes)	PC min	MIL-STD750-1 Method1037	-	-	AQG324 test for Modules	-

Mechanical shock	MS	IEC 60068-2-27	-	-	AQG324 test for Modules	-
Vibration	V	IEC60068-2-6	-	-	AQG324 test for Modules	-

### 5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS			
						L1	L2	L3	L4
PC	-	JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	-	522	0/522			
Parametric Verification	-	ST datasheet	Over part temperature range (note 1)	-	110	Refer to paragraph 6.1 in Annexes			
Physical Dimension	-	JESD22B-100	-	-	60	Refer to paragraph 6.2 in Annexes			
External Visual inspection	-	JESD22B-101	All qualification parts submitted for testing passed External & Visual inspection. during manufacturing process						
MS1	-	JESD22-A113	MSL=1, Reflow=3 Temperature=85°C Humidity (HR)=85%	168Hrs	30	0/30	-	-	-
HTRB	-	MIL-STD-750-1 M1038 Method A	Junction Temperature=125°C Voltage=800V	1Khrs	154	-	-	0/77	0/77
			Junction Temperature=125°C Voltage=600V		77	-	0/77	-	-
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	1Kcy	308	0/77	0/77	0/77	0/77
RSH	-	JESD22 A-111	Temperature=260°C Time (on)=10s	-	90	0/30	0/30	0/30	-
H3TRB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Voltage=100V	1Khrs	77	-	0/77	-	-
UHAST	Y	JESD22 A-118	130°C; 85% RH 2.3bar	96hrs	77	-	0/77	-	-
SD	-	J-STD-002 JESD22 B-102	Wet ageing SnPb bath 220°C	-	15	-	0/15	-	-
			Dry ageing SnPb bath 220°C		15	-	0/15	-	-
			Wet ageing SnAgCu bath 245°C		15	-	0/15	-	-
			Dry ageing SnAgCu bath 245°C		15	-	0/15	-	-
DBT	-	DM00112629 (ST internal)	IR reflow after flux deposition	-	30	-	0/30	-	-

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.

Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers."

## 6 ANNEXES

### 6.1 Parametric Verification

#### Result on product of Z0109MUF

TEST	IDRM	IDRM	IRRM	IRRM	VTM	VTM
Condition 1	25°C	25°C	125°C	125°C	25°C	25°C
Condition 2	VDRM=600V	VDRM=600V	VDRM=600V	VDRM=600V	ITM=1,4A	ITM=1,4A
Condition 3	Direct	Reverse	Direct	Reverse	Direct	Reverse
Min. Datasheet						
Max. Datasheet	5	5	0,5	0,5	1,6	1,6
UNIT	uA	uA	mA	mA	V	V
N	40	40	10	10	40	40
Min	0,057	0,099	0,00789	0,01665	1,245	1,250
Max	0,263	0,326	0,00955	0,02345	1,305	1,302
Moy.	0,125	0,247	0,00858	0,01950	1,259	1,264

TEST	IGT Q1	IGT Q2	IGT Q3	IGT Q4	VGT Q1	VGT Q2	VGT Q3	VGT Q4
Condition 1	25°C							
Condition 2	VD=12V							
Condition 3	RL=30ohms							
Min. Datasheet								
Max. Datasheet	10	10	10	10	1,3	1,3	1,3	1,3
UNIT	mA	mA	mA	mA	V	V	V	V
N	40	40	40	40	40	40	40	40
Min	1	2,4	2,7	5,799	0,673	0,695	0,737	0,843
Max	1,099	2,799	3,1	7,299	0,691	0,707	0,752	0,881
Moy.	1,077	2,704	2,887	6,284	0,682	0,702	0,744	0,851

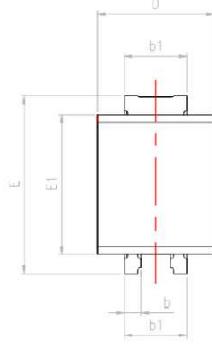
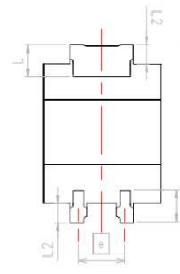
TEST	IH	IH	IL Q1	IL Q2	IL Q3	IL Q4
Condition 1	25°C	25°C	25°C	25°C	25°C	25°C
Condition 2	IT=50mA	IT=50mA	IG=12mA	IG=12mA	IG=12mA	IG=12mA
Condition 3	IG=15mA	IG=15mA				
Min. Datasheet	Direct	Reverse				
Max. Datasheet	10	10	15	25	15	15
UNIT	mA	mA	mA	mA	mA	mA
N	40	40	40	40	40	40
Min	1,480	1,860	2,938	13,360	2,400	4,618
Max	1,780	2,060	3,387	13,650	2,625	5,214
Moy.	1,657	1,990	3,209	13,547	2,529	4,826

## Result on product of TS110-8SUF

TEST	IDRM	IDRM	IRRM	IRRM
Condition 1	25°C	125°C	25°C	125°C
Condition 2	VDRM=800V	VDRM=800V	VDRM=800V	VDRM=800V
Condition 3	RGK=220Ohms	RGK=220Ohms	RGK=220Ohms	RGK=220Ohms
Min. Datasheet	Direct	Reverse	Direct	Reverse
Typ. Datasheet				
Max. Datasheet	1	100	1	100
UNIT	uA	mA	uA	mA
N	50	10	50	10
Min	9,345	0,307	0,000	1,629
Max	198,000	0,771	238,900	2,733
Moy.	61,884	0,528	111,019	2,093

TEST	VGT	IGT	IH	IL Q1	VTM
Condition 1	25°C	25°C	25°C	25°C	25°C
Condition 2	VD=12V	VD=12V	IT=50mA	IG=5mA	ITM=2,5A
Condition 3	RL=140ohms	RL=140ohms	RGK=220Ohms	RGK=220Ohms	
Min. Datasheet					
Typ. Datasheet		1			
Max. Datasheet	0,8	100	12	12	1,6
UNIT	V	uA	mA	mA	V
N	50	50	50	50	50
Min	0,593	6,910	5,860	6,132	1,396
Max	0,606	17,100	6,820	7,157	1,437
Moy.	0,601	11,986	6,383	6,718	1,419

## 6.2 Physical Dimensions

New SMB Flat Package																																																																																																																																															
Package outline						Dimensions values																																																																																																																																									
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## 6.3 Tests description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTRB</b> High Temperature Reverse Bias / <b>HTFB</b> High Temperature Forward Bias	<p>The device is stressed in static configuration, trying to satisfy as much as possible the following conditions:</p> <ul style="list-style-type: none"> <li>- Low power dissipation</li> <li>- Max. supply voltage compatible with diffusion process and internal circuitry limitations.</li> </ul> <p>Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature</p>	<p>To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way.</p> <p>To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.</p> <p>To assess active area and contacts integrity</p>
<b>Package Oriented</b>		
<b>PC</b> Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	<p>As stand-alone test: to investigate the moisture sensitivity level.</p> <p>As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.</p>
<b>H3TRB</b> High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
<b>TC</b> Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>UHAST</b> Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>RSH</b> Resistance to Solder Heat	Package is dipped by the leads in a solder bath after initial wet ageing (for SMDs only). Assessment by electrical test + no external crack	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
<b>SD</b> Solderability	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
<b>DBT</b> Dead Bug Test	To evaluate the wettability of the package leads. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.
<b>Functional Tests</b>		

## Public Products List

Public Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

**PCN Title :** Qualification of new assembly line for SMB Flat 3 leads wire package at ST Bouskoura in Morocco

**PCN Reference :** ADG/23/13931

**Subject :** Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

Z0109MUF	TS110-7UF	X0202NUF
Z0107MUF	X0115MUF	TS110-8UF
Z0103MUF		

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(<sup>1</sup>) ADG: Automotive and Discrete Group

## **PCN**

### **Product/Process Change Notification**

#### **Qualification of new assembly line for SMB Flat 3 leads wire package at ST Bouskoura in Morocco**

<b>Notification number:</b>	ADG/23/13931	<b>Issue Date</b>	14-MAR-2023
<b>Issued by</b>	Sophie DA SILVA		
<b>Product series affected by the change</b>	TS110-7UF TS110-8SUF TS110-8UF X0115MUF X0202NUF Z0103MUF Z0107MUF Z0109MUF		
<b>Type of change</b>	Back-End realization		

#### **Description of the change**

STMicroelectronics is qualifying the transfer of SMB Flat 3 leads wire production activity to a new assembly line at same Back-End plant (ST Bouskoura) in Morocco.

With this new line, the manufacturing process will be enhanced with conversion to Pb-free based Die-attach material and with package outline optimization.

#### **Reason for change**

With this additional line investment, STMicroelectronics will increase its production capacity to better serve its customers through service improvement and lead time reduction.

To ease report on boards at customers side, ST is proposing package outline optimization with notch on package back side.

<b>Former versus changed product:</b>	<p>The changed products do not present modified electrical or thermal parameters, leaving unchanged the current information published in the product datasheet.</p> <p>Package outline modification with notch on package back side, keeping unchanged recommended footprint.</p> <p>All products (Former and New) are compliant to a common Package outline.</p> <p>The Moisture Sensitivity Level of the part (according to the</p>
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(<sup>1</sup>) ADG: Automotive and Discrete Group

	<p>IPC/JEDEC JSTD-020D standard) remains unchanged. There is no change in the packing modes and the standard delivery quantities either.</p> <p>TS110-xx products are now proposed as ECOPACK®2 (so called “halogen-free”) or ECOPACK®3 grade (Lead-free and Green Molding Compound). Other products remain ECOPACK®2 (so called “halogen-free”).</p>
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#### Disposition of former products

Units manufactured on former line will be delivered till stock depletion.

#### Marking and traceability

Traceability of the change will be ensured by Finished Good/Type print on carton labels.

Commercial part number Order code	Former Finished Good/Type	New Finished Good/Type
TS110-7UF	TS1107UF/Z	TS1107UF/ZH
TS110-8SUF	TS1108SUF/Z	TS1108SUF/ZH
TS110-8UF	TS1108UF/Z	TS1108UF/ZH
X0115MUF	X0115MUF\Z	X0115MUF\ZS
X0202NUF	X0202NUF\Z	X0202NUF\ZS
Z0103MUF	Z0103MUF\Z	Z0103MUF\ZS
Z0107MUF	Z0107MUF\Z	Z0107MUF\ZS
Z0109MUF	Z0109MUF\Z	Z0109MUF\ZS

#### Qualification completion date

Week 10-2023

#### Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
THYRISTOR	ASD THYRISTOR	TS110-7UF	Week 12-2023
THYRISTOR	ASD THYRISTOR	TS110-8SUF	Week 12-2023
THYRISTOR	ASD THYRISTOR	TS110-8UF	Week 12-2023
THYRISTOR	THYRISTOR	X0115MUF	Week 12-2023
THYRISTOR	THYRISTOR	X0202NUF	Week 12-2023
THYRISTOR	TRIAC	Z0103MUF	Week 12-2023
THYRISTOR	TRIAC	Z0107MUF	Week 12-2023
THYRISTOR	TRIAC	Z0109MUF	Week 12-2023

For sample(s) request, please inform FSE (Field Sales Engineer) in order to insert corresponding **Non-Standard Samples Order** (a single Commercial Product for each request) with **PCN reference** as additional information.

(<sup>1</sup>) ADG: Automotive and Discrete Group

**Change implementation schedule**

Sales-types	Estimated production start	Estimated first shipments
All	Apr-2023	Jun -2023

**Comments:** With early PCN acceptance, possible shipment starting W18-2023.

**Customer's feedback**

Please contact your local ST sales representative or quality contact for requests concerning this change notification.  
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change.  
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change.

**Qualification program** 23006QRP Attached

# Qualification Report

## Qualification of new assembly line SMB Flat 3 leads wire package at ST Bouskoura

General Information		Locations	
<b>Product Line</b>	<i>Triac – ASD Thyristor - Thyristor</i>	<b>Wafer Fab</b>	<i>ST TOURS - FRANCE</i>
<b>Product Description</b>	<i>High surge voltage 1.25A SCR for circuit breaker (TS110-7UF – TS110-8UF- TS110-8SUF) 1.25A sensitive gate SCR (X0202NUF) 1A sensitive gate SCR thyristor (X0115MUF) Standard 1A Triacs (Z0103MUF- Z0107MUF-Z0109MUF)</i>	<b>Assembly Plant</b>	<i>ST BOUSKOURA - MOROCCO</i>
<b>Product Perimeter</b>	<i>TS110-7UF TS110-8SUF TS110-8UF X0115MUF X0202NUF Z0103MUF Z0107MUF Z0109MUF</i>	<b>Reliability Lab</b>	<i>ST TOURS – FRANCE</i>
<b>Product Group</b>	<i>ADG</i>	<b>Reliability Assessment</b>	<i>Solderability test done at ST SHENZHEN -CHINA</i>
<b>Product Division</b>	<i>Discrete &amp; Filter</i>		
<b>Packages</b>	<i>SMB flat 3L</i>		
<b>Maturity level step</b>	<i>QUALIFIED</i>		<b>PASS</b>

### DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	01-Mar-2023	14	Elisabeth PREVOST		Initial release. Linked to PCN ADG/23/13931

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.

This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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## 1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
<b>JESD 47</b>	Stress-Test-Driven Qualification of Integrated Circuits
<b>JESD 94</b>	Application specific qualification using knowledge based test methodology
<b>JESD 22</b>	Reliability test methods for packaged devices
<b>MIL-STD-750C</b>	Test method for semiconductor devices

## 2 GLOSSARY

<b>ACBV</b>	Alternative Current Blocking Voltage
<b>DBT</b>	Dead Bug Test
<b>EV</b>	External Visual
<b>GD</b>	Generic Data
<b>H3TRB</b>	High Humidity High Temperature Reverse Bias
<b>MSL</b>	Moisture Sensitivity Level
<b>PC</b>	Preconditioning
<b>PD</b>	Physical Dimensions
<b>RSH</b>	Resistance to Soldering Heat
<b>SD</b>	Solderability test
<b>SS</b>	Sample Size
<b>TC</b>	Temperature Cycling
<b>UHAST</b>	Unbiased Highly Accelerated Stress Test

### **3 RELIABILITY EVALUATION OVERVIEW**

#### **3.1 Objectives**

The objective of this report is to qualify a new assembly line for Triacs and SCR Thyristors housed in SMB Flat 3 Leads package (wire) in ST BOUSKOURA (MORROCO).

The involved products are listed in the table here below:

Product	Description	Package	Assembly Location		
TS110-7UF	ASD Thyristor	SMB Flat 3L	ST BOUSKOURA - MORROCO		
TS110-8SUF					
TS110-8UF					
X0115MUF	Thyristor				
X0202NUF					
Z0103MUF	Triacs				
Z0107MUF					
Z0109MUF					

Item	Before	After
ADG/23/13931	No change	STMicroelectronics will increase its production capacity to better serve its customers through service improvement and lead time reduction.  With this new line, the manufacturing process will be enhanced with conversion to Pb-free based Die-attach material and with package outline optimization.

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology. »

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.
- RSH, Solderability and DBT to check compatibility of package with customer assembly.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

#### **3.2 Conclusion**

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

## 4 DEVICE CHARACTERISTICS

### 4.1 Construction Note

Z01xxMUF	
<b>Wafer/Die fab. information</b>	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	TRIACS
<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	ST TOURS - FRANCE
<b>Assembly information</b>	
Assembly site	ST BOUSKOURA - MORROCO
Package description	SMB FLAT 3L
Molding compound	ECOPACK®3
Lead finishing material	Lead free (pure Tin)
<b>Final testing information</b>	
Testing location	ST BOUSKOURA - MORROCO

TS110-xUF – X0115MUF – X020NUF	
<b>Wafer/Die fab. information</b>	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	SCR Thyristors
<b>Wafer Testing (EWS) information</b>	
Electrical testing manufacturing location	ST TOURS - FRANCE
<b>Assembly information</b>	
Assembly site	ST BOUSKOURA - MORROCO
Package description	SMB FLAT 3L
Molding compound	ECOPACK®3
Lead finishing material	Lead free (pure Tin)
<b>Final testing information</b>	
Testing location	ST BOUSKOURA - MORROCO

## 5 TESTS PLAN AND RESULTS SUMMARY

### 5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	Z0109MUF	SMB Flat 3L	Qualification lot 1
L2	Z0109MUF		Qualification lot 2
L3	TS110-8SUF		Qualification lot 3
L4	TS110-8SUF		Qualification lot 4

Detailed results in below chapter will refer to these references.

## 5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL Not applicable for PTH and WLCSP without coating	X
MSL research	MSL	J-STD-020	L1	30	Not applicable for PTH and WLCSP without coating	X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L1 L2	110		X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L2, L3, L4	231 (3*77)	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A	-	-	Required for Thyristor only. Alternative to HTRB	-
High Temperature Forward Bias	HTFB	JESD22 A-108	-	-	Not required, applicable only to LEDs Alternative to HTRB	-
High Temperature Operating Life	HTOL		-	-	Covered by HTRB or ACBV	-
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B	-	-	Required for Voltage Regulator (Zener) only.	-
High Temperature Gate Bias	HTGB	JESD 22A-108	-	-	Required for Power MOSFET – IGBT only.	-
High Temperature Storage Life	HTSL	JESD22 A-103	-	-	Covered by HTRB	-
Temperature Humidity Storage	THS	JESD22 A-118	-	-	Covered by H3TRB	-
Temperature Cycling	TC	JESD22A-104	L1, L2, L3, L4	308 (4*77)		X
Temperature Cycling Hot Test	TCHT	JESD22A-104	-	-	Required for Power MOSFET – IGBT only.	-
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035	-	-	Required for Power MOSFET – IGBT only. Alternative to TCHT	-
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037	-	-	For dissimilar metal bonding systems only	-
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101	L2	77	Required for SCR/TRIAC RECTIFIER and Protection devices	X
Autoclave	AC	JESD22A-102	-	-	Alternative to UHAST	-
Highly Accelerated Stress Test	HAST	JESD22A-110	-	-	Covered by H3TRB (same failure mechanisms activation).	-
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L2	77	Alternative to HAST	X
High Temperature High Humidity Bias	HTHBB	JED22A-101	-	-	Not required, LED only	-
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	-	-	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	-

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Power and Temperature Cycle	PTC	JED22A-105	-	-	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if $\Delta T_j > 100^\circ\text{C}$ cannot be achieved with IOL Alternative to IOL	-
ESD Characterization	ESD HBM	AEC Q101-001 and 005	-	-		-
ESD Characterization	ESD CDM	AEC Q101-001 and 005	-	-		-
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	-	-	After H3TRB and TC	-
Physical Dimension	PD	JESD22B-100	-	60 (2*30)		X
Terminal Strength	TS	MIL-STD-750 Method 2036	-	-	Required for leaded parts only	-
Resistance to Solvents	RTS	JESD22B-107	-	--	Not applicable for Laser Marking	-
Constant Acceleration	CA	MIL-STD-750 Method 2006	-	-	Required for hermetic packaged parts only.	-
Vibration Variable Frequency	VVF	JESD22B-103	-	-	Required for hermetic packaged parts only.	-
Mechanical Shock	MS	JESD22 B-104	-	-	Required for hermetic packaged parts only.	-
Hermeticity	HER	JESD22A-109	-	-	Required for hermetic packaged parts only.	-
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	L1, L2, L3	90 (3*30)	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	X
Solderability	SD	J-STD-002 JESD22B102	L2	60 (4*15)		X
Dead Bug Test	DBT	ST Internal specification	L2	30	Mandatory for SMD package Data collection for PTH package	X
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	-	-	Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	-
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	-	-	Covered during workability trials	-
Bond Shear	BS	AEC-Q101-003	-	-	Covered during workability trials	-
Die Shear	DS	MIL-STD-750 Method 2017	-	-	Not Applicable to parts with solder paste die attach	-
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2	-	-	Required for Power MOS and internally clamped IGBTs only	--
Dielectric Integrity	DI	AEC-Q101-004 section 3	-	-	Required for Power MOSFET – IGBT only.	-
Short Circuit Reliability Characterization	SCR	AEC-Q101-006	-	-	Required for smart power parts only	-
Whisker Growth Evaluation	WG	AEC-Q005 JESD201	-	-		-
Early Life Failure Rate	ELFR	JESD74	-	-	Recommended for new techno development in case of identified failure mechanism	-
Functional Test (in rush, di/dt...)	FT	Internal specification	-	-		-
Repetitive Surge	RS	Internal specification	-	-	Required for protection devices only.	-

Low Temperature Storage	LTS	JESD-22 A119: 209	--	-	AQG324 test for Modules	-
Thermal shock test	TST	JESD22-A104	-	--	AQG324 test for Modules	-
Power Cycling (seconds)	PC sec	MIL-STD750-1 Method1037	--	-	AQG324 test for Modules	-
Power Cycling (minutes)	PC min	MIL-STD750-1 Method1037	-	-	AQG324 test for Modules	-

Mechanical shock	MS	IEC 60068-2-27	-	-	AQG324 test for Modules	-
Vibration	V	IEC60068-2-6	-	-	AQG324 test for Modules	-

### 5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS			
						L1	L2	L3	L4
PC	-	JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	-	522	0/522			
Parametric Verification	-	ST datasheet	Over part temperature range (note 1)	-	110	Refer to paragraph 6.1 in Annexes			
Physical Dimension	-	JESD22B-100	-	-	60	Refer to paragraph 6.2 in Annexes			
External Visual inspection	-	JESD22B-101	All qualification parts submitted for testing passed External & Visual inspection. during manufacturing process						
MS1	-	JESD22-A113	MSL=1, Reflow=3 Temperature=85°C Humidity (HR)=85%	168Hrs	30	0/30	-	-	-
HTRB	-	MIL-STD-750-1 M1038 Method A	Junction Temperature=125°C Voltage=800V	1Khrs	154	-	-	0/77	0/77
			Junction Temperature=125°C Voltage=600V		77	-	0/77	-	-
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	1Kcy	308	0/77	0/77	0/77	0/77
RSH	-	JESD22 A-111	Temperature=260°C Time (on)=10s	-	90	0/30	0/30	0/30	-
H3TRB	Y	JESD22 A-101	Humidity (HR)=85% Temperature=85°C Voltage=100V	1Khrs	77	-	0/77	-	-
UHAST	Y	JESD22 A-118	130°C; 85% RH 2.3bar	96hrs	77	-	0/77	-	-
SD	-	J-STD-002 JESD22 B-102	Wet ageing SnPb bath 220°C	-	15	-	0/15	-	-
			Dry ageing SnPb bath 220°C		15	-	0/15	-	-
			Wet ageing SnAgCu bath 245°C		15	-	0/15	-	-
			Dry ageing SnAgCu bath 245°C		15	-	0/15	-	-
DBT	-	DM00112629 (ST internal)	IR reflow after flux deposition	-	30	-	0/30	-	-

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.

Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers."

## 6 ANNEXES

### 6.1 Parametric Verification

#### Result on product of Z0109MUF

TEST	IDRM	IDRM	IRRM	IRRM	VTM	VTM
Condition 1	25°C	25°C	125°C	125°C	25°C	25°C
Condition 2	VDRM=600V	VDRM=600V	VDRM=600V	VDRM=600V	ITM=1,4A	ITM=1,4A
Condition 3	Direct	Reverse	Direct	Reverse	Direct	Reverse
Min. Datasheet						
Max. Datasheet	5	5	0,5	0,5	1,6	1,6
UNIT	uA	uA	mA	mA	V	V
N	40	40	10	10	40	40
Min	0,057	0,099	0,00789	0,01665	1,245	1,250
Max	0,263	0,326	0,00955	0,02345	1,305	1,302
Moy.	0,125	0,247	0,00858	0,01950	1,259	1,264

TEST	IGT Q1	IGT Q2	IGT Q3	IGT Q4	VGT Q1	VGT Q2	VGT Q3	VGT Q4
Condition 1	25°C							
Condition 2	VD=12V							
Condition 3	RL=30ohms							
Min. Datasheet								
Max. Datasheet	10	10	10	10	1,3	1,3	1,3	1,3
UNIT	mA	mA	mA	mA	V	V	V	V
N	40	40	40	40	40	40	40	40
Min	1	2,4	2,7	5,799	0,673	0,695	0,737	0,843
Max	1,099	2,799	3,1	7,299	0,691	0,707	0,752	0,881
Moy.	1,077	2,704	2,887	6,284	0,682	0,702	0,744	0,851

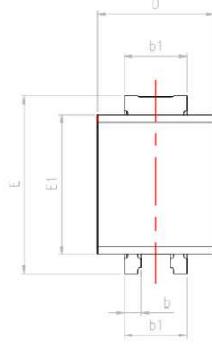
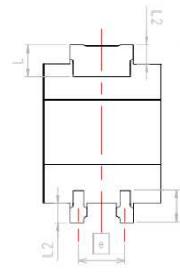
TEST	IH	IH	IL Q1	IL Q2	IL Q3	IL Q4
Condition 1	25°C	25°C	25°C	25°C	25°C	25°C
Condition 2	IT=50mA	IT=50mA	IG=12mA	IG=12mA	IG=12mA	IG=12mA
Condition 3	IG=15mA	IG=15mA				
Min. Datasheet	Direct	Reverse				
Max. Datasheet	10	10	15	25	15	15
UNIT	mA	mA	mA	mA	mA	mA
N	40	40	40	40	40	40
Min	1,480	1,860	2,938	13,360	2,400	4,618
Max	1,780	2,060	3,387	13,650	2,625	5,214
Moy.	1,657	1,990	3,209	13,547	2,529	4,826

## Result on product of TS110-8SUF

TEST	IDRM	IDRM	IRRM	IRRM
Condition 1	25°C	125°C	25°C	125°C
Condition 2	VDRM=800V	VDRM=800V	VDRM=800V	VDRM=800V
Condition 3	RGK=220Ohms	RGK=220Ohms	RGK=220Ohms	RGK=220Ohms
Min. Datasheet	Direct	Reverse	Direct	Reverse
Typ. Datasheet				
Max. Datasheet	1	100	1	100
UNIT	uA	mA	uA	mA
N	50	10	50	10
Min	9,345	0,307	0,000	1,629
Max	198,000	0,771	238,900	2,733
Moy.	61,884	0,528	111,019	2,093

TEST	VGT	IGT	IH	IL Q1	VTM
Condition 1	25°C	25°C	25°C	25°C	25°C
Condition 2	VD=12V	VD=12V	IT=50mA	IG=5mA	ITM=2,5A
Condition 3	RL=140ohms	RL=140ohms	RGK=220Ohms	RGK=220Ohms	
Min. Datasheet					
Typ. Datasheet		1			
Max. Datasheet	0,8	100	12	12	1,6
UNIT	V	uA	mA	mA	V
N	50	50	50	50	50
Min	0,593	6,910	5,860	6,132	1,396
Max	0,606	17,100	6,820	7,157	1,437
Moy.	0,601	11,986	6,383	6,718	1,419

## 6.2 Physical Dimensions

New SMB Flat Package																																																																																																																																															
Package outline						Dimensions values																																																																																																																																									
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## 6.3 Tests description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTRB</b> High Temperature Reverse Bias / <b>HTFB</b> High Temperature Forward Bias	<p>The device is stressed in static configuration, trying to satisfy as much as possible the following conditions:</p> <ul style="list-style-type: none"> <li>- Low power dissipation</li> <li>- Max. supply voltage compatible with diffusion process and internal circuitry limitations.</li> </ul> <p>Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature</p>	<p>To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way.</p> <p>To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.</p> <p>To assess active area and contacts integrity</p>
<b>Package Oriented</b>		
<b>PC</b> Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	<p>As stand-alone test: to investigate the moisture sensitivity level.</p> <p>As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.</p>
<b>H3TRB</b> High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
<b>TC</b> Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>UHAST</b> Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>RSH</b> Resistance to Solder Heat	Package is dipped by the leads in a solder bath after initial wet ageing (for SMDs only). Assessment by electrical test + no external crack	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
<b>SD</b> Solderability	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.
<b>DBT</b> Dead Bug Test	To evaluate the wettability of the package leads. Good indicator to determine the bad solderability behavior	Components are glued up-side down on a substrate. Pins are wetted with a moderately activated flux. Then run once through the reflow oven with leadfree temperature profile. Visual inspection is performed with suitable tool.
<b>Functional Tests</b>		