PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/22/13808
1.3 Title of PCN	ACEPACK SMIT Line Transfer to Shenzhen (China)
1.4 Product Category	Power MOSFET HV
1.5 Issue date	2022-11-28

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Maurizio GIUDICE
2.1.2 Marketing Manager	Paolo PETRALI
2.1.3 Quality Manager	Vincenzo MILITANO

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	Shenzhen (China)

4. Description of change		
	Old	New
4.1 Description	ACEPACK SMIT products are manufactured in Integrated Micro-Electronics Inc. (Philippines)	ACEPACK SMIT products are manufactured in Shenzhen (China)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	no impact	

5. Reason / motivation for change	
5.1 Motivation	ACEPACK SMIT Automotive line Transfer
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	By internal traceability and dedicated FG code

7. Timing / schedule	
7.1 Date of qualification results	2023-01-31
7.2 Intended start of delivery	2023-05-29
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13808 Binder1.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2022-11-28

9. Attachments (additional documentations)

13808 Public product.pdf
13808 ACEPACK SMIT Line transfer to Shenzhen (China).pdf
13808 Binder1.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	SH32N65DM6AG	
	SH68N65DM6AG	

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PCN ADG/22/13808

Catania, November 25, 2022

Power Transistor Sub-Group
High Voltage Business Unit
Automotive & Discrete Group (ADG)

Process Change Notification

ACEPACK SMIT Line Transfer to Shenzhen (China)
AUTOMOTIVE

Dear Customer,

Following the continuous improvement of our service and with the aim of increasing production capacity, this document announces ACEPACK SMIT Line Transfer to Shenzhen (China).
ACEPACK SMIT manufactured in Shenzhen, has the same POA and it guarantees the same electrical characteristics as per current production.

Qualification program and results availability:
The intermediate Reliability Qualification Report is provided in attachment to this document.
The Final Report will be released after the end of January 2023 with results of PCsec/PCmin Characterization.

Samples availability:
Samples of the test vehicle devices will be available on request starting from week 50 of 2022.
Any other sample request will be processed and scheduled by High Voltage Business Unit upon request.

Involved Products	Package	Test Vehicle
Power MOSFET Transistors	ACEPACK SMIT	SH32N65DM6AG SH68N65DM6AG

Change implementation schedule:
The production start and first will be implemented after agreement with the customer.

Marking and traceability:
Unless otherwise stated by customer specific requirement, traceability of products in ACEPACK SMIT, manufactured in Shenzhen (China) will be ensured by internal code (Finished Good) and Q.A. number.

Yours faithfully.

SH68N65DM6AG (PQ7ZA6)
Power Module HV MOSFET MDMESH DM6
Package ACEPACK SMIT – ST Shenzhen
Reliability Evaluation Report

General Information	
Commercial Product	**SH68N65DM6AG**
Product Line	**PQ7ZA6**
Silicon process Technology	**HV MOSFET MDMESH DM6**
Package	**ACEPACK SMIT**

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Revision history

Rev.	Changes description	Author	Date
1	Release without PC characterization	T.Lo Piparo ADG Reliability	17th November, 2022
2	Updated Generalities (Final Datasheet)	T.Lo Piparo ADG Reliability	21st November, 2022
3	Update ST logo	T.Lo Piparo ADG Reliability	25th November, 2022

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Catania (Italy)	V.Giuffrida	25th November, 2022

Table of Contents

1. Reliability Evaluation Overview

1.1. Objective

Aim of this report is to present the reliability evaluation results performed on **SH68N65DM6AG** (PQ7ZA6 as ST internal silicon line) that is a Power Module intended for Automotive application, including 2 dice designed in HV MOSFET MDMESH DM6 Technology, diffused in ST SG8 Singapore 8" Wafer Fab and assembled in ACEPACK SMIT package in ST Shenzhen (China).

1.2. Reliability Strategy and Test Plan

1.2.1. Reliability strategy

Reliability tests were performed in agreement with AQG-324 Ver.02.1/2019 specification, stress tests are listed in the Test Plan below.

For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

1.2.2. Test Plan

AQG 324 Test Plan Table

#	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
1	QM TEST	Pre- and Post-Stress Electrical Test	Yes
2	IPI/VI/OMA	Internal Physical Inspection/Visual Inspection Optical Microscope Assessment	Yes
3	ISO test	Isolation test	Yes
4	QM-01	Interconnection Layers (**SAM**)	Yes
5	QC-01	Determining Parasitic Stray Inductance (**Lp**)	Yes
6	QC-02	Determining Thermal Resistance (**Rth** measure)	Yes
7	QC-03	Determining Short-Circuit Capability	Yes
8	QC-04	Insulation Test	Yes
9	QC-05	Determining Mechanical Data	Yes
10	QE-01	Thermal Shock Test (**TST**)	Yes
11	QE-02	Contactability (**CO**)	No
12	QE-03	Vibration (**V**)	Yes
13	QE-04	Mechanical Shock (MS)	Yes
14	QL-01	Power Cycling (**PCsec**)	Yes
15	QL_02	Power Cycling (**PCmin**)	Yes
16	QL-03	High Temperature Storage (**HTS**)	Yes
17	QL-04	Low Temperature Storage (**LTS**)	Yes
18	QL-05	High Temperature Reverse Bias (**HTRB**)	Yes
19	QL-06	High Temperature Gate Bias (**HTGB**)	Yes
20	QL-07	High-humidity High-temperature reverse bias (**H3TRB**)	Yes

1.3. Conclusion

All reliability tests have been completed with positive results, neither functional nor parametric rejects were detected at final electrical testing.

Only PCsec/PCmin characterization is still running. The current report will be updated as soon as those activities will be completed.

Based on the achieved positive results, the Power Module **SH68N65DM6AG** (PQ7ZA6 as ST internal silicon line) intended for Automotive application, including 2 dice designed in HV MOSFET MDMESH DM6 Technology, diffused in ST SG8 Singapore 8" Wafer Fab and assembled in ACEPACK SMIT package in ST Shenzhen China, has positively passed the reliability evaluation in agreement with ST 0061692 guideline and AQG324 Ver.02/2019 specification.

2. Product Characteristics

2.1. Generalities

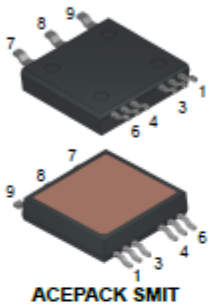
Power Module HV MOSFET MDMESH DM6

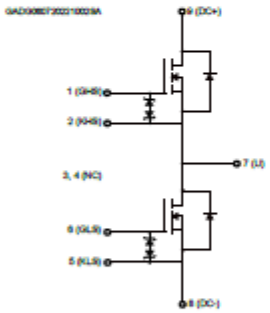
life.augmented

SH68N65DM6AG

Datasheet

Automotive-grade N-channel 650 V, 35 mΩ typ., 64 A MDmesh DM6 half-bridge topology Power MOSFET in an ACEPACK SMIT package





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SH68N65DM6AG	650 V	41 mΩ	64 A

- AQG 324 qualified
- Half-bridge power module
- 650 V blocking voltage
- Fast recovery body diode
- Very low switching energies
- Low package inductance
- Dice on direct bond copper (DBC) substrate
- Low thermal resistance
- Isolation rating of 3.4 kVrms/min

Applications

- Switching applications

Description

This device combines two MOSFETs in a half-bridge topology. The ACEPACK SMIT is a very compact and rugged power module in a surface mount package for easy assembly. Thanks to the DBC substrate, the ACEPACK SMIT package offers low thermal resistance coupled with an isolated top-side thermal pad. The high design flexibility of the package enables several configurations, including phase legs, boost, and single switch through different combinations of the internal power switches.

Product status link
SH68N65DM6AG

Product summary	
Order code	SH68N65DM6AG
Marking	H68N65DM6
Package	ACEPACK SMIT
Packing	Tape and reel

2.2. Traceability

2.2.1. Lot Information

Batch #	Wafer lot #	Die Code	Assy lot #
1	C20956K	XPQ7ZA8V	GK2230Q701

2.2.2. Wafer Fab information

Wafer fab name / location	ST SG8 Singapore
Wafer diameter (inches)	8”
Silicon process technology	HV MOSFET MDMESH DM6
Die finishing front side	Ti/TiN/TiAlCu + TEOS + SiN
Die finishing back side	Ti-NiV-Ag
Die area (Stepping die size)	11700 x 6850 µm
Wafer Thickness	200um +/-20um

2.2.3. Assembly information

Assembly plant name / location	ST Shenzhen
Package	ACEPACK SMIT
Resin	KCC KTMC 5800GVP D18mm W12.4g
DBC	CERAMIC SMIT AL2O3
Solder	Solder paste Pb/Sn/Ag /5/2.5 Print. 500g
Frame	FRAME SMIT 9L 237x62 BareCu
Wire bonding material/diameter	- WIRE Al-Mg .5% D5 BL150-160g EL8-22% 400 - WIRE Al D15 BL550-750g EL10-30% CR spC/2

2.2.4. Reliability Testing information

Reliability laboratory location	STM Catania (Italy)
Electrical testing / location	Accotest test system / Catania (Italy)

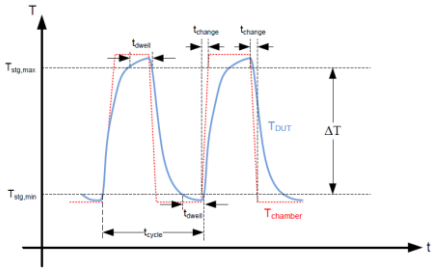
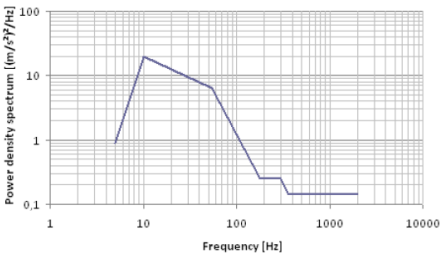
3. Tests Results Summary

3.1. Test results summary (table)

Test method revision reference is the one active at the date of reliability trial execution.

Test #	Test Name	Reference	STM Test Conditions	Comments
-	Preconditioning	JESD22-A113 JSTD-020	MSL3 - 24h bake @125°C Store 192h @ TA=30°C RH=60% 3x IR Reflow @ 260°C	Performed on SMD package for all biased qualification parts before stress

#	Test Name	Reference	AQG324 - STM Test Name/Conditions	Lots	Sample size	Total	Results Fail/SS/Lots	Comments
1	QM TEST		User specification or supplier's standard specification	1	84	84	0/84/1	All qualification parts before/after stress
2	IPI/VI/ OMA			1	84	84	0/84/1	All qualification parts before/after stress
3	ISO test	Short Circuit capability	Forcing 3600V on power paths	1	84	84	0/84/1	All qualification parts before/after stress
4	QM-01	Interconnection layer test	SAM analysis	1	24	24	0/24/1	All parts submitted to QC-05, QE-01, QL-01 and QL-02
5	QC-01	IEC 60747-15:2012, section 5.3.2 (double pulse testing)	Parasitic Stray inductance (**Lp**) double pulse	1	72	72	0/72/1	All parts submitted to QC-03, QC-04, QE and QL
6	QC-02	IEC 60747-15:2012, section 5.3.6	Thermal Resistance (**Rth**)	1	6	6	0/6/1	To be done, linked with Power Cycling test
7	QC-03	AQG 324	Hard Switch and Under Load failures Vds: 400V; Vgs=18V; Tp:1.7us;	1	6	6	0/6/1	3 samples coming from QC-01 and 3 from QC-02
8	QC-04	AQG 324	Insulation Test	1	6	6	0/6/1	3 samples coming from QC-01 and 3 from QC-02

<table>
<tr><td>9</td><td>QC-05</td><td></td><td>Mechanical Data/User specification</td><td>1</td><td>6</td><td>6</td><td>0/6/1</td><td></td></tr>
<tr><td>10</td><td>QE-01</td><td>IEC 60749-25:2003</td><td>Thermal Shock Test (TST)
Ta= -40°C/125°C, duration= 1000cy
<table><tr><td>Lowest value of the storage temperature</td><td>$T_{stg,min}$</td><td>$-40°C^{0}_{-10}$</td></tr><tr><td>Highest value of the storage temperature</td><td>$T_{stg,max}$</td><td>$+125°C^{+15}_{0}$</td></tr><tr><td>Transfer duration</td><td>t_{change}</td><td>< 30 s</td></tr><tr><td>Minimum dwell time for highest/lowest temperature</td><td>t_{dwell}</td><td>> 15 min</td></tr><tr><td>Minimum number of cycles without failures</td><td>N_C</td><td>> 1000</td></tr></table>  </td><td>1</td><td>6</td><td>6</td><td>0/6/1</td><td></td></tr>
<tr><td>11</td><td>QE-02</td><td></td><td>Contactability (CO)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Withdrawn for the time being on AQG-324</td></tr>
<tr><td>12</td><td>QE-03</td><td>IEC 60068-2-6
IEC 60068-2-64</td><td>Vibration (V)
T ambient - Vibration profile D as per AQG324 (components installed on sprung masses)
<table><tr><td>Vibration excitation</td><td colspan="2">Wide-band random vibration</td></tr><tr><td>Test duration for each spatial axis</td><td colspan="2">8 h</td></tr><tr><td>RMS value of acceleration</td><td colspan="2">30.8 m/s²</td></tr><tr><td rowspan="9">Vibration profile Figure 8.6</td><td>Frequency in Hz</td><td>Power density spectrum in (m/s²)²/Hz</td></tr><tr><td>5</td><td>0.884</td></tr><tr><td>10</td><td>20</td></tr><tr><td>55</td><td>6.5</td></tr><tr><td>180</td><td>0.25</td></tr><tr><td>300</td><td>0.25</td></tr><tr><td>360</td><td>0.14</td></tr><tr><td>1 000</td><td>0.14</td></tr><tr><td>2 000</td><td>0.14</td></tr></table>  </td><td>1</td><td>6</td><td>6</td><td>0/6/1</td><td></td></tr>
</table>

13	QE-04	IEC 60068-2-27	Mechanical Shock (**MS**) Peak acceleration = 500m/s2 shock duration = 6ms shock form = half-sine n. shock per direction (±X, ±Y, ±Z) = 10	1	6	6	0/6/1	
14	QL-01	IEC 60749-34:2011	Power Cycling Short **(Pcsec)** Electric Forcing conditions: Forcing Mode: MOSFET Vgate: tuned for each switch to reach DT_j = 100degC T_{on}=tbd s (t_{cy} = xx s) I_{load}=xxA	1	6	6	First fail occurred - for V_{ds} drift > 5%	To be completed
15	QL-02	IEC 60749-34:2011	Power Cycling Long **(Pcmin)** Electric Forcing conditions: Forcing Mode: MOSFET Vgate: tuned for each switch to reach DT_j = 100degC t_{on}=xxs (t_{cy} = xxs) I_{load}=xxA	1	6	6	First fail occurred - for V_{ds} drift > 5%	
16	QL-03	IEC 60749-6:2002	High Temperature Storage (**HTS**) T_j=150°C, duration=1000h	1	6	6	0/6/1	
17	QL-04	JEDEC JESD-22 A119:2009	Low Temperature Storage (**LTS**) T_j=-40°C, duration=1000h	1	6	6	0/6/1	
18	QL-05	IEC 60747-9:2007	High Temperature Reverse Bias (**HTRB**) Vbias= 80% Vsd max - T_j = 150°C duration=1000h	1	6	6	0/6/1	
19a	QL-06	IEC 60747-9:2007	High Temperature Gate Bias (**HTGB**) Vbias = Vgs max = +25V - T_j = 150°C duration=1000h	1	6	6	0/6/1	
19b			Vbias = Vgs max = -25V - T_j = 150°C duration=1000h	1	6	6	0/6/1	
20	QL-07	IEC 60747	High-humidity High-temperature reverse bias (**H3TRB**) Vbias= 100V, Ta = 85°C, RH=85% duration=1000h	1	6	6	0/6/1	

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SH32N65DM6AG (PQ7LA6)
Power Module HV MOSFET MDMESH DM6
Package ACEPACK SMIT – ST Shenzhen
Reliability Evaluation Report

General Information	
Commercial Product	**SH32N65DM6AG**
Product Line	**PQ7LA6**
Silicon process Technology	**HV MOSFET MDMESH DM6**
Package	**ACEPACK SMIT**

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Revision history

Rev.	Changes description	Author	Date
1.0	Release without PC characterization	T.Lo Piparo ADG Reliability	18th November 2022
2.0	Updated Generalities (Final Datasheet)	T.Lo Piparo ADG Reliability	21st November 2022
3.0	Update ST logo	T.Lo Piparo ADG Reliability	25th November, 2022

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Catania (Italy)	V.Giuffrida	25th November, 2022

Table of Contents

1. Reliability Evaluation Overview

1.1. Objective

Aim of this document is to present the qualification plan to release in mass production the Power Module **SH32N65DM6AG** (PQ7LA6 as ST internal line) intended for Automotive application designed in HV MOSFET MDMESH Technology, diffused in ST SG8 Singapore 8" Wafer Fab and assembled in ACEPACK SMIT package in ST Shenzhen (China).

The **SH32N65DM6AG** (PQ7LA6) is classified as Derivative of Master device **SH68N65DM6AG** (PQ7ZA6 as ST internal line) sharing same Front-End Technology and diffusion fab, same Back-End Package typology, Bill of Material and assembly plant but lower switches size.

1.2. Reliability Strategy and Test Plan

1.2.1. Reliability strategy

Reliability tests were performed in agreement with AQG-324 Ver.02.1/2019 specification, stress tests are listed in the Test Plan below.

For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

1.2.2. Test Plan

AQG 324 Test Plan Table

#	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
1	QM TEST	Pre- and Post-Stress Electrical Test	Yes
2	IPI/VI/OMA	Internal Physical Inspection/Visual Inspection Optical Microscope Assessment	Yes
3	ISO test	Isolation test	Yes
4	QM-01	Interconnection Layers (**SAM**)	Yes
5	QC-01	Determining Parasitic Stray Inductance (**Lp**)	Yes
6	QC-02	Determining Thermal Resistance (**Rth** measure)	Yes
7	QC-03	Determining Short-Circuit Capability	Yes
8	QC-04	Insulation Test	Yes
9	QC-05	Determining Mechanical Data	Yes
10	QE-01	Thermal Shock Test (**TST**)	Similarity (generic data)
11	QE-02	Contactability (**CO**)	No
12	QE-03	Vibration (**V**)	Similarity (generic data)
13	QE-04	Mechanical Shock (MS)	Similarity (generic data)
14	QL-01	Power Cycling (**PCsec**)	Similarity (generic data)
15	QL_02	Power Cycling (**PCmin**)	Similarity (generic data)
16	QL-03	High Temperature Storage (**HTS**)	Similarity (generic data)
17	QL-04	Low Temperature Storage (**LTS**)	Similarity (generic data)
18	QL-05	High Temperature Reverse Bias (**HTRB**)	Similarity (generic data)
19	QL-06	High Temperature Gate Bias (**HTGB**)	Similarity (generic data)
20	QL-07	High-humidity High-temperature reverse bias (**H3TRB**)	Similarity (generic data)

1.3. Conclusion

The reliability tests on Master device **SH68N65DM6AG** has been positively completed (refer to #RERPTD22088 Reliability Report), results are extended also to the derivative product **SH32N65DM6AG**.

Only PCsec/PCmin characterization is still running. The current report will be updated as soon as those activities will be completed.

Product Characteristics

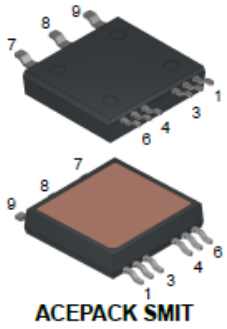
1.4. Generalities

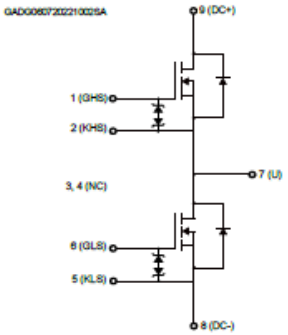
Power Module HV MOSFET MDMESH DM6

SH32N65DM6AG

Datasheet

Automotive-grade N-channel 650 V, 89 mΩ typ., 32 A MDmesh DM6 half-bridge topology Power MOSFET in an ACEPACK SMIT package





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
SH32N65DM6AG	650 V	97 mΩ	32 A

- AQG 324 qualified
- Half-bridge power module
- 650 V blocking voltage
- Fast recovery body diode
- Very low switching energies
- Low package inductance
- Dice on direct bond copper (DBC) substrate
- Low thermal resistance
- Isolation rating of 3.4 kVrms/min

Applications

- Switching applications

Description

This device combines two MOSFETs in a half-bridge topology. The ACEPACK SMIT is a very compact and rugged power module in a surface mount package for easy assembly. Thanks to the DBC substrate, the ACEPACK SMIT package offers low thermal resistance coupled with an isolated top-side thermal pad. The high design flexibility of the package enables several configurations, including phase legs, boost, and single switch through different combinations of the internal power switches.

Product status link
SH32N65DM6AG

Product summary	
Order code	SH32N65DM6AG
Marking	H32N65DM6
Package	ACEPACK SMIT
Packing	Tape and reel

1.5. Traceability

1.5.1. Lot information

Batch #	Wafer lot #	Die Code	Assy lot #
1	C11930P	XPQ7LA8V	GK2230Q801

1.5.2. Wafer Fab information

Wafer fab name / location	ST SG8 Singapore
Wafer diameter (inches)	8”
Silicon process technology	HV MOSFET MDMESH DM6
Die finishing front side	Ti/TiN/TiAlCu + TEOS + SiN
Die finishing back side	Ti-NiV-Ag
Die area (Stepping die size)	6850 x 5080 µm
Wafer Thickness	200um +/-20um

1.5.3. Assembly information

Assembly plant name / location	ST Shenzhen
Package	ACEPACK SMIT
Resin	KCC KTMC 5800GVP D18mm W12.4g
DBC	CERAMIC SMIT AL2O3
Solder	Solder paste Pb/Sn/Ag /5/2.5 Print. 500g
Frame	FRAME SMIT 9L 237x62 BareCu
Wire bonding material/diameter	- WIRE Al-Mg .5% D5 BL150-160g EL8-22% 400 - WIRE Al D15 BL550-750g EL10-30% CR spC/2

1.5.4. Reliability Testing information

Reliability laboratory location	STM Catania (Italy)
Electrical testing / location	Accotest test system / Catania (Italy)

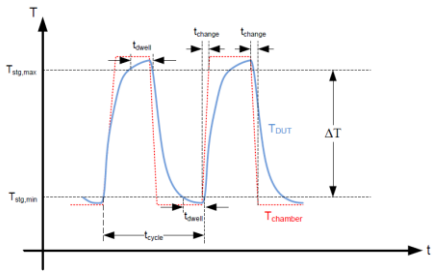
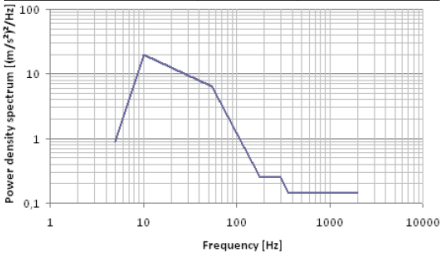
2. Tests Results Summary

2.1. Test results summary (table)

Test method revision reference is the one active at the date of reliability trial execution.

Test #	Test Name	Reference	STM Test Conditions	Comments
-	Preconditioning	JESD22-A113 JSTD-020	MSL3 - 24h bake @125°C Store 192h @ TA=30°C RH=60% 3x IR Reflow @ 245°C	Performed on SMD package for all biased qualification parts before stress

#	Test	Reference	AQG324 - STM Test Name/Conditions	Lots	Sample size	Total	Results Fail/SS/ Lots	Comments
1	QM TEST		User specification or supplier's standard specification	1	30	30	0/30/1	All qualification parts before/after stress
2	IPI/VI/ OMA			1	30	30	0/30/1	All qualification parts before/after stress
3	ISO test		Forcing 3600V on power paths	1	30	30	0/30/1	All qualification parts before/after stress
4	QM-01	Interconnection layer test	SAM analysis	1	6	6	0/6/1	All parts submitted to QC-05, QE-01, QL-01 and QL-02
5	QC-01	IEC 60747-15:2012, section 5.3.2 (double pulse testing)	Parasitic stray inductance Lp between current paths and main contacts	1	12	12	0/12/1	All parts submitted to QC-03, QC-04, QE and QL
6	QC-02	IEC 60747-15:2012, section 5.3.6	Thermal Resistance (**Rth**)	1	6	6	0/6/1	
7	QC-03	AQG 324	Hard Switch and Under Load failures	1	6	6	0/6/1	3 samples coming from QC-01 and 3 from QC-02
8	QC-04	AQG 324	Insulation Test	1	6	6	0/6/1	3 samples coming from QC-01 and 3 from QC-02
9	QC-05		Mechanical Data/User specification	1	6	6	0/6/1	

<table>
<tr><td>10</td><td>QE-01</td><td>IEC 60749-25:2003</td><td>Thermal Shock Test (TST)
Ta= -40°C/125°C, duration= 1000cy
<table><tr><td>Lowest value of the storage temperature</td><td>$T_{stg,min}$</td><td>$-40°C^{0}_{-10}$</td></tr><tr><td>Highest value of the storage temperature</td><td>$T_{stg,max}$</td><td>$+125°C^{+15}_{0}$</td></tr><tr><td>Transfer duration</td><td>t_{change}</td><td>< 30 s</td></tr><tr><td>Minimum dwell time for highest/lowest temperature</td><td>t_{dwell}</td><td>> 15 min</td></tr><tr><td>Minimum number of cycles without failures</td><td>N_C</td><td>> 1000</td></tr></table>  </td><td>-</td><td>-</td><td>-</td><td>-</td><td>Family data</td></tr>
<tr><td>11</td><td>QE-02</td><td></td><td>Contactability (CO)</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Withdrawn for the time being on AQG-324</td></tr>
<tr><td>12</td><td>QE-03</td><td>IEC 60068-2-6
IEC 60068-2-64</td><td>Vibration (V)
T ambient - Vibration profile D as per AQG324
(components installed on sprung masses)
<table><tr><td>Vibration excitation</td><td colspan="2">Wide-band random vibration</td></tr><tr><td>Test duration for each spatial axis</td><td colspan="2">8 h</td></tr><tr><td>RMS value of acceleration</td><td colspan="2">30.8 m/s²</td></tr><tr><td rowspan="9">Vibration profile Figure 8.6</td><td>Frequency in Hz</td><td>Power density spectrum in (m/s²)²/Hz</td></tr><tr><td>5</td><td>0.884</td></tr><tr><td>10</td><td>20</td></tr><tr><td>55</td><td>6.5</td></tr><tr><td>180</td><td>0.25</td></tr><tr><td>300</td><td>0.25</td></tr><tr><td>360</td><td>0.14</td></tr><tr><td>1 000</td><td>0.14</td></tr><tr><td>2 000</td><td>0.14</td></tr></table>  </td><td>-</td><td>-</td><td>-</td><td>-</td><td>Family data</td></tr>
<tr><td>13</td><td>QE-04</td><td>IEC 60068-2-27</td><td>Mechanical Shock (MS)
<table><tr><td>Peak acceleration</td><td>500 m/s²</td></tr><tr><td>Shock duration</td><td>6 ms</td></tr><tr><td>Shock form</td><td>half-sine</td></tr><tr><td>Number of shocks per direction (±X, ±Y, ±Z)</td><td>10</td></tr><tr><td>Number of DUTs</td><td>6</td></tr></table></td><td>-</td><td>-</td><td>-</td><td>-</td><td>Family data</td></tr>
<tr><td>14</td><td>QL-01</td><td>IEC 60749-34:2011</td><td>Power Cycling Short (Pcsec)

Electric Forcing conditions:
Forcing Mode: MOSFET
Vgate: tuned for each switch to reach
DTj = 100degC
T_{on}=3.5s (t_{cy} = 7.5s)
I_{load}=50A</td><td>-</td><td>-</td><td>-</td><td>-</td><td rowspan="2">To be completed</td></tr>
<tr><td>15</td><td>QL-02</td><td>IEC 60749-34:2011</td><td>Power Cycling Long (Pcmin)

Electric Forcing conditions:
Forcing Mode: MOSFET
Vgate: tuned for each switch to reach
DTj = 100degC
t_{on}=20s (t_{cy} = 45s)
I_{load}=48A</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
</table>

16	QL-03	IEC 60749-6:2002	High Temperature Storage (**HTS**) Ta=150°C, duration=1000h	-	-	-	-	Family data
17	QL-04	JEDEC JESD-22 A119:2009	Low Temperature Storage (**LTS**) Ta=-55°C, duration=1000h	-	-	-	-	Family data
18	QL-05	IEC 60747-9:2007	High Temperature Reverse Bias (**HTRB**) Vbias=520V - Tj = 150°C duration=1000h	-	-	-	-	Family data
19a	QL-06	IEC 60747-9:2007	High Temperature Gate Bias (**HTGB**) Vbias = Vgs max = +25V - Tj = 150°C duration=1000h	-	-	-	-	Family data
19b			Vbias = Vgs max = -25V - Tj = 150°C duration=1000h	-	-	-	-	Family data
20	QL-07	IEC 60747	High-humidity High-temperature reverse bias (**H3TRB**) Vbias= 100V, Ta = 85°C, RH=85% duration=1000h	-	-	-	-	Family data

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