


PRODUCT / PROCESS CHANGE INFORMATION

1. PCI basic data

1.1 Company		STMicroelectronics International N.V
1.2 PCI No.	ADG/22/13595	
1.3 Title of PCI	STL220N6F7 (OD68): Datasheet Updated	
1.4 Product Category	STL220N6F7	
1.5 Issue date	2022-08-02	

2. PCI Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
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2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Mario ASTUTI
2.1.2 Marketing Manager	Michele SCUTO
2.1.3 Quality Manager	Daniela FAZIO

3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Modification of datasheet : Errata/error fix	NA

4. Description of change

	Old	New
4.1 Description	Datasheet revision 4	Datasheet revision 5
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change

5.1 Motivation	Datasheet update
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change

6.1 Description	Datasheet available on www.st.com
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7. Timing / schedule

7.1 Date of qualification results	2022-08-01
7.2 Intended start of delivery	2022-09-01
7.3 Qualification sample available?	Not Applicable

8. Qualification / Validation

8.1 Description	13595_DS_STL220N6F7_rev5.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2022-08-02

9. Attachments (additional documentations)

13595 Public product.pdf
13595_DS_STL220N6F7_rev5.pdf
13595 Details.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STL220N6F7	

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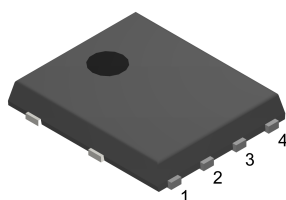
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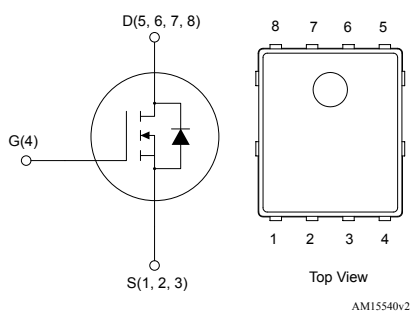
PRODUCT/PROCESS CHANGE INFORMATION

TITLE	STL220N6F7 (OD68): Datasheet Update
CHANGE REASON	Service Continuity
CHANGE DESCRIPTION	Document update See Datasheet history for details
TRACEABILITY	Datasheets available on www.st.com and included in this communication

N-channel 60 V, 1.2 mΩ typ., 120 A STripFET F7 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL220N6F7	60 V	1.4 mΩ	120 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



Product status link

[STL220N6F7](#)

Product summary

Order code	STL220N6F7
Marking	220N6F7
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(2)(1)}$	Drain current (pulsed)	480	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	40	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	28.5	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	160	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_{AS} = 20\text{ A}$)	900	mJ
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	188	W
$P_{TOT}^{(3)}$	Total power dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
T_j	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
	Storage temperature range		

1. This value is rated according to R_{thj-c} .
2. Pulse width limited by safe operating area.
3. This value is rated according to $R_{thj-pcb}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case	0.8	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$		1.2	1.4	m Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	6500	-	pF
C_{oss}	Output capacitance		-	3200	-	pF
C_{rss}	Reverse transfer capacitance		-	230	-	pF
Q_g	Total gate charge	$V_{DD} = 30\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	98	-	nC
Q_{gs}	Gate-source charge		-	38	-	nC
Q_{gd}	Gate-drain charge		-	28	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$, $I_D = 20\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see and Figure 17. Switching time waveform)	-	41	-	ns
t_r	Rise time		-	45	-	ns
$t_{d(off)}$	Turn-off delay time		-	68	-	ns
t_f	Fall time		-	35	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 40\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_D = 40\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	69		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 48\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	103		nC
I_{RRM}	Reverse recovery current		-	3		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

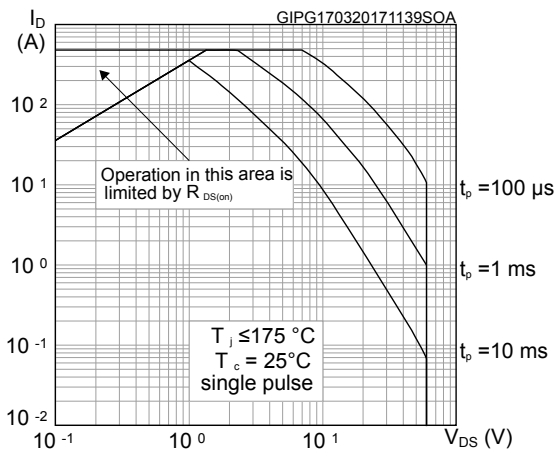
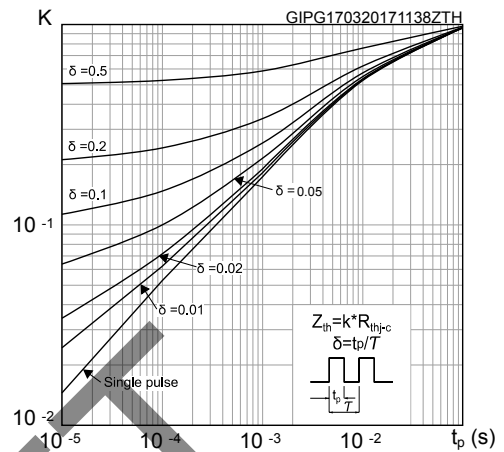
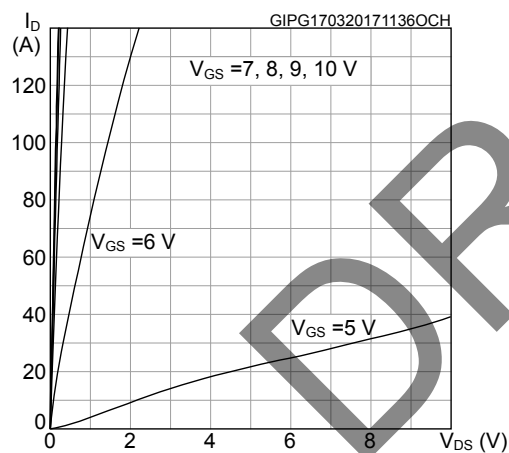
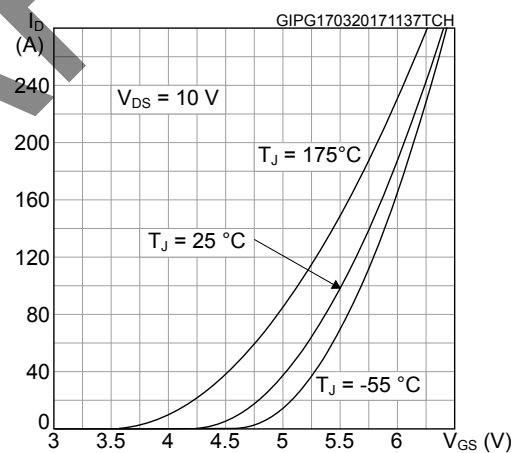
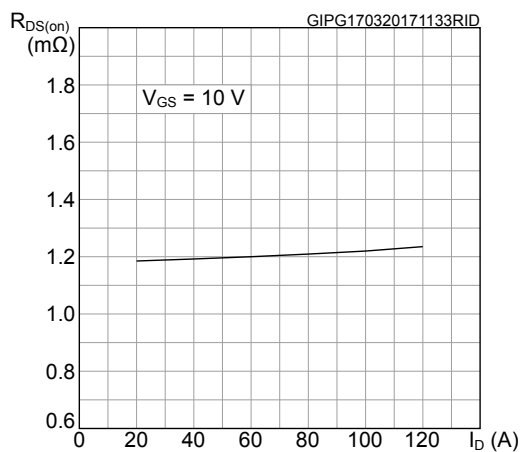
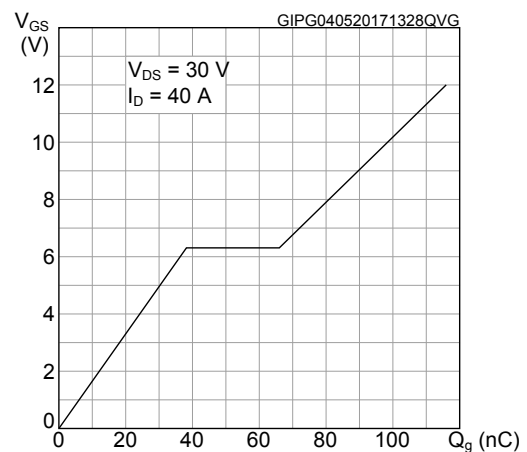
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Static drain-source on-resistance

Figure 6. Gate charge vs gate-source voltage


Figure 7. Capacitance variations

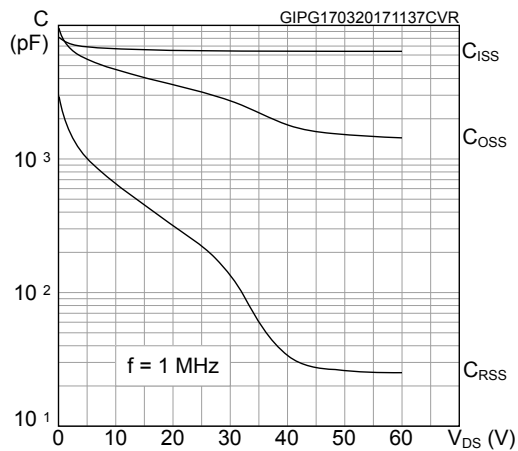


Figure 8. Normalized gate threshold voltage vs temperature

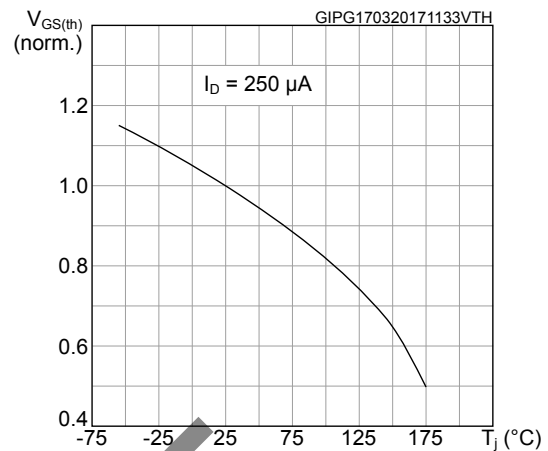


Figure 9. Normalized on-resistance vs temperature

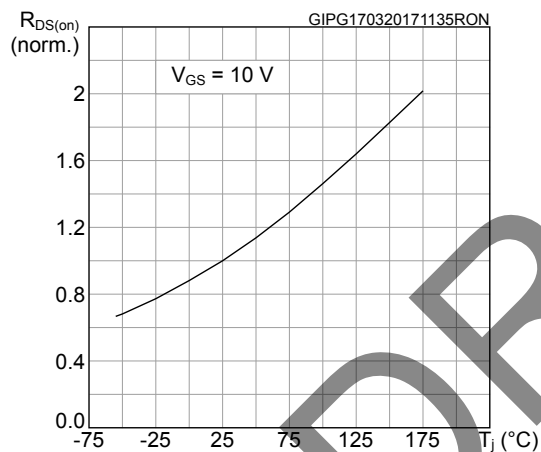


Figure 10. Source-drain diode forward characteristics

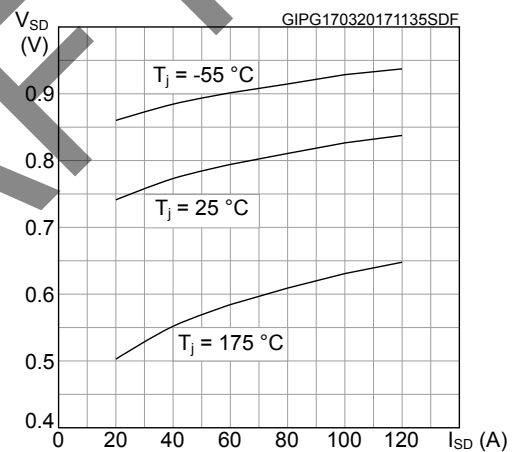
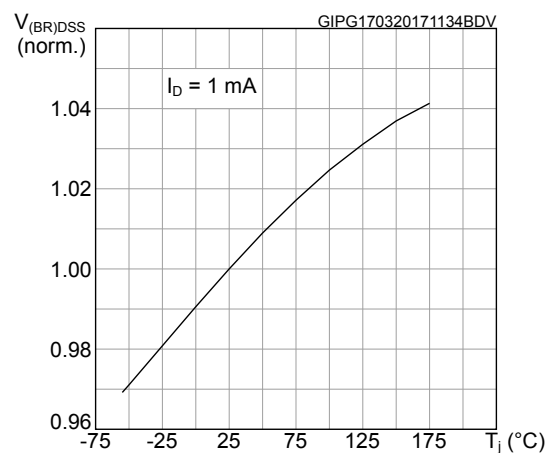
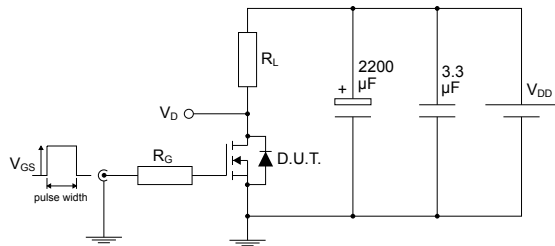


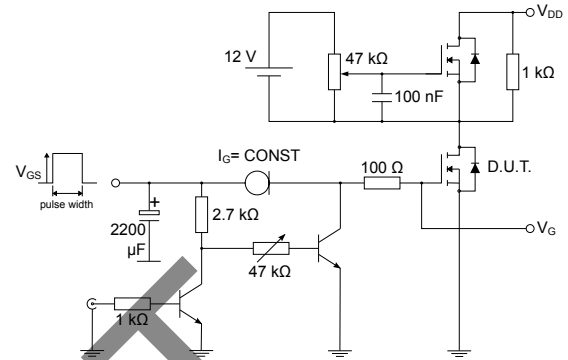
Figure 11. Normalized $V_{(BR)DSS}$ vs temperature



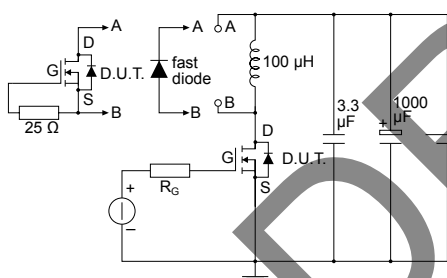
3 Test circuits

Figure 12. Test circuit for resistive load switching times


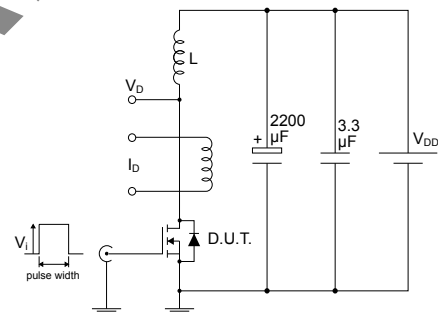
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Figure 13. Test circuit for gate charge behavior


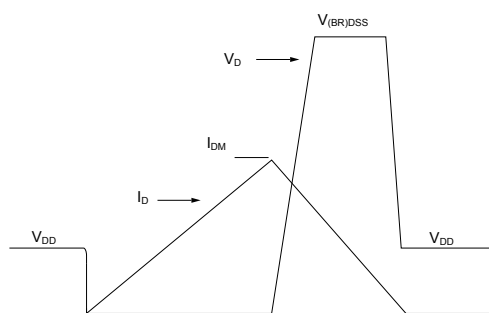
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Figure 14. Test circuit for inductive load switching and diode recovery times


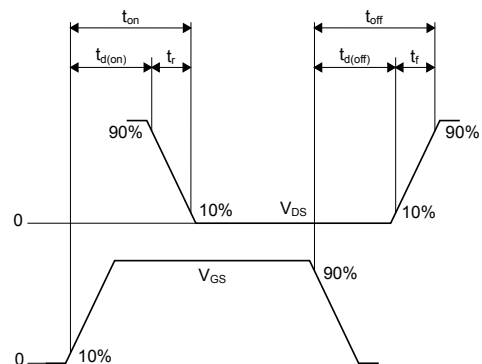
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Figure 15. Unclamped inductive load test circuit


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Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


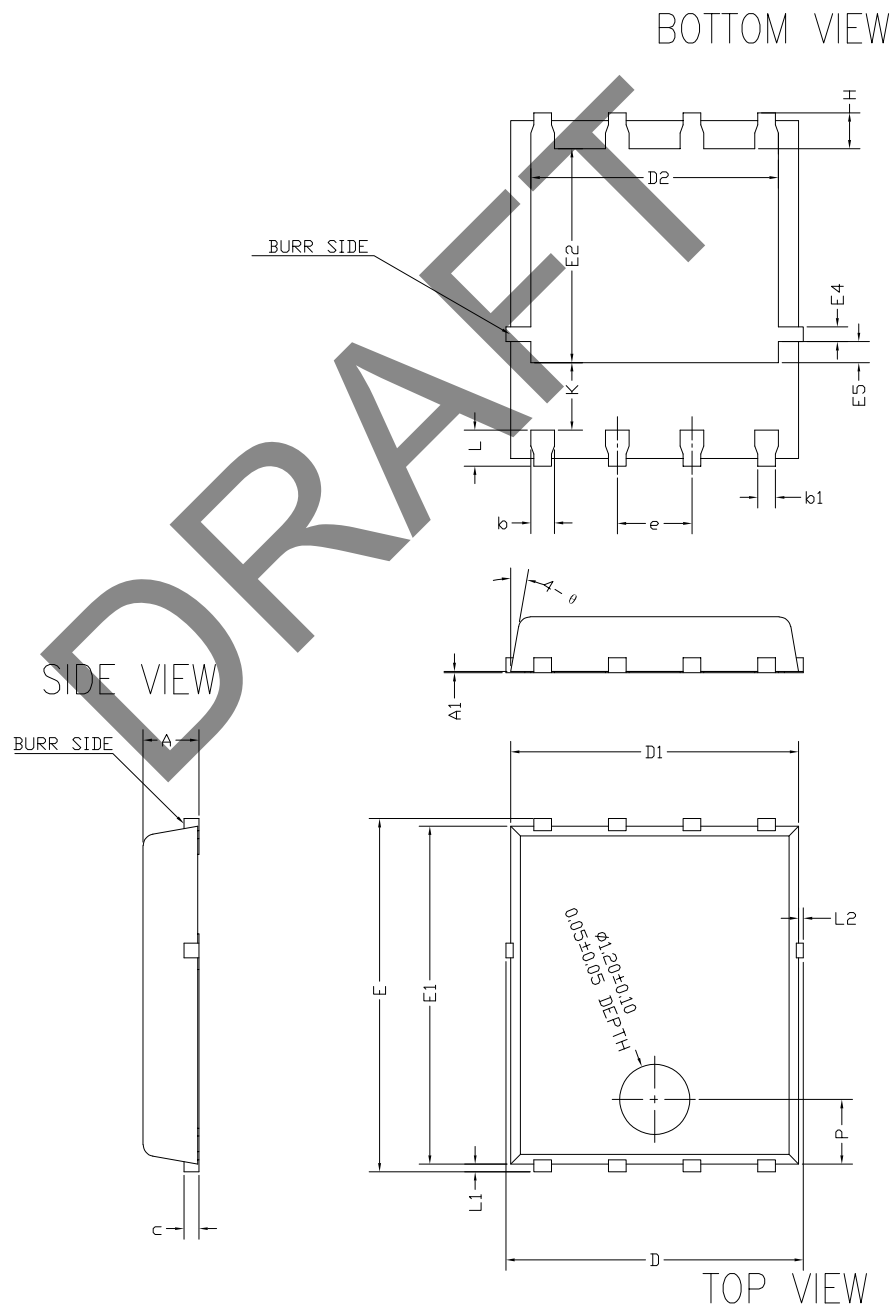
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 type B package information

Figure 18. PowerFLAT 5x6 type B package outline

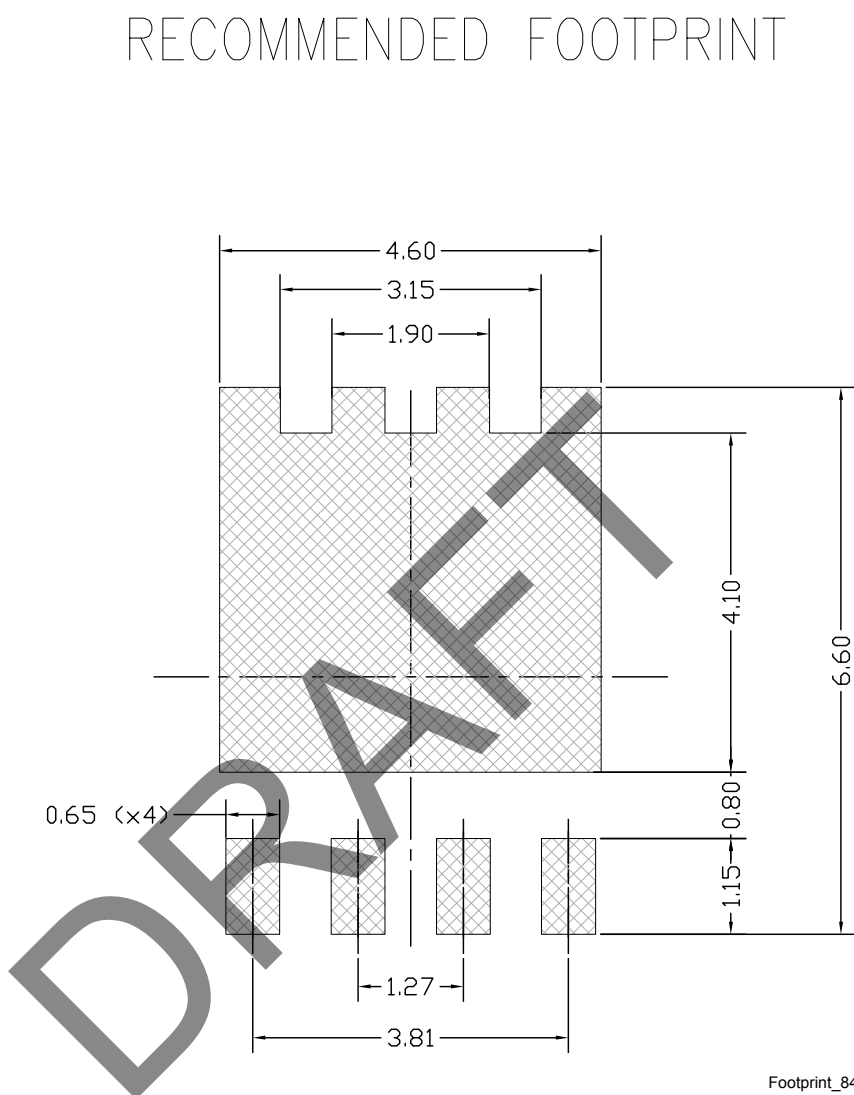


Drawing_8472137_typeB rev5

Table 7. PowerFLAT 5x6 type B mechanical data

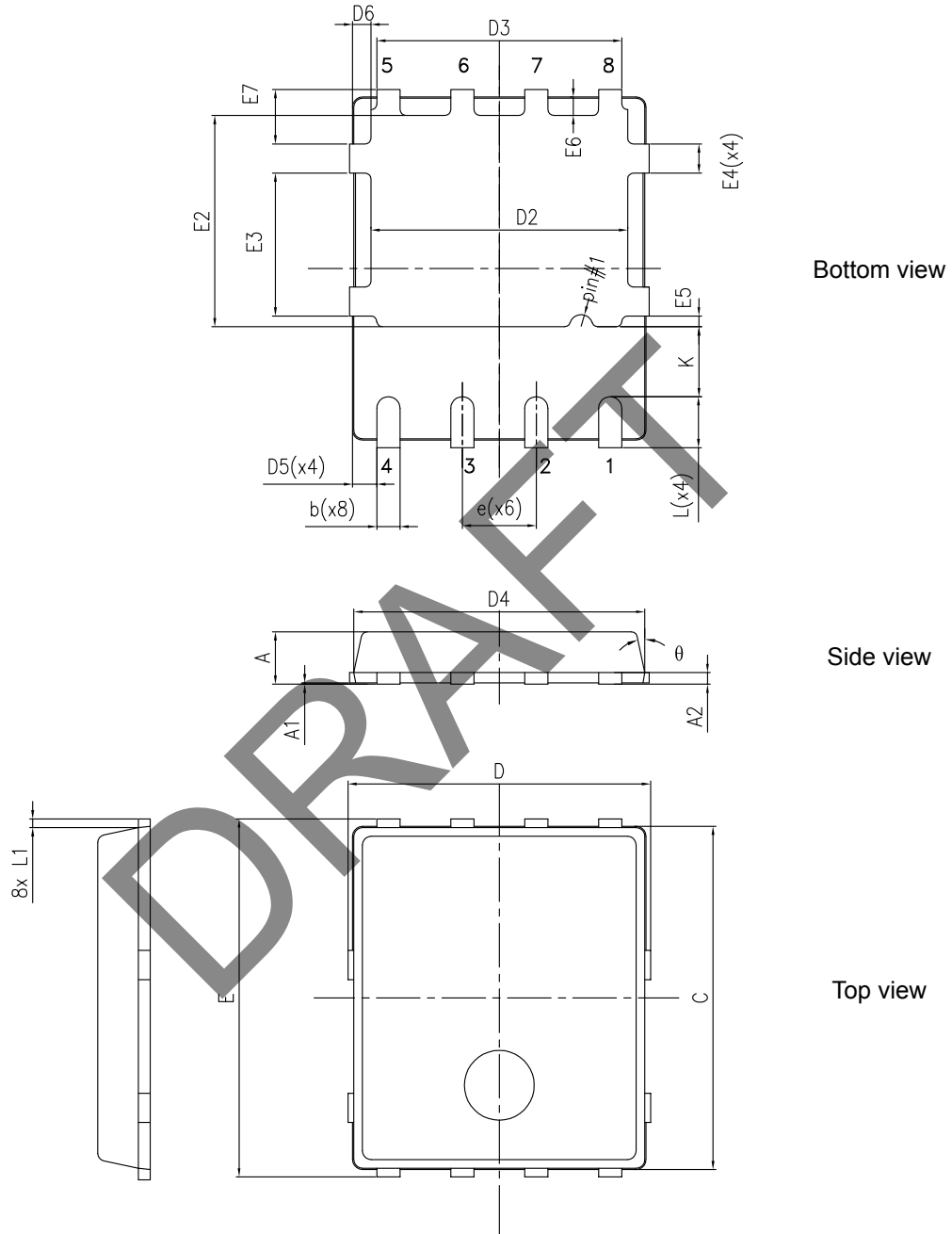
Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D	4.80		5.10
D1	4.80	4.90	5.00
D2	4.01	4.21	4.31
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.54	3.64	3.74
E4	0.15	0.25	0.35
E5	0.26	0.36	0.46
H	0.51	0.61	0.71
K	0.95		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

Figure 19. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT 5x6 type C package information

Figure 20. PowerFLAT 5x6 type C package outline

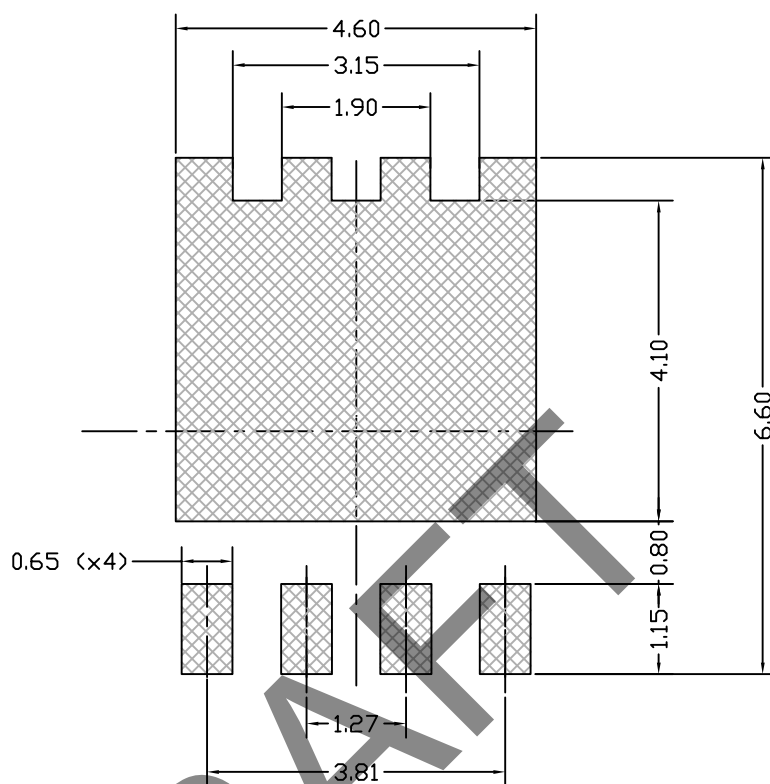


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Table 8. PowerFLAT 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

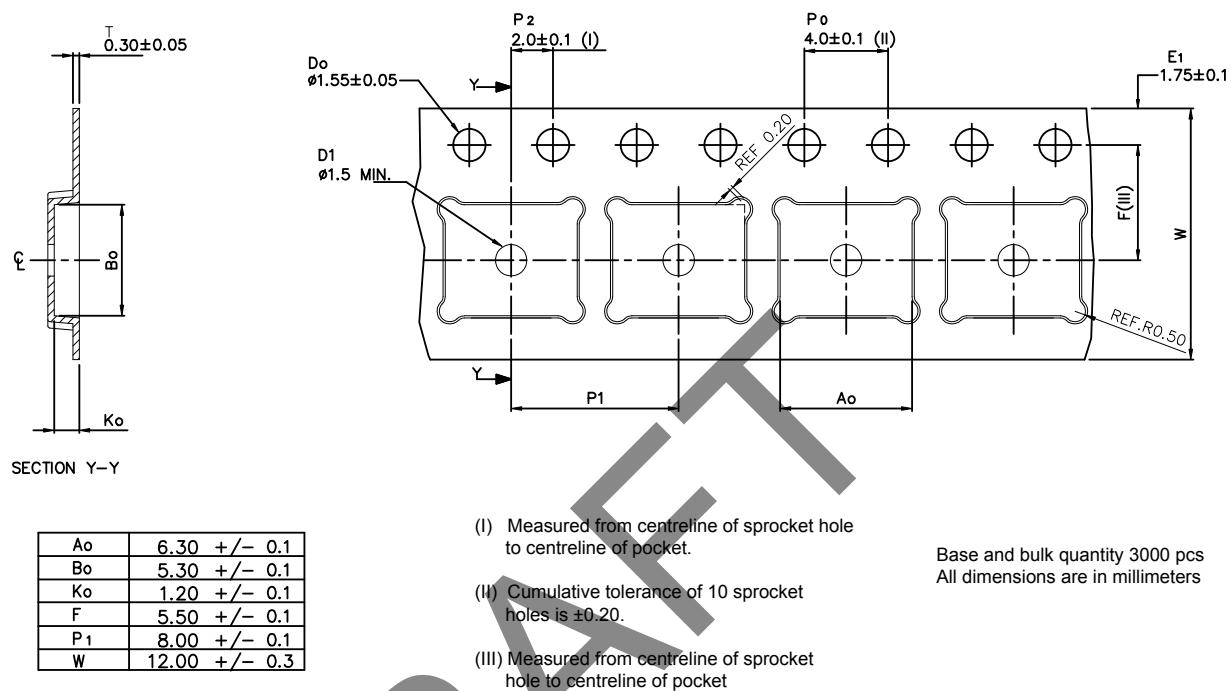
Figure 21. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



8231817_FOOTPRINT_simp_Rev_20

4.3 PowerFLAT 5x6 packing information

Figure 22. PowerFLAT 5x6 tape (dimensions are in mm)



8234350_Tape_rev_C

Figure 23. PowerFLAT 5x6 package orientation in carrier tape

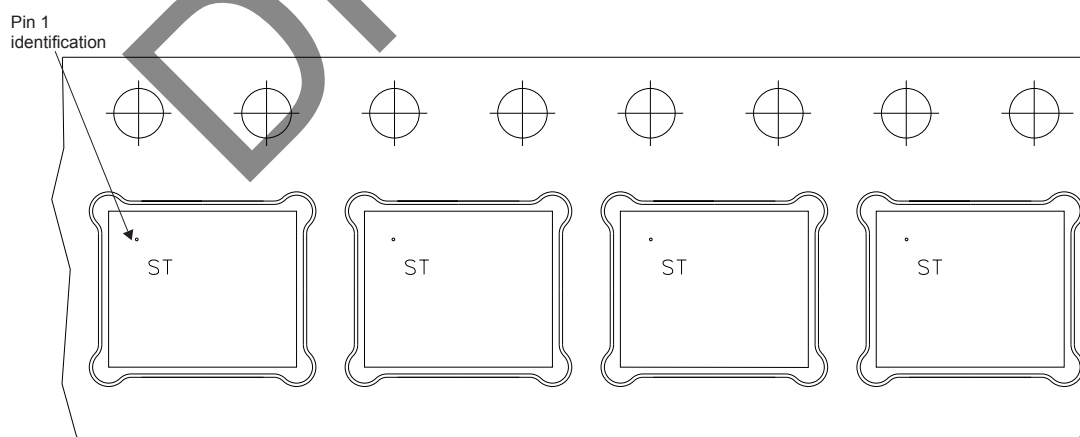
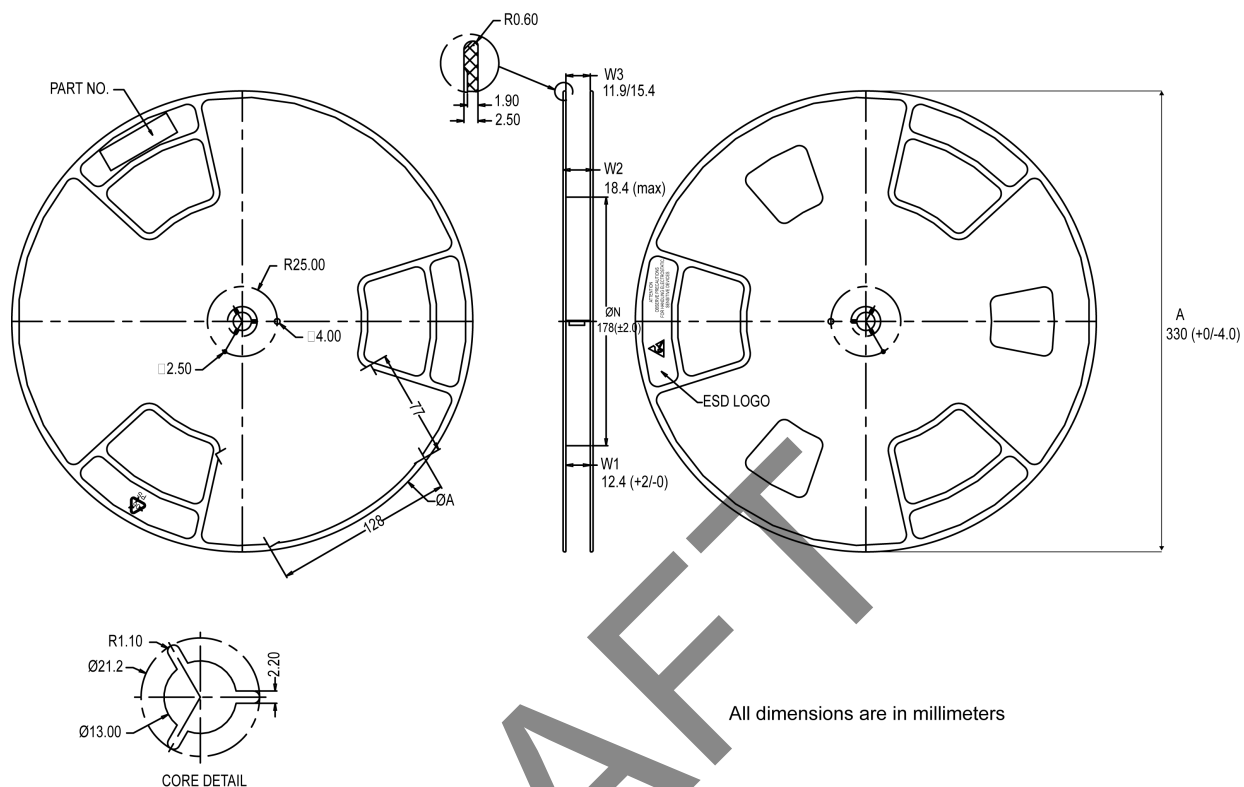


Figure 24. PowerFLAT 5x6 reel



8234350_Reel_rev_C

Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Jun-2014	1	First release.
22-Sep-2014	2	Updated title, features and description in cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "On /off states"</i> , <i>Table 5: "Dynamic"</i> , <i>Table 6: "Switching times"</i> and <i>Table 7: "Source-drain diode"</i> . Added <i>Section 3: "Electrical characteristics (curves)"</i> .
14-Jan-2015	3	Document status promoted from preliminary to production data.
02-May-2017	4	Modified title and features table on cover page. Modified <i>Table 1. Absolute maximum ratings</i> , <i>Table 3. On /off states</i> , <i>Table 4. Dynamic</i> , <i>Table 5. Switching times</i> and <i>Table 6. Source-drain diode</i> . Modified <i>Section 2.1 Electrical characteristics (curves)</i> . Minor text changes.
15-Jul-2022	5	Inserted Section 4.1 PowerFLAT 5x6 type B package information . Minor text changes.

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PCI Title : STL220N6F7 (OD68): Datasheet Updated

PCI Reference : ADG/22/13595

Subject : Public Products List

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STL220N6F7		
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