PRODUCT / PROCESS CHANGE INFORMATION

1. PCI basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCI No.	ADG/22/13511
1.3 Title of PCI	Die thickness change for ECMF4-2450A60N10
1.4 Product Category	ECMF4-2450A60N10
1.5 Issue date	2022-07-01

2. PCI Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Stephane CHAMARD
2.1.2 Marketing Manager	Philippe LEGER
2.1.3 Quality Manager	Jean-Paul REBRASSE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Wafer Fab (Process)	Backside finish modification except for wafer for sale: change final wafer thickness	STMicroelectronics Tours - France

4. Description of change		
	Old	New
4.1 Description	Thinnest die (part of ECMF4-2450A60N10) is of 90µm thickness.	Increase the thickness of the thinnest die (part of ECMF4-2450A60N10) from 90µm to 125µm.
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No	

5. Reason / motivation for change	
5.1 Motivation	In the frame of production yields optimization, STMicroelectronics has decided to increase the thickness of the thinnest die (part of ECMF4-2450A60N10) from 90µm to 125µm. New die thickness is already qualified for other product ECMF4-40A100N10 (directly qualified with this new 125µm thickness).
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Traceability of the change will be ensured by Finished Good/Type print on carton labels.

7. Timing / schedule	
7.1 Date of qualification results	2022-06-20
7.2 Intended start of delivery	2022-10-07
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13511 18054QRP v2.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2022-07-01

9. Attachments (additional documentations)
13511 Public product.pdf 13511 ECMF4-2450A60N10 die thickness.pdf 13511 18054QRP v2.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	ECMF4-2450A60N10	

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Qualification Report

ECMF4-2450A60N10

General Information	
Product Line	*IPAD*
Product Description	*Common mode filter with ESD protection for High Speed Serial interface*
Product Perimeter	*ECMF4-2450A60N10*
Product Group	*ADG*
Product Division	*Discrete & Filter*
Packages	*QFN 2.2 x 1.35*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST Tours (FRANCE)*
Assembly Plant	*ST Subcontractor 996H (CHINA)*
Reliability Lab	*ST TOURS – FRANCE*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
0.1	11-07-2018	8	Olivier CHAVANON	Aude DROMEL	Preliminary Report
1.0	01-08-2018	8	Olivier CHAVANON	Julien MICHELON	Initial Release
2.0	24-06-2022	13	Timothée PINGAULT	Julien Michelon Digitally signed by Julien Michelon Date: 2022.06.28 11:37:16 +02'00'	Qualification of change : increased thickness of the ESD die.

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

AC	Autoclave
Alt	Alternative test
EV	External Visual
GD	Generic Data
HTRB	High Temperature Reverse Bias
MSL	Moisture Sensitivity Level
PC	Preconditioning
PD	Physical Dimensions
PV	Parametric Verification
SD	Solderability test
SS	Sample Size
TC	Temperature Cycling
THB	Temperature Humidity Bias

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify ECMF4-2450A60N10 product, Common mode filter with ESD protection for High Speed Serial interface embedded in QFN 2.2 x 1.35 package.

This report has also been updated in order to include the qualification of the change PCI: ADG/22/13511, which increases the ESD die thickness to 125µm (from 90µm).

Item	Before	After
ADG/22/13511	ESD die thickness = 90µm	ESD die thickness = 125µm

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology ».

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- AC, THB to check the robustness to corrosion and the good package hermeticity.
- Solderability to check compatibility of package with customer assembly.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

Based on these results, ECMF4-2450A60N10 reliability assessment is compliant.

4 DEVICE CHARACTERISTICS

4.1 Device description

Refer to product datasheet:

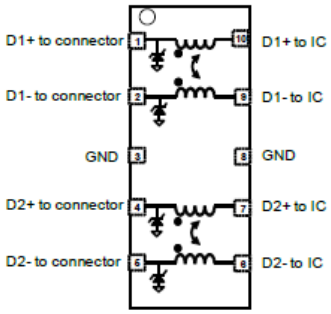
life.augmented

ECMF4-2450A60N10

Datasheet

Common mode filter with ESD protection for high speed serial interface

µQFN-10L
1.35 mm x 2.2 mm x 0.5 mm



Product status
ECMF4-2450A60N10

Features

- 6.4 GHz differential bandwidth to comply with HDMI 2.1, HDMI 2.0, HDMI 1.4, USB 4, USB 3.2 Gen 1 and Gen 2, MIPI, display port, etc.
- High common mode attenuation on WLAN frequencies :
  - From - 30 dB to - 33 dB at 2.4 – 2.47 GHz: Wi-Fi CH1-14 frequencies
  - From - 20 dB to - 15 dB at 5.18 – 5.82 GHz: Wi-Fi CH36-165 frequencies
- Very low PCB space consumption
- Thin package: 0.5 mm max.
- Lead free and RoHS package
- High reduction of parasitic elements through integration
- Exceeds IEC 61000-4-2 level 4 standards:
  - ±25 kV (air discharge)
  - ±10 kV (contact discharge)

Applications

- Notebook, laptop
- Streaming box
- Set top box
- Portable devices
- Tablet

Description

The ECMF4-2450A60N10 is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like HDMI 2.1, HDMI 2.0, HDMI1.4, USB 4, USB 3.2 Gen 1 and Gen 2, ethernet, MIPI, display port and other high speed serial interfaces.

It has a very large differential bandwidth to comply with these standards and can also protect and filter 2 differential lanes.

4.2 Construction Note

	ECMF4-2450A60N10
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS (FRANCE)
Technology / Process family	IPAD CMF
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS (FRANCE)
Assembly information	
Assembly site	ST SUBCONTRACTOR 996H (CHINA)
Package description	QFN 2.2 x 1.35
Molding compound	ECOPACK®2 (“Halogen-free”) molding compound
Lead finishing material	NiPdAu
Final testing information	
Testing location	ST SUBCONTRACTOR 996H (CHINA)

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Wafer fab location	Assy plant Location	Comments
L1	ECMF4-2450A60N10	FPN 2.2x1.35	ST Tours	ST Subcontractor - CHINA	Qualification lots
L2					
L3					
L4					Lot used for parametric, ESD and dimension verification after small die thickness increase
GD1	ECMF4-2450A17M10	FPN 2.6 x 1.35			Generic data: same die technology, same package technology, same assembly plant
GD2	HSP053-4M5	FPN 1.3x0.8			Generic data: same die technology, same package technology, same assembly plant
GD3	HSP053-4M5				
GD4	HSP053-4M5				
GD5	EMIF08-LCD04M16	FPN 3.3x1.35			Generic data: same package technology, same assembly plant
GD6	ECMF4-2459A6M10Y	FPN 2.6 x 1.35	ST Tours	ST Subcontractor - MALAYSIA	Generic data : same die attach material, same die attach thickness, same ESD die size, similar lead-frame but thicker ESD die. Can be used as similarity for ESD die thickness change.
GD7					
GD8					

GD: Test vehicles used for similarity.

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL	X
MSL research	MSL	J-STD-020	GD1	30		X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L1, L4	2	To confirm correct behavior of 125µm small die thickness	X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	GD2, GD3, GD4	231	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A	Lx or GDx	xx		
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for PowerMOSFET – IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104	GD1, GD6, GD7, GD8	77		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET – IGBT only. Alternative to TCHT	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101	Lx or GDx	xx		
Autoclave	AC	JESD22A-102	L1, L2, L3	75	Alternative to UHAST	X
Highly Accelerated Stress Test	HAST	JESD22A-110				
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	GD2, GD3, GD4	74		X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	
Power and Temperature Cycle	PTC	JED22A-105	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if $\Delta Tj>100°C$ cannot be achieved with IOL Alternative to IOL	
ESD Characterization	ESD HBM	JEDEC JS-001-2017	L1, L2, L3, L4	42		X
ESD Characterization	ESD HBM	IEC61000-4-2 (contact)	L1, L2, L3, L4	98		X
ESD Characterization	ESD CDM	AEC Q101-001 and 005		xx		
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	Lx or GDx	xx	After H3TRB and TC	
Physical Dimension	PD	JESD22B-100	L4	30		X
Terminal Strength	TS	MIL-STD-750 Method 2036	Lx or GDx	xx	Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	Lx or GDx	xx	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102	GD5	40		X
Dead Bug Test	DBT	ST Internal specification	Lx or GDx	xx	Mandatory for SMD package Data collection for PTH package	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	Lx or GDx	xx	Required in case of process change.	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
					Not applicable to protection device as no limit specified in the datasheet	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	Lx or GDx	xx	Covered during workability trials	
Bond Shear	BS	AEC-Q101-003	Lx or GDx	xx	Covered during workability trials	
Die Shear	DS	MIL-STD-750 Method 2017	Lx or GDx	xx	Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET - IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201	Lx or GDx			
Early Life Failure Rate	ELFR	JESD74	Lx or GDx	xx	Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,...)	FT	Internal specification	Lx or GDx	xx		
Repetitive Surge	RS	Internal specification	Lx or GDx	xx	Required for protection devices only.	

Low Temperature Storage	LTS	JESD-22 A119: 209	Lx or GDx	xx	AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27	Lx or GDx	xx	AQG324 test for Modules	
Vibration	V	IEC60068-2-6	Lx or GDx	xx	AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS											
						L1	L2	L3	L4	GD 1	GD 2	GD 3	GD 4	GD 5	GD 6	GD 7	GD 8
Pre- and Post-Electrical Test		ST datasheet	Ir, Vf,parameters following product datasheet	-		0/760											
MSL research	Y	JESD22-A113	Reflow=3 Temperature=85°C Humidity (HR)=85%	168h	30					0/ 30							
External Visual		JESD22 B-101	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process														
Parametric Verification		ST datasheet	Over part temperature range (note 1)		2	Refer to paragraph 6.2 in Annexes											
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=150°C VR= 3.6V	1Khrs	231					0/ 77	0/ 77	0/ 77					
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	500cy	308				0/ 77						0/ 77	0/ 77	0/ 77
AC (Alt to UHAST)	Y	JESD22 A-102	121°C; 100% RH 2bar	96hrs	75	0/ 25	0/ 25	0/ 25									
H3TRB (Alt to HAST)	Y	JESD22 A-101	85°C; 85% RH VR=3.6V	1Khrs	74						0/ 24	0/ 24	0/ 24				
ESD		JEDEC JS-001-2017	ESD HBM, refer to annex 6.1	-	42	0/ 30			0/ 12								
ESD		IEC61000-4-2 (contact)	ESD surge, refer to annex 6.1	-	98	0/ 30	0/ 30	0 /30	0/ 8								
SD	N	J-STD-002 JESD22 B-102	Wet ageing SnPb bath 220°C	-	10									0/ 10			
	N		Dry ageing SnPb bath 220°C	-	10									0/ 10			
	N		Wet ageing SnAgCu bath 245°C	-	10									0/ 10			
	N		Dry ageing SnAgCu bath 245°C	-	10									0/ 10			

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers."

6 ANNEXES

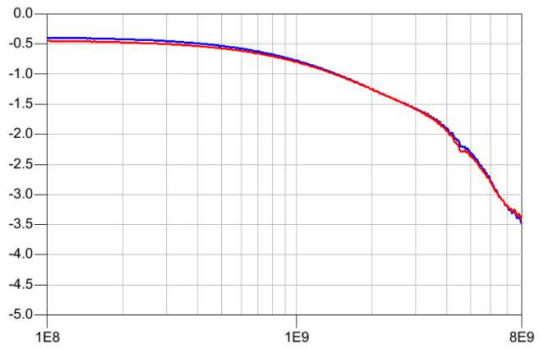
6.1 ESD

	Lot 1	Lot 2	Lot 3	Lot 4
ESD die thickness	90µm	90µm	90µm	125µm
Temperature	25°C	25°C	25°C	25°C
ESD IEC61000-4-2	30 units	30 units	30 units	8 units
	>10kV	>10kV	>10kV	>10kV
ESD HBM JEDEC JS-001-2017	30 units			12 units
	>8kV			>8kV

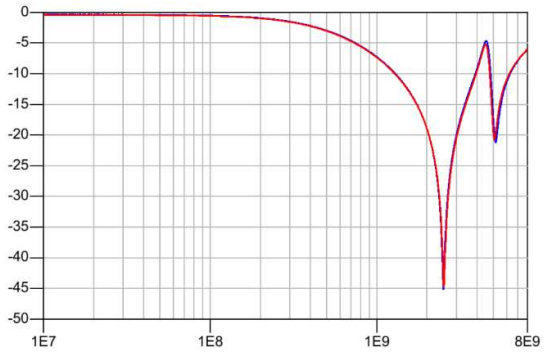
6.2 Comparative data

In order to ensure compliance of units with die thickness change to 125µm (from 90µm), comparative characteristics curves are provided. Compliance with datasheet is ensure for both 90µm and 125µm die thickness :

Legend :
- 90µm ESD die
- 125µm ESD die



Differential attenuation versus frequency



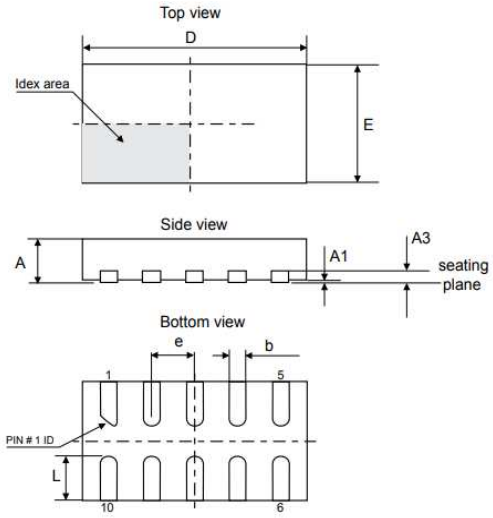
Common mode attenuation versus frequency

All parameters are compliant to ST datasheet limits.
These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet.

6.3 Physical Dimensions

Measurements done on Lot 4.

DIMENSION	A	A1	b	D	E	e	L
Min (mm)	**0.410**	**0.000**	**0.150**	**2.150**	**1.300**		**0.400**
Typ (mm)	**0.450**	**0.020**	**0.200**	**2.200**	**1.350**	**0.400**	**0.500**
Max (mm)	**0.500**	**0.050**	**0.250**	**2.250**	**1.400**		**0.600**
1	0.445	0.025	0.218	2.195	1.35	0.401	0.508
2	0.449	0.028	0.227	2.206	1.357	0.404	0.497
3	0.443	0.023	0.216	2.191	1.353	0.403	0.498
4	0.448	0.027	0.215	2.2	1.347	0.402	0.508
5	0.455	0.03	0.221	2.204	1.346	0.404	0.511
6	0.446	0.027	0.226	2.197	1.358	0.405	0.491
7	0.444	0.025	0.22	2.202	1.344	0.405	0.502
8	0.447	0.027	0.222	2.195	1.357	0.403	0.5
9	0.452	0.028	0.223	2.196	1.345	0.401	0.494
10	0.449	0.026	0.218	2.199	1.349	0.4	0.506
11	0.45	0.026	0.219	2.194	1.342	0.403	0.497
12	0.448	0.023	0.22	2.201	1.347	0.4	0.505
13	0.456	0.029	0.225	2.204	1.35	0.401	0.492
14	0.457	0.025	0.215	2.192	1.351	0.399	0.495
15	0.446	0.024	0.223	2.202	1.352	0.401	0.493
16	0.442	0.025	0.225	2.199	1.355	0.405	0.511
17	0.452	0.026	0.222	2.201	1.343	0.403	0.504
18	0.456	0.026	0.22	2.193	1.353	0.405	0.493
19	0.451	0.023	0.227	2.204	1.343	0.402	0.505
20	0.443	0.02	0.22	2.192	1.356	0.398	0.508
21	0.45	0.019	0.219	2.208	1.341	0.397	0.505
22	0.456	0.028	0.221	2.198	1.345	0.393	0.496
23	0.445	0.02	0.222	2.203	1.348	0.406	0.492
24	0.459	0.021	0.219	2.193	1.354	0.399	0.5
25	0.453	0.019	0.226	2.207	1.35	0.402	0.498
26	0.451	0.023	0.221	2.197	1.346	0.403	0.501
27	0.455	0.025	0.224	2.206	1.356	0.396	0.49
28	0.458	0.025	0.219	2.19	1.344	0.405	0.492
29	0.445	0.021	0.228	2.201	1.349	0.402	0.489
30	0.452	0.022	0.227	2.202	1.355	0.403	0.501
MOY	**0.450**	**0.025**	**0.222**	**2.199**	**1.350**	**0.402**	**0.499**
σ	**0.005**	**0.003**	**0.004**	**0.005**	**0.005**	**0.003**	**0.007**
MIN	**0.442**	**0.019**	**0.215**	**2.190**	**1.341**	**0.393**	**0.489**
MAX	**0.459**	**0.030**	**0.228**	**2.208**	**1.358**	**0.406**	**0.511**
Cpk	**2.72**	**2.74**	**2.60**	**3.19**	**3.27**		**5.04**



6.4 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations. Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
AC Autoclave	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
SD Solderability	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.

PCI
Product/Process Change Information

Die thickness change for ECMF4-2450A60N10

Notification number:	ADG/22/13511	**Issue Date**	20-Jun-2022
Issued by	Isabelle BALLON		
Product series affected by the change		ECMF4-2450A60N10	

Reason for change

In the frame of production yields optimization, STMicroelectronics has decided to increase the thickness of the thinnest die (part of ECMF4-2450A60N10) from 90µm to 125µm.

New die thickness is already qualified for other product ECMF4-40A100N10 (directly qualified with this new 125µm thickness).

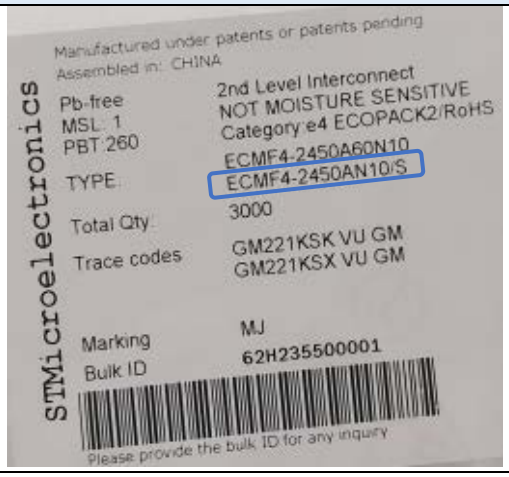
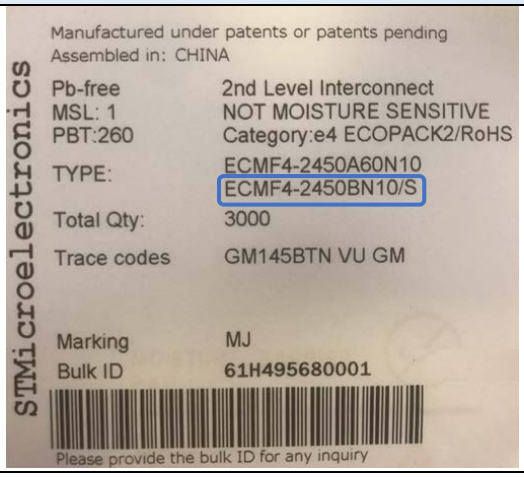
Effects of change

With this optimization of die thickness and yields, STMicroelectronics will improve its production outputs to better serve its customers.
The changed product does not present modified electrical, dimensional, or thermal parameters, leaving unchanged the current information (including marking) published in the product datasheet.

Product identification and traceability

Traceability of the change will be ensured by Finished Good/Type print on carton labels.

Commercial part number/Order code	Former Finished Good/Type	New Finished Good/Type
ECMF4-2450A60N10	ECMF4-2450**A**60N10/S	ECMF4-2450**B**60N10/S

Former Label	New Label
	

Qualification complete date	Week 25-2022

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Protection	ASIP	ECMF4-2450A60N10	Week 27-2022

For sample(s) request, please inform FSE (Field Sales Engineer) to insert corresponding **Non-Standard Samples Order** with **PCI reference** into remarks of order.

Change implementation schedule

Sales type	Estimated production start	Estimated first shipments
ECMF4-2450A60N10	**Week 27-2022**	**Week 40-2022**

Delivery of the current product version will continue until the stock last.

Qualification Report

ECMF4-2450A60N10

General Information	
Product Line	*IPAD*
Product Description	*Common mode filter with ESD protection for High Speed Serial interface*
Product Perimeter	*ECMF4-2450A60N10*
Product Group	*ADG*
Product Division	*Discrete & Filter*
Packages	*QFN 2.2 x 1.35*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST Tours (FRANCE)*
Assembly Plant	*ST Subcontractor 996H (CHINA)*
Reliability Lab	*ST TOURS – FRANCE*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
0.1	11-07-2018	8	Olivier CHAVANON	Aude DROMEL	Preliminary Report
1.0	01-08-2018	8	Olivier CHAVANON	Julien MICHELON	Initial Release
2.0	24-06-2022	13	Timothée PINGAULT	Julien Michelon Digitally signed by Julien Michelon Date: 2022.06.28 11:37:16 +02'00'	Qualification of change : increased thickness of the ESD die.

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

AC	Autoclave
Alt	Alternative test
EV	External Visual
GD	Generic Data
HTRB	High Temperature Reverse Bias
MSL	Moisture Sensitivity Level
PC	Preconditioning
PD	Physical Dimensions
PV	Parametric Verification
SD	Solderability test
SS	Sample Size
TC	Temperature Cycling
THB	Temperature Humidity Bias

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify ECMF4-2450A60N10 product, Common mode filter with ESD protection for High Speed Serial interface embedded in QFN 2.2 x 1.35 package.

This report has also been updated in order to include the qualification of the change PCI: ADG/22/13511, which increases the ESD die thickness to 125µm (from 90µm).

Item	Before	After
ADG/22/13511	ESD die thickness = 90µm	ESD die thickness = 125µm

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology ».

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- AC, THB to check the robustness to corrosion and the good package hermeticity.
- Solderability to check compatibility of package with customer assembly.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

Based on these results, ECMF4-2450A60N10 reliability assessment is compliant.

4 DEVICE CHARACTERISTICS

4.1 Device description

Refer to product datasheet:

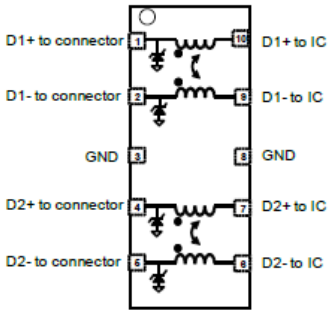
life.augmented

ECMF4-2450A60N10

Datasheet

Common mode filter with ESD protection for high speed serial interface

µQFN-10L
1.35 mm x 2.2 mm x 0.5 mm



Product status
ECMF4-2450A60N10

Features

- 6.4 GHz differential bandwidth to comply with HDMI 2.1, HDMI 2.0, HDMI 1.4, USB 4, USB 3.2 Gen 1 and Gen 2, MIPI, display port, etc.
- High common mode attenuation on WLAN frequencies :
  - From - 30 dB to - 33 dB at 2.4 – 2.47 GHz: Wi-Fi CH1-14 frequencies
  - From - 20 dB to - 15 dB at 5.18 – 5.82 GHz: Wi-Fi CH36-165 frequencies
- Very low PCB space consumption
- Thin package: 0.5 mm max.
- Lead free and RoHS package
- High reduction of parasitic elements through integration
- Exceeds IEC 61000-4-2 level 4 standards:
  - ±25 kV (air discharge)
  - ±10 kV (contact discharge)

Applications

- Notebook, laptop
- Streaming box
- Set top box
- Portable devices
- Tablet

Description

The ECMF4-2450A60N10 is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like HDMI 2.1, HDMI 2.0, HDMI1.4, USB 4, USB 3.2 Gen 1 and Gen 2, ethernet, MIPI, display port and other high speed serial interfaces.

It has a very large differential bandwidth to comply with these standards and can also protect and filter 2 differential lanes.

4.2 Construction Note

	ECMF4-2450A60N10
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS (FRANCE)
Technology / Process family	IPAD CMF
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST TOURS (FRANCE)
Assembly information	
Assembly site	ST SUBCONTRACTOR 996H (CHINA)
Package description	QFN 2.2 x 1.35
Molding compound	ECOPACK®2 (“Halogen-free”) molding compound
Lead finishing material	NiPdAu
Final testing information	
Testing location	ST SUBCONTRACTOR 996H (CHINA)

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Wafer fab location	Assy plant Location	Comments
L1	ECMF4-2450A60N10	FPN 2.2x1.35	ST Tours	ST Subcontractor - CHINA	Qualification lots
L2					
L3					
L4					Lot used for parametric, ESD and dimension verification after small die thickness increase
GD1	ECMF4-2450A17M10	FPN 2.6 x 1.35			Generic data: same die technology, same package technology, same assembly plant
GD2	HSP053-4M5	FPN 1.3x0.8			Generic data: same die technology, same package technology, same assembly plant
GD3	HSP053-4M5				
GD4	HSP053-4M5				
GD5	EMIF08-LCD04M16	FPN 3.3x1.35			Generic data: same package technology, same assembly plant
GD6	ECMF4-2459A6M10Y	FPN 2.6 x 1.35	ST Tours	ST Subcontractor - MALAYSIA	Generic data : same die attach material, same die attach thickness, same ESD die size, similar lead-frame but thicker ESD die. Can be used as similarity for ESD die thickness change.
GD7					
GD8					

GD: Test vehicles used for similarity.

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL	X
MSL research	MSL	J-STD-020	GD1	30		X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L1, L4	2	To confirm correct behavior of 125µm small die thickness	X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	GD2, GD3, GD4	231	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A	Lx or GDx	xx		
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for PowerMOSFET – IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104	GD1, GD6, GD7, GD8	77		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET – IGBT only. Alternative to TCHT	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101	Lx or GDx	xx		
Autoclave	AC	JESD22A-102	L1, L2, L3	75	Alternative to UHAST	X
Highly Accelerated Stress Test	HAST	JESD22A-110				
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	GD2, GD3, GD4	74		X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	
Power and Temperature Cycle	PTC	JED22A-105	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if $\Delta Tj>100°C$ cannot be achieved with IOL Alternative to IOL	
ESD Characterization	ESD HBM	JEDEC JS-001-2017	L1, L2, L3, L4	42		X
ESD Characterization	ESD HBM	IEC61000-4-2 (contact)	L1, L2, L3, L4	98		X
ESD Characterization	ESD CDM	AEC Q101-001 and 005		xx		
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	Lx or GDx	xx	After H3TRB and TC	
Physical Dimension	PD	JESD22B-100	L4	30		X
Terminal Strength	TS	MIL-STD-750 Method 2036	Lx or GDx	xx	Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	Lx or GDx	xx	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102	GD5	40		X
Dead Bug Test	DBT	ST Internal specification	Lx or GDx	xx	Mandatory for SMD package Data collection for PTH package	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	Lx or GDx	xx	Required in case of process change.	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
					Not applicable to protection device as no limit specified in the datasheet	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	Lx or GDx	xx	Covered during workability trials	
Bond Shear	BS	AEC-Q101-003	Lx or GDx	xx	Covered during workability trials	
Die Shear	DS	MIL-STD-750 Method 2017	Lx or GDx	xx	Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET - IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201	Lx or GDx			
Early Life Failure Rate	ELFR	JESD74	Lx or GDx	xx	Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,...)	FT	Internal specification	Lx or GDx	xx		
Repetitive Surge	RS	Internal specification	Lx or GDx	xx	Required for protection devices only.	

Low Temperature Storage	LTS	JESD-22 A119: 209	Lx or GDx	xx	AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27	Lx or GDx	xx	AQG324 test for Modules	
Vibration	V	IEC60068-2-6	Lx or GDx	xx	AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS											
						L1	L2	L3	L4	GD 1	GD 2	GD 3	GD 4	GD 5	GD 6	GD 7	GD 8
Pre- and Post-Electrical Test		ST datasheet	Ir, Vf,parameters following product datasheet	-		0/760											
MSL research	Y	JESD22-A113	Reflow=3 Temperature=85°C Humidity (HR)=85%	168h	30					0/ 30							
External Visual		JESD22 B-101	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process														
Parametric Verification		ST datasheet	Over part temperature range (note 1)		2	Refer to paragraph 6.2 in Annexes											
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=150°C VR= 3.6V	1Khrs	231					0/ 77	0/ 77	0/ 77					
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	500cy	308				0/ 77						0/ 77	0/ 77	0/ 77
AC (Alt to UHAST)	Y	JESD22 A-102	121°C; 100% RH 2bar	96hrs	75	0/ 25	0/ 25	0/ 25									
H3TRB (Alt to HAST)	Y	JESD22 A-101	85°C; 85% RH VR=3.6V	1Khrs	74						0/ 24	0/ 24	0/ 24				
ESD		JEDEC JS-001-2017	ESD HBM, refer to annex 6.1	-	42	0/ 30			0/ 12								
ESD		IEC61000-4-2 (contact)	ESD surge, refer to annex 6.1	-	98	0/ 30	0/ 30	0 /30	0/ 8								
SD	N	J-STD-002 JESD22 B-102	Wet ageing SnPb bath 220°C	-	10									0/ 10			
	N		Dry ageing SnPb bath 220°C	-	10									0/ 10			
	N		Wet ageing SnAgCu bath 245°C	-	10									0/ 10			
	N		Dry ageing SnAgCu bath 245°C	-	10									0/ 10			

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers."

6 ANNEXES

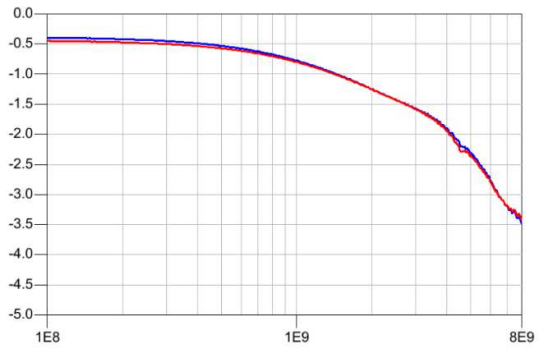
6.1 ESD

	Lot 1	Lot 2	Lot 3	Lot 4
ESD die thickness	90µm	90µm	90µm	125µm
Temperature	25°C	25°C	25°C	25°C
ESD IEC61000-4-2	30 units	30 units	30 units	8 units
	>10kV	>10kV	>10kV	>10kV
ESD HBM JEDEC JS-001-2017	30 units			12 units
	>8kV			>8kV

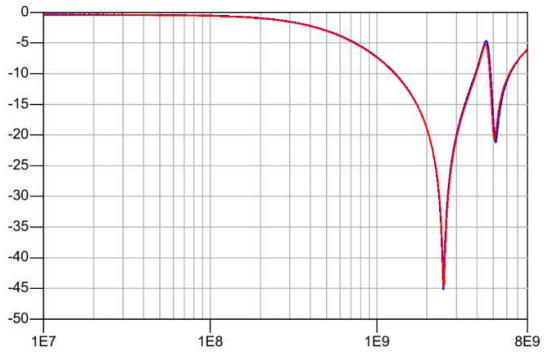
6.2 Comparative data

In order to ensure compliance of units with die thickness change to 125µm (from 90µm), comparative characteristics curves are provided. Compliance with datasheet is ensure for both 90µm and 125µm die thickness :

Legend :
- 90µm ESD die
- 125µm ESD die



Differential attenuation versus frequency



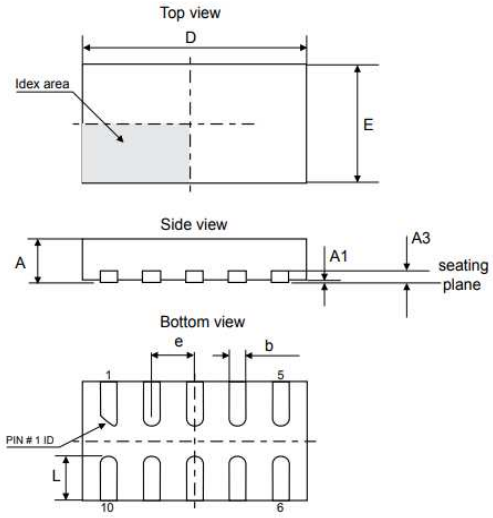
Common mode attenuation versus frequency

All parameters are compliant to ST datasheet limits.
These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet.

6.3 Physical Dimensions

Measurements done on Lot 4.

DIMENSION	A	A1	b	D	E	e	L
Min (mm)	**0.410**	**0.000**	**0.150**	**2.150**	**1.300**		**0.400**
Typ (mm)	**0.450**	**0.020**	**0.200**	**2.200**	**1.350**	**0.400**	**0.500**
Max (mm)	**0.500**	**0.050**	**0.250**	**2.250**	**1.400**		**0.600**
1	0.445	0.025	0.218	2.195	1.35	0.401	0.508
2	0.449	0.028	0.227	2.206	1.357	0.404	0.497
3	0.443	0.023	0.216	2.191	1.353	0.403	0.498
4	0.448	0.027	0.215	2.2	1.347	0.402	0.508
5	0.455	0.03	0.221	2.204	1.346	0.404	0.511
6	0.446	0.027	0.226	2.197	1.358	0.405	0.491
7	0.444	0.025	0.22	2.202	1.344	0.405	0.502
8	0.447	0.027	0.222	2.195	1.357	0.403	0.5
9	0.452	0.028	0.223	2.196	1.345	0.401	0.494
10	0.449	0.026	0.218	2.199	1.349	0.4	0.506
11	0.45	0.026	0.219	2.194	1.342	0.403	0.497
12	0.448	0.023	0.22	2.201	1.347	0.4	0.505
13	0.456	0.029	0.225	2.204	1.35	0.401	0.492
14	0.457	0.025	0.215	2.192	1.351	0.399	0.495
15	0.446	0.024	0.223	2.202	1.352	0.401	0.493
16	0.442	0.025	0.225	2.199	1.355	0.405	0.511
17	0.452	0.026	0.222	2.201	1.343	0.403	0.504
18	0.456	0.026	0.22	2.193	1.353	0.405	0.493
19	0.451	0.023	0.227	2.204	1.343	0.402	0.505
20	0.443	0.02	0.22	2.192	1.356	0.398	0.508
21	0.45	0.019	0.219	2.208	1.341	0.397	0.505
22	0.456	0.028	0.221	2.198	1.345	0.393	0.496
23	0.445	0.02	0.222	2.203	1.348	0.406	0.492
24	0.459	0.021	0.219	2.193	1.354	0.399	0.5
25	0.453	0.019	0.226	2.207	1.35	0.402	0.498
26	0.451	0.023	0.221	2.197	1.346	0.403	0.501
27	0.455	0.025	0.224	2.206	1.356	0.396	0.49
28	0.458	0.025	0.219	2.19	1.344	0.405	0.492
29	0.445	0.021	0.228	2.201	1.349	0.402	0.489
30	0.452	0.022	0.227	2.202	1.355	0.403	0.501
MOY	**0.450**	**0.025**	**0.222**	**2.199**	**1.350**	**0.402**	**0.499**
σ	**0.005**	**0.003**	**0.004**	**0.005**	**0.005**	**0.003**	**0.007**
MIN	**0.442**	**0.019**	**0.215**	**2.190**	**1.341**	**0.393**	**0.489**
MAX	**0.459**	**0.030**	**0.228**	**2.208**	**1.358**	**0.406**	**0.511**
Cpk	**2.72**	**2.74**	**2.60**	**3.19**	**3.27**		**5.04**



6.4 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations. Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
AC Autoclave	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
SD Solderability	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder.	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finish.

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCI Title : Die thickness change for ECMF4-2450A60N10

PCI Reference : ADG/22/13511

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

ECMF4-2450A60N10		

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