

PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data

1.1 Company		STMicroelectronics International N.V
1.2 PCN No.		ADG/21/13047
1.3 Title of PCN		Wafer Manufacturing & EWS capacity extension in ST Singapore for Automotive SiC 650V products
1.4 Product Category		Automotive SiC 650V products
1.5 Issue date		2021-10-11

2. PCN Team

2.1 Contact supplier		
2.1.1 Name		ROBERTSON HEATHER
2.1.2 Phone		+1 8475853058
2.1.3 Email		heather.robertson@st.com
2.2 Change responsibility		
2.2.1 Product Manager		Stephane CHAMARD
2.1.2 Marketing Manager		Philippe LEGER
2.1.3 Quality Manager		Jean-Paul REBRASSE

3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication	ST Catania - Italy ST Singapore

4. Description of change

	Old	New
4.1 Description	ST Catania - Italy	ST Catania - Italy ST Singapore with Process rationalization for both plants
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No	

5. Reason / motivation for change

5.1 Motivation	In line with the commitment of ST Company to reinforce its leading position in the SiC Power Rectifiers market and to support strong SiC business increase, STMicroelectronics has decided to expand the manufacturing & EWS capacity of SiC 650V diodes. This additional wafer fab & EWS capacity will be done through production line located in the Singapore existing plant. ST is taking the opportunity to enhance and to standardize production flows using the same metallization and thicknesses for all SiC products.
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change

6.1 Description	Finished Good and plant code
-----------------	------------------------------

7. Timing / schedule

7.1 Date of qualification results	2021-10-04
7.2 Intended start of delivery	2022-04-08
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation

8.1 Description	13047 21072QRP.pdf
-----------------	--------------------

8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-10-11
---	----------------------------	-------------------	------------

9. Attachments (additional documentations)	
13047 Public product.pdf	
13047 Automotive SiC650V in ST Singapore.pdf	
13047 21072QRP.pdf	
13047 21074QRP.pdf	

10. Affected parts		
10.1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STPSC10065DY	
	STPSC10065GY-TR	
	STPSC10C065RY	
	STPSC10H065BY-TR	
	STPSC10H065DY	
	STPSC10H065GY-TR	
	STPSC12065DY	
	STPSC12065G2Y-TR	
	STPSC12065GY-TR	
	STPSC12C065DY	
	STPSC12H065DY	
	STPSC20065DY	
	STPSC20065GY-TR	
	STPSC20065WY	
	STPSC20H065CTY	
	STPSC20H065CWY	
	STPSC40065CWY	
	STPSC6H065BY-TR	
	STPSC8065DY	
	STPSC8H065BY-TR	
	STPSC8H065G2Y-TR	

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Subject to any contractual arrangement in force with you or to any industry standard implemented by us, STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved

Qualification Report

Wafer Manufacturing & EWS capacity extension in ST Singapore for Automotive 650V SiC diodes

General Information		Locations	
Product Line	Rectifiers	Wafer fab	ST SINGAPORE
Product Description	Silicon Carbide Power Schottky	Assembly plant	ST Shenzhen – CHINA Subcontractor 998G - CHINA
Product perimeter	Refer to list page 4	Reliability Lab	ST TOURS - FRANCE
Product Group	ADG	Reliability assessment	PASS
Product division	Discrete & Filter		
Package	DPAK, D ² PAK, TO-220AB, TO-220AC, I ² PAK, DO247, TO247, TO247LL		
Maturity level step	QUALIFIED		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	30-Sept-2021	16	Christophe GOIN	Julien MICHELON	Initial release. Linked to PCN 13047.

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1	APPLICABLE AND REFERENCE DOCUMENTS	3
2	GLOSSARY	3
3	RELIABILITY EVALUATION OVERVIEW.....	4
3.1	OBJECTIVES.....	4
3.2	CONCLUSION.....	4
4	DEVICE CHARACTERISTICS	5
4.1	DEVICE DESCRIPTION.....	5
4.2	CONSTRUCTION NOTE.....	8
5	TESTS RESULTS SUMMARY	10
5.1	TEST VEHICLES	10
5.2	TEST PLAN	11
5.3	RESULTS SUMMARY	13
6	ANNEXES	14
6.1	PARAMETRIC VERIFICATIONS	14
6.2	TESTS DESCRIPTION	16

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101 Rev.D1	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices
AEC-Q005	Pb-Free Test Requirements

2 GLOSSARY

SS	Sample Size
PC	Pre-Conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
H3TRB	High Humidity High Temperature Reverse Bias
IOLT	Intermittent Operating Life Test
UHAST	Unbiased Highly Accelerated Stress Test
GD	Generic Data
MSL	Moisture Sensitivity Level
T_j	Junction Temperature
BS	Bond Shear
DS	Die Shear
WBS	Wire Bond Strength
DPA	Destructive Physical Analysis (after TC and H3TRB)

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify wafer production & test for 650V Silicon Carbide Power Schottky Rectifier products in ST Singapore.

The involved products are listed in the table here below:

Product	Description	Package	Assembly Location	
STPSC6H065BY-TR	6 A, 650 V	DPAK	ST Shenzhen - China	
STPSC8H065BY-TR	8 A, 650 V			
STPSC10H065BY-TR	10 A, 650 V			
STPSC10H065GY-TR	10 A, 650 V			
STPSC20065GY-TR	20 A, 650 V	D ² PAK	ST Shenzhen - China	
STPSC8H065G2Y-TR	8 A, 650 V			
STPSC20065WY	20 A, 650 V	DO-247	Subcontractor – China (998G)	
STPSC20H065CWY	2x10 A, 650 V	TO-247		
STPSC40065CWY	2x20 A, 650 V			
STPSC20H065CTY	2x10 A, 650 V	TO-220AB		
STPSC10H065DY	10 A, 650 V	TO-220AC	Subcontractor – China (998G)	
STPSC6C065DY	6 A, 650 V			
STPSC20065DY	20 A, 650 V			
STPSC10C065RY	10 A, 650 V	I ² PAK	Subcontractor – China (998G)	
STPSC20H065CWLY	20 A, 650 V	TO247LL		

The reliability test methodology used follows the JESD47: « Stress Test riven Qualification Methodology » and AECQ-101 RevD1 guidelines.

The following reliability tests ensuing are:

- TC and IOLT to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

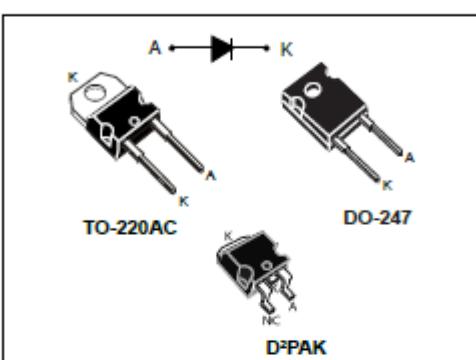
4.1 Device description

Refer to ST specification (examples below for STPSC20065-Y, STPSC10H065BY and STPSC20H065CWLY):

STPSC20065-Y

Automotive 650 V power Schottky silicon carbide diode

Datasheet - production data



Description

The SiC diode is an ultra high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Especially suited for use in PFC applications, this ST SiC diode will boost performance in hard switching conditions. Its high forward surge capability ensures good robustness during transient phases.

Features

- AEC-Q101 qualified
- No reverse recovery charge in application current range
- Switching behavior independent of temperature
- Dedicated to PFC applications
- High forward surge capability
- ECOPACK®2 compliant component
- PPAP capable
- Operating T_j from -40 °C to 175 °C

Table 1: Device summary

Symbol	Value
$I_{F(AV)}$	20 A
V_{RRM}	650 V
T_j (max.)	175 °C
V_F (typ.)	1.30 V

Automotive 650 V power Schottky silicon carbide diode



Features

- AEC-Q101 qualified
- No reverse recovery charge in application current range
- Switching behavior independent of temperature
- Recommended to PFC applications
- PPAP capable
- ECOPACK®2 compliant component

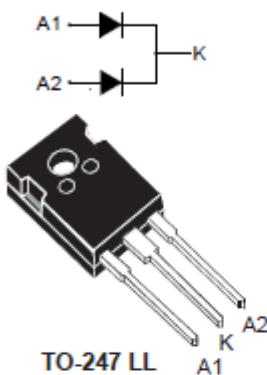
Description

The SiC diode is an ultra-high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Especially suited for use in PFC applications, this ST SiC diode will boost performance in hard switching conditions.

Product status	
STPSC10H065BY-TR	
Product summary	
Symbol	Value
$I_{F(AV)}$	10 A
V_{RRM}	650 V
$T_{J(max.)}$	175 °C

Automotive 20 A 650 V power Schottky silicon carbide diode



Features



- AEC-Q101 qualified
- PPAP capable
- No or negligible reverse recovery
- Switching behavior independent of temperature
- Dedicated to PFC applications
- High forward surge capability
- ECOPACK² compliant component

Applications

- On board charger (OBC)
- Charging stations
- PFC applications
- UPS
- Inverters
- Telecom power supplies

Description

The STPSC20H065CWLY is an ultra-high-performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature and are ideal for automotive applications.

Especially suited for use in PFC applications, UPS, inverters, telecom power supplies and battery chargers (either integrated in the vehicle or in a charging station), this diode will enhance the performance of the targeted application. Its high forward surge capability ensures a good robustness during transient phases.

Product status link	
STPSC20H065CWLY	
Product summary	
$I_{F(AV)}$	2 x 10 A
V_{RRM}	650 V
T_J (max.)	175 °C
V_F (typ.)	1.45 V
Product label	
	

4.2 Construction Note

STPSCxxH065BY-TR	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	DPAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSCxxH065GY-TR	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	D ² PAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20065WY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	DO-247
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CWY - STPSC40065CWY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-247
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CTY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-220AB
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSCxxH065DY - STPSCxx065DY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-220AC
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CWLY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST subcontractor – China (998G)
Package description	TO-247LL
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST subcontractor – China (998G)

STPSC10C065RY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	I ² PAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	STPSC10H065BY	DPAK	Qualification lot 1
L2	STPSC20065DY	TO220AC	Qualification lot 2
L3	STPSC10H065DY	TO220AC	Qualification lot 3
L4	STPSC20H065CWLY	TO247LL	Qualification lot 4

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard specification	All qualification parts tested per the requirements of the appropriate device specification			X
Pre-conditioning	PC	JESD22A-113	All qualification parts tested per the requirements of the appropriate device specification		As per targeted MSL	X
MSL research	MSL	J-STD-020	L1	30		X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	All qualification parts tested per the requirements of the appropriate device specification			X
High Temperature Storage Life	HTSL	JESD22B-101			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
High Temperature Gate Bias	HTGB	JESD22A-108			Required for PowerMOSFET – IGBT only.	
High Temperature Reverse Bias	HTRB	JESD22A-108	L1, L2, L4	231		X
High Temperature Forward Bias	HTFB	JESD22A-108			Not required, applicable only to LEDs	
High Temperature Operating Life Test	HTOL	JESD22A-108			Covered by HTRB.	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test B			Required for Voltage Regulator (Zener) only.	
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test A			Required for Thyristor only.	
Temperature Cycling	TC	JESD22A-104	L1, L2, L3, L4	308		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET – IGBT only.	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118	L1, L2, L4	231		X
Autoclave	AC	JESD22A-102			Not recommended	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1, L2, L4	231		X
High Temperature High Humidity Bias	HTHBB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	L1, L2, L3, L4	308	For power devices.	X
Power and Temperature Cycle	PTC	JED22A-105			Covered by IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005		120	For automotive products only	X
ESD Characterization	ESD CDM	AEC Q101-001 and 005		120	For automotive products only	X

Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	L1	4	After H3TRB and TC. For automotive products only	X
Physical Dimension	PD	JESD22B-100			Not relevant for wafer production and test qualification	
Terminal Strength	TS	MIL-STD-750 Method 2036			Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)			Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102			Not relevant for wafer production and test qualification	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate			Required in case of process change.	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	L1, L2, L3, L4	58	Covered during workability trials	X
Bond Shear	BS	AEC-Q101-003	L1, L2, L3, L4	58	Covered during workability trials	X
Die Shear	DS	MIL-STD-750 Method 2017	L1	10	Not Applicable to parts with solder paste die attach	X
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET – IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201			Not relevant for wafer production and test qualification	
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Low Temperature Storage	LTS	JESD-22 A119: 209			AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104			AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037			AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037			AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27			AQG324 test for Modules	
Vibration	V	IEC60068-2-6			AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.			
						Lot 1	Lot 2	Lot 3	Lot 4
Parametric Verifications		ST datasheet	Over part temperature range	120	-	Refer to paragraph 6.1 in Annexes			
External Visual Inspection		JESD22 B-101	-	1309	-	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process			
Pre and Post Electrical Test		ST datasheet	I _R , V _F parameters following product datasheet	1309	-	0/1309			
PC		JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	385	-	0/385			
MSL1 research	N	JESD22 A-113	MSL=1, Reflow=3 Temperature=85°C Humidity (HR)=85%	30	-	0/30			
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Junction Temperature=175°C Voltage=650V	231	1000h	0/77	0/77		0/77
TC	N	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-55°C	231	1000cy		0/77	0/77	0/77
	Y			77	1000cy	0/77			
		AEC-Q101	DPA after TC	2	-	0/2			
H3TRB	N	JESD22-A101	Humidity (HR)=85% Temperature=85°C Voltage=100V	154	1000h		0/77		0/77
	Y			77	1000h	0/77			
		AEC-Q101	DPA after H3TRB	2	-	0/2			
uHAST	Y	JESD22 A-118	Humidity (HR)=85% Pressure=2.3bar Temperature=130°C	77	96h	0/77			
	N			154	96h		0/77		0/77
IOLT	Y	MIL-STD 750 Method 1037	Delta T _j =125°C Intensity (If)=2.1A Time (on/off)=120s/120s	77	500h	0/77			
	N		Delta T _j =100°C Intensity (If)=2A Time (on/off)=120s/120s	77	1000h		0/77		
	N		Delta T _j =125°C Intensity (If)= 2.1A Time (on/off)=210s/210s	77	500h			0/77	
	N		Delta T _j =125°C Intensity (If)=3.5A Time (on/off)=300s/300s	77	500h				0/77
Wire Bond Strength		MIL-STD-750 Method 2037	Pre and Post change 10 bonds from minimum 5parts	58	-	0/10	0/8	0/10	0/30
Bond Shear		AEC-Q101-003	10 bonds from minimum 5parts	58	-	0/10	0/8	0/10	0/30
Die Shear		MIL-STD-750 Method 2037	Pre and Post change	10	-	0/10			

6 ANNEXES

6.1 Parametric Verifications and ESD

- Results on STPSC20H065CWLY product:

TEST	VR	VR	VR	IR	IR	IR
EQUIPMENT	TESEC_881TT_TEST292					
UNIT	-40°C	25°C	150°C	-40°C	25°C	150°C
Condition 1				VR=650V	VR=650V	VR=650V
Condition 2						
Condition 3						
Min. Datasheet	650V	650V	650V			
Typ. Datasheet					9uA	85uA
Max. Datasheet					100uA	425uA
UNIT	V	V	V	nA	nA	uA
N	60	60	60	60	60	60
Min	900.900	910.400	932.000		19.950	0.877
Max	943.900	953.900	976.400		3973.000	11.090
Avg	929.387	939.210	961.568	No value due to frost issue	160.286	1.658

TEST	VF	VF	VF	RTH(J-C)	ESD_CDM	ESD_HBM
EQUIPMENT	TESEC_881TT_TEST292					
UNIT	-40°C	25°C	150°C	RTH(PHASE11) _MESU1150	ESD-CDM TEST SYSTEM	ESS6008
Condition 1	IF=10A	IF=10A	IF=10A		25°C	25°C
Condition 2						
Min. Datasheet						
Typ. Datasheet		1.45V	1.7V	1.25°C/W		
Max. Datasheet		1.65V	2.05V	1.50°C/W		
UNIT	V	V	V	°C/W	KV	KV
N	60	60	60	20	60	60
Min	1.497	1.456	1.650	0.988	>1.0	>8.0
Max	1.544	1.517	1.786	1.078	>1.0	>8.0
Avg	1.526	1.498	1.748	1.026		

- Results on STPSC10H065BY product:

TEST	VR	VR	VR	IR	IR	IR
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	-40°C	24°C	150°C	-40°C	24°C	150°C
Condition 2				VR=650V	VR=650V	VR=650V
Min. Datasheet	650V	650V	650V			
Typ. Datasheet					9uA	85uA
Max. Datasheet					100uA	425uA
UNIT	V	V	V	nA	nA	uA
N	30	30	30	30	30	30
Min	907.200	915.700	934.900		18.550	0.456
Max	937.200	946.200	969.500		625.600	2.690
Avg	920.390	929.123	951.547	No value due to frost issue	106.576	1.002

TEST	VF	VF	VF	RTH(J-C)	ESD_CDM	ESD_HBM
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	-40°C	24°C	150°C	RTH(PHASE11) _MESU1150	ESD-CDM TEST SYSTEM	ESS6008
Condition 2	IF=10A	IF=10A	IF=10A		25°C	23°C
Min. Datasheet						
Typ. Datasheet		1.45V	1.70V	1.25°C/W		
Max. Datasheet		1.65V	2.05V	1.50°C/W		
UNIT	V	V	V	°C/W	KV	KV
N	30	30	30	10	30	30
Min	1.453	1.425	1.579	0.883	>1.0	>8.0
Max	1.493	1.467	1.724	0.992	>1.0	>8.0
Avg	1.472	1.447	1.671	0.946		

- Results on STPSC20065DY product:

TEST	VR	VR	VR	IR	IR	IR
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	-40°C	23°C	150°C	-40°C	23°C	150°C
Condition 2				VR=650V	VR=650V	VR=650V
Min. Datasheet	650V	650V	650V			
Typ. Datasheet					30uA	280uA
Max. Datasheet					300uA	2000uA
UNIT	V	V	V	nA	uA	uA
N	30	30	30	30	30	30
Min	862.000	867.300	884.600	No value due to frost issue	0.336	3.347
Max	898.300	904.800	926.200		6.682	20.000
Avg	885.087	891.440	913.540		1.196	6.865

TEST	VF	VF	VF	RTH(J-C)	ESD_CDM	ESD_HBM
EQUIPMENT	TESEC_881TT_TEST292					RTH(PHASE11) _MESU1150
Condition 1	-40°C	23°C	150°C		23°C	23°C
Condition 2	IF=10A	IF=20A	IF=20A			
Min. Datasheet		1.30V	1.45V	0.60°C/W		
Typ. Datasheet		1.45V	1.65V	0.90°C/W		
Max. Datasheet						
UNIT	V	V	V	°C/W	KV	KV
N	30	30	30	10	30	30
Min	1.189	1.299	1.390	0.514	>1.0	>8.0
Max	1.200	1.326	1.474	0.565	>1.0	>8.0
Avg	1.193	1.310	1.440	0.535		

6.2 Tests description

Test name	Description	Purpose
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
HTRB High Temperature Reverse	The diode is biased in static reverse mode at targeted junction temperature.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature.	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
DPA Destructive Physical Analysis	Specific construction analysis on random parts that have successfully completed H3TRB or TC.	To investigate on reliability stresses impact on delamination, corrosion and product construction integrity.
WBS Wire Bond Strength	To apply the specified stress to the bond, lead wire, or terminal.	To measure bond strength, evaluate bond strength distributions, or to determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermo-compression, ultrasonic, or related techniques
BS Bond Shear	This test establishes a procedure for determining the strength of the interface between a gold ball bond and a die bonding surface, or an aluminum wedge/stitch bond and a die or package bonding surface, on either pre-encapsulation or post-encapsulation components. This strength measurement is extremely important in determining two features: 1) the integrity of the metallurgical bond which has been formed. 2) the reliability of gold and aluminum wire bonds to die or package bonding surfaces. This test method can be used only when the ball height and diameter for ball bonds, or the wire height (1.25 mil and larger at the compressed bond area) for wedge/stitch bonds, are large enough and adjacent interfering structures are far enough away to allow suitable placement and clearance (e.g., above the bonding	To check the integrity of the metallurgical bond.
DS Die Shear	A sufficient force to shear the die from its mounting shall be applied to the die.	To establish the integrity of the semiconductor die attachment to the package header or other substrate.

Qualification Report

*Top & Back side metallization rationalization for
Automotive SiC diodes 650V in ST Catania*

General Information		Locations	
Product Line	Rectifiers	Wafer fab	ST Catania - ITALY
Product Description	Silicon Carbide Power Schottky	Assembly plant	ST Shenzhen - CHINA Subcontractor 994X - CHINA Subcontractor 998G - CHINA
Product perimeter	Refer to list page 4	Reliability Lab	ST TOURS - FRANCE
Product Group	ADG	Reliability assessment	PASS
Product division	Discrete & Filter		
Package	DPAK, D ² PAK, TO-220AB, TO-220AC, I ² PAK, DO247, TO247, TO247LL		
Maturity level step	QUALIFIED		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	30-Sept-2021	17	Christophe GOIN	Julien MICHELON	Initial release. Linked to PCN 13047.

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1	APPLICABLE AND REFERENCE DOCUMENTS	3
2	GLOSSARY	3
3	RELIABILITY EVALUATION OVERVIEW.....	4
3.1	OBJECTIVES.....	4
3.2	CONCLUSION.....	4
4	DEVICE CHARACTERISTICS	5
4.1	DEVICE DESCRIPTION.....	5
4.2	CONSTRUCTION NOTE.....	8
5	TESTS RESULTS SUMMARY	11
5.1	TEST VEHICLES	11
5.2	TEST PLAN	12
5.3	RESULTS SUMMARY	14
6	ANNEXES	15
6.1	PARAMETRIC VERIFICATIONS	15
6.2	TESTS DESCRIPTION	17

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101 Rev.D1	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices
AEC-Q005	Pb-Free Test Requirements

2 GLOSSARY

SS	Sample Size
PC	Pre-Conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
H3TRB	High Humidity High Temperature Reverse Bias
IOLT	Intermittent Operating Life Test
UHAST	Unbiased Highly Accelerated Stress Test
GD	Generic Data
MSL	Moisture Sensitivity Level
T_j	Junction Temperature
BS	Bond Shear
DS	Die Shear
WBS	Wire Bond Strength
DPA	Destructive Physical Analysis (after TC and H3TRB)

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify Top & Back side metallization rationalization for 650V Silicon Carbide Power Schottky Rectifier products in ST Catania.

The involved products are listed in the table here below:

Product	Description	Package	Assembly Location	
STPSC6H065BY-TR	6 A, 650 V	DPAK	ST Shenzhen - China	
STPSC8H065BY-TR	8 A, 650 V			
STPSC10H065BY-TR	10 A, 650 V			
STPSC10H065GY-TR	10 A, 650 V			
STPSC20065GY-TR	20 A, 650 V	D ² PAK	ST Shenzhen - China	
STPSC8H065G2Y-TR	8 A, 650 V			
STPSC20065WY	20 A, 650 V	DO-247	Subcontractor – China (998G)	
STPSC20H065CWY	2x10 A, 650 V	TO-247		
STPSC40065CWY	2x20 A, 650 V			
STPSC20H065CTY	2x10 A, 650 V	TO-220AB		
STPSC10H065DY	10 A, 650 V	TO-220AC	Subcontractor – China (998G)	
STPSC6C065DY	6 A, 650 V			
STPSC20065DY	20 A, 650 V			
STPSC10C065RY	10 A, 650 V	I ² PAK	Subcontractor – China (998G)	
STPSC20H065CWLY	20 A, 650 V	TO247LL		

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology » and AECQ-101 RevD1 guidelines.

The following reliability tests ensuing are:

- TC and IOLT to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

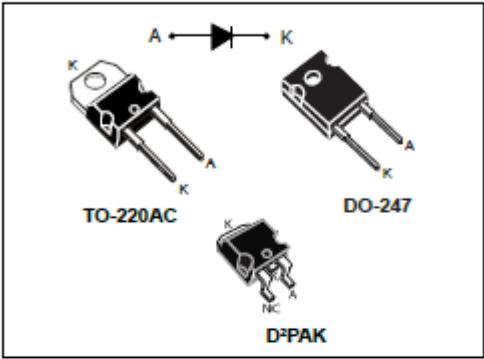
4.1 Device description

Refer to ST specification (examples below for STPSC20065-Y, STPSC10H065BY and STPSC20H065CWLY):

STPSC20065-Y

Automotive 650 V power Schottky silicon carbide diode

Datasheet - production data



Description

The SiC diode is an ultra high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Especially suited for use in PFC applications, this ST SiC diode will boost performance in hard switching conditions. Its high forward surge capability ensures good robustness during transient phases.

Features

- AEC-Q101 qualified
- No reverse recovery charge in application current range
- Switching behavior independent of temperature
- Dedicated to PFC applications
- High forward surge capability
- ECOPACK®2 compliant component
- PPAP capable
- Operating T_j from -40 °C to 175 °C

Table 1: Device summary

Symbol	Value
$I_{F(AV)}$	20 A
V_{RRM}	650 V
T_j (max.)	175 °C
V_F (typ.)	1.30 V

Automotive 650 V power Schottky silicon carbide diode

**Features**

- AEC-Q101 qualified
- No reverse recovery charge in application current range
- Switching behavior independent of temperature
- Recommended to PFC applications
- PPAP capable
- ECOPACK®2 compliant component

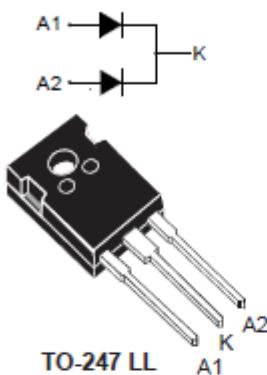
Description

The SiC diode is an ultra-high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Especially suited for use in PFC applications, this ST SiC diode will boost performance in hard switching conditions.

Product status	
STPSC10H065BY-TR	
Product summary	
Symbol	Value
$I_{F(AV)}$	10 A
V_{RRM}	650 V
$T_{J(max.)}$	175 °C

Automotive 20 A 650 V power Schottky silicon carbide diode



Features



- AEC-Q101 qualified
- PPAP capable
- No or negligible reverse recovery
- Switching behavior independent of temperature
- Dedicated to PFC applications
- High forward surge capability
- ECOPACK² compliant component

Applications

- On board charger (OBC)
- Charging stations
- PFC applications
- UPS
- Inverters
- Telecom power supplies

Description

The STPSC20H065CWLY is an ultra-high-performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature and are ideal for automotive applications.

Especially suited for use in PFC applications, UPS, inverters, telecom power supplies and battery chargers (either integrated in the vehicle or in a charging station), this diode will enhance the performance of the targeted application. Its high forward surge capability ensures a good robustness during transient phases.

Product status link	
STPSC20H065CWLY	
Product summary	
$I_{F(AV)}$	2 x 10 A
V_{RRM}	650 V
T_J (max.)	175 °C
V_F (typ.)	1.45 V
Product label	
	

4.2 Construction Note

STPSCxxH065BY-TR	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	DPAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSCxxH065GY-TR	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	D ² PAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20065WY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	DO-247
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CWY - STPSC40065CWY

Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-247
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CTY

Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-220AB
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSCxxH065DY - STPSCxx065DY

Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-220AC
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CWLY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST subcontractor – China (998G)
Package description	TO-247LL
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST subcontractor – China (998G)

STPSC10C065RY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	I ² PAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	STPSC10H065BY	DPAK	Qualification lot 1 – back side metallization
L2	STPSC20H12CWY	TO247	Qualification lot 2 – back side metallization
L3	STPSC40H12CWL	TO247LL	Qualification lot 3 – back side metallization
L4	STPSC10H12B	DPAK	Qualification lot 4 – back side metallization
L5	STPSC20065G	D2PAK	Qualification lot 5 – front side metallization
L6	STPSC10H065B	DPAK	Qualification lot 6 – front side metallization
L7	STPSC15H12DY	TO-220	Qualification lot 7 – front side metallization
L8	STPS20H065CWLY	TO247LL	Qualification lot 8 – front & back side metallization

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard specification	All qualification parts tested per the requirements of the appropriate device specification			X
Pre-conditioning	PC	JESD22A-113	All qualification parts tested per the requirements of the appropriate device specification		As per targeted MSL	X
MSL research	MSL	J-STD-020	L1, L4	60		X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	All qualification parts tested per the requirements of the appropriate device specification			X
High Temperature Storage Life	HTSL	JESD22B-101			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
High Temperature Gate Bias	HTGB	JESD22A-108			Required for PowerMOSFET – IGBT only.	
High Temperature Reverse Bias	HTRB	JESD22A-108			Not applicable for metallization change	
High Temperature Forward Bias	HTFB	JESD22A-108			Not required, applicable only to LEDs	
High Temperature Operating Life Test	HTOL	JESD22A-108			Covered by HTRB.	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test B			Required for Voltage Regulator (Zener) only.	
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test A			Required for Thyristor only.	
Temperature Cycling	TC	JESD22A-104	L1, L2, L4, L5, L6, L7, L8	539		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET – IGBT only.	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118			Covered by H3TRB	
Autoclave	AC	JESD22A-102			Not recommended	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1, L2, L3, L8	308		X
High Temperature High Humidity Bias	HTHBB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	L1, L3, L8	231	For power devices.	X
Power and Temperature Cycle	PTC	JED22A-105			Covered by IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005			Not required for metallization change	
ESD Characterization	ESD CDM	AEC Q101-001 and 005			Not required for metallization change	

Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	L1	4	After H3TRB and TC. For automotive products only	X
Physical Dimension	PD	JESD22B-100			Not relevant for wafer production and test qualification	
Terminal Strength	TS	MIL-STD-750 Method 2036			Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	L1, L4	60	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	X
Solderability	SD	J-STD-002 JESD22B102			Not relevant for wafer production and test qualification	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate			Required in case of process change.	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	L5, L6, L7, L8	60	Covered during workability trials	X
Bond Shear	BS	AEC-Q101-003	L5, L6, L7, L8	60	Covered during workability trials	X
Die Shear	DS	MIL-STD-750 Method 2017	L1, L2, L3, L4	60	Not Applicable to parts with solder paste die attach	X
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET – IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201			Not relevant for wafer production and test qualification	
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Low Temperature Storage	LTS	JESD-22 A119: 209			AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104			AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037			AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037			AQG324 test for Modules	
Mechanical shock	MS	IEC 60068-2-27			AQG324 test for Modules	
Vibration	V	IEC60068-2-6			AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.							
						Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	Lot 8
Parametric Verifications		ST datasheet	Over part temperature range	120	-	Refer to paragraph 6.1 in Annexes							
External Visual Inspection		JESD22 B-101	-	830	-	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process							
Pre and Post Electrical Test		ST datasheet	I_R , V_F parameters following product datasheet	1138	-	0/1061							
PC		JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	462	-	0/462							
MSL1 research	N	JESD22 A-113	MSL=1 Reflow=3 Temperature=85°C Humidity (HR)=85%	60	-	0/30			0/30				
TC	Y	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	308	1000c	0/77			0/77	0/77	0/77		
	N		Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	231	1000c		0/77					0/77	0/77
DPA after TC	Y	AEC-Q101	DPA after 1000c of TC	2	-	0/2							
H3TRB	Y	JESD22-A101	Humidity (HR)=85% Temperature=85°C Voltage=100V	77	1000h	0/77							
	N			231	1000h		0/77	0/77					0/77
DPA after H3TRB	Y	AEC-Q101	DPA after 1000h of H3TRB	2	-	0/2							
IOLT	Y	MIL-STD 750 Method 1037	Delta T_j =100°C Intensity (If)=2.1A Time (off)=120s Time (on)=120s	77	1000h	0/77							
	N		Delta T_j =100°C Intensity (If)=2A Time (off)=120s Time (on)=120s	154	1000h			0/77					0/77
RSH	N	JESD22A-111 (SMD) / JESD22B-106 (PTH)	Temperature=260°C Time (on)=10s	60	-	0/30			0/30				
Die Shear		MIL-STD-750 Method 2017	Pre and Post change	60	-	0/15	0/15	0/15	0/15				
Wire Bond Strength		MIL-STD-750 Method 2037	10 bonds from minimum 5 parts	60	-					0/10	0/10	0/10	0/30
Bond Shear		AEC-Q101-003	10 bonds from minimum 5 parts	60	-					0/10	0/10	0/10	0/30

6 ANNEXES

6.1 Parametric Verifications

- Results on STPSC10H065BY product (Back side metallization rationalization):

TEST	VBR	IR	VF	RTH(J-C)
EQUIPMENT	TESEC_881TT_TEST292			MESU1150
Condition 1	24°C	24°C	24°C	
Condition 2		VR=650V	IF=10A	
Min. Datasheet	650V			
Typ. Datasheet		9uA	1.45V	1.25°C/W
Max. Datasheet		100uA	1.65V	1.50°C/W
UNIT	V	uA	V	°C/W
N	30	30	30	10
Min	914.300	0.045	1.393	0.972
Max	934.200	15.400	1.526	1.117
Moy.	927.883	4.051	1.428	1.060

- Results on STPSC20065D product (Back side metallization rationalization):

TEST	VBR	IR	IR	VF	RTH(J-C)
EQUIPMENT	TESEC_881TT_TEST292			MESU1150	
Condition 1	25°C	25°C	25°C	25°C	
Condition 2		VR=600V	VR=650V	IF=20A	
Min. Datasheet	650V				
Typ. Datasheet		15uA	30uA	1.30V	0.60°C/W
Max. Datasheet		150uA	300uA	1.45V	0.90°C/W
UNIT	V	nA	nA	V	°C/W
N	30	30	30	30	10
Min	874.400	126.500	329.100	1.320	0.528
Max	920.200	1743.000	3806.000	1.344	0.596
Moy.	883.327	336.570	838.530	1.326	0.558

- Results on STPSC10H065B product (Front side metallization rationalization):

TEST	VBR	IR	IR	VF	VF
EQUIPMENT	TESEC_881TT_TEST292				
Condition 1	25°C	25°C	150°C	25°C	150°C
Condition 2		VR=650V	VR=650V	IF=10A	IF=10A
Min. Datasheet	650V				
Typ. Datasheet		9uA	85uA	1.56V	1.98V
Max. Datasheet		100uA	425uA	1.75V	2.5V
UNIT	V	nA	uA	V	V
N	30	30	15	30	15
Min	932.200	22.350	0.588	1.450	1.650
Max	958.500	3456.000	2.986	1.682	1.855
Avg	943.603	262.980	1.033	1.518	1.736

- Results on STPSC20065GY product (Front side metallization rationalization):

TEST	VBR	IR	IR	IR	VF	VF
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	25°C	25°C	25°C	150°C	25°C	150°C
Condition 2		VR=600V	VR=650V	VR=650V	IF=20A	IF=20A
Min. Datasheet	650V					
Typ. Datasheet		15uA	30uA	280uA	1.30V	1.45V
Max. Datasheet		150uA	300uA	2000uA	1.45V	1.65V
UNIT	V	uA	uA	uA	V	V
N	30	30	30	15	30	15
Min	857.700	0.102	0.268	2.849	1.311	1.447
Max	921.000	9.135	16.340	131.600	1.340	1.486
Avg	898.960	1.162	2.336	28.572	1.319	1.467

- Results on STPSC20065D product (Front & Back side metallization rationalization):

TEST	VRRM	VRRM	VRRM	VF	VF	VF
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	-40°C	25°C	150°C	-40°C	25°C	150°C
Condition 2				IF=20A	IF=20A	IF=20A
Min. Datasheet	650V	650V	650V			
Typ. Datasheet					1.30V	1.45V
Max. Datasheet					1.45V	1.65V
UNIT	V	V	V	V	V	V
N	30	30	30	30	30	30
Min	829.300	827.300	852.000	1.336	1.308	1.412
Max	904.400	913.500	931.400	1.370	1.345	1.499
Avg	886.050	891.350	910.390	1.349	1.325	1.469

TEST	IR	IR	IR	IR
EQUIPMENT	TESEC_881TT_TEST292			
Condition 1	-40°C	25°C	25°C	150°C
Condition 2	VR=650V	VR=600V	VR=650V	VR=650V
Min. Datasheet				
Typ. Datasheet		15uA	30uA	280uA
Max. Datasheet		150uA	300uA	2000uA
UNIT	nA	nA	nA	uA
N	30	30	30	30
Min	No value due to frost issue	98.200	282.100	2.480
Max		2049.000	3847.000	20.230
Avg		305.614	707.173	4.689

6.2 Tests description

Test name	Description	Purpose
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
HTRB High Temperature Reverse	The diode is biased in static reverse mode at targeted junction temperature.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature.	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
DPA Destructive Physical Analysis	Specific construction analysis on random parts that have successfully completed H3TRB or TC.	To investigate on reliability stresses impact on delamination, corrosion and product construction integrity.
WBS Wire Bond Strength	To apply the specified stress to the bond, lead wire, or terminal.	To measure bond strength, evaluate bond strength distributions, or to determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermo-compression, ultrasonic, or related techniques
BS Bond Shear	This test establishes a procedure for determining the strength of the interface between a gold ball bond and a die bonding surface, or an aluminum wedge/stitch bond and a die or package bonding surface, on either pre-encapsulation or post-encapsulation components. This strength measurement is extremely important in determining two features: 1) the integrity of the metallurgical bond which has been formed. 2) the reliability of gold and aluminum wire bonds to die or package bonding surfaces. This test method can be used only when the ball height and diameter for ball bonds, or the wire height (1.25 mil and larger at the compressed bond area) for wedge/stitch bonds, are large enough and adjacent interfering structures are far enough away to allow suitable placement and clearance (e.g., above the bonding)	To check the integrity of the metallurgical bond.
DS Die Shear	A sufficient force to shear the die from its mounting shall be applied to the die.	To establish the integrity of the semiconductor die attachment to the package header or other substrate.

(1) ADG: Automotive and Discrete Group

PCN

Product/Process Change Notification

Wafer Manufacturing & EWS capacity extension in ST Singapore

for Automotive SiC 650V products

Notification number:	ADG/21/13047	Issue Date	08-Oct-2021		
Issued by	Isabelle BALLON				
Product series affected by the change	STPSCxxx065xY STPSCxxx065xY-TR Refer to attached table for involved Commercial Products Specific devices not expressly listed in table are included in this change.				
Type of change	Front-End realization & EWS				

Description of the change

STMicroelectronics is qualifying an additional Front-End line (Wafer manufacturing) & EWS (Electrical Wafer Sorting) for Automotive SiC 650V products.

This capacity extension will be enhanced by wafer manufacturing process rationalization on both locations.

Reason for change

In line with the commitment of ST Company to reinforce its leading position in the SiC Power Rectifiers market and to support strong SiC business increase, STMicroelectronics has decided to expand the manufacturing & EWS capacity of SiC 650V diodes.

This additional wafer fab & EWS capacity will be done through production line located in the Singapore existing plant.

With this additional SiC wafer & EWS line investment, STMicroelectronics will increase its production capacity to better serve its customers through service improvement and lead time reduction, especially as demand grows.

650V SiC Power Schottky Rectifiers wafer manufacturing & EWS sites qualification overview:

	Before PCN	After PCN
SiC 650V Wafer manufacturing & EWS locations	ST plant Catania – Italy	ST plant Catania – Italy ST plant Singapore

Former versus changed product:	The changed products do not present modified electrical, dimensional, or thermal parameters, leaving unchanged the
---------------------------------------	--

(1) ADG: Automotive and Discrete Group

	<p>current information published in the products datasheet.</p> <p>ST decides to rationalize Top & Back side metallization on all SiC technologies lines.</p> <p>This rationalization is part of Sustainability and ST Eco-design approach (engagement in Responsible Mineral Initiative).</p> <p>ST Sustainable Technology Brochure</p> <p>EWS flow remains the same.</p> <p>The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged.</p> <p>There is no change in the packing modes and the standard delivery quantities either.</p>					
Disposition of former products						
As the purpose is a manufacturing capacity extension, shipments will be supported using the two production lines with rationalized process.						
Marking and traceability						
Traceability will be ensured by Finished Good/Type and Plant code in Trace code print on carton labels.						
Commercial part number (Order code) Example	ST Catania - Italy Current Finished Good (Type) Example	ST Catania - Italy New Finished Good (Type) Example	ST Singapore New Finished Good (Type) Example			
STPSC10H065DY	YPSC10H065DF6 ⁷	YPSC10H065DG ⁷	YPSC10H065D% ⁷			
Qualification complete date	08-Oct-2021					

(1) ADG: Automotive and Discrete Group

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date ST Catania - Italy	Availability date ST Singapore
Rectifiers	SiC	STPSC20065DY	Week 11-2022	Week 40-2021
Rectifiers	SiC	STPSC20H065CWY	Week 05-2022	Week 40-2021
Rectifiers	SiC	STPSC10C065RTKY	Week 05-2022	Week 48-2021
Rectifiers	SiC	STPSC20H065CWLY	Week 05-2022	Week 40-2021
Rectifiers	SiC	STPSC6H065BY-TR	Week 05-2022	Week 48-2021
Rectifiers	SiC	STPSC8H065BY-TR	Week 05-2022	Week 48-2021
Rectifiers	SiC	STPSC10H065GY-TR	Week 05-2022	Week 40-2021

Other samples are available on demand.

Change implementation schedule

Sales-types	Estimated production start	Estimated first shipments
All	Week 21-2021 (ST Singapore)	Week 14-2022 (ST Singapore)
Comments:		For proper traceability robustness, process rationalization in Catania will be effective from w42-2021.

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.

Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change.

Absence of additional response within 180 days of receipt of this PCN will constitute acceptance of the change.

Qualification program and results	21072QRP Attached (ST Singapore) 21074QRP Attached (for ST Catania process rationalization)
--	--

(1) ADG: Automotive and Discrete Group

Involved Commercial part numbers
STPSC10065DY
STPSC10065GY-TR
STPSC10C065RY
STPSC10H065BY-TR
STPSC10H065DY
STPSC10H065GY-TR
STPSC12065DY
STPSC12065G2Y-TR
STPSC12065GY-TR
STPSC12C065DY
STPSC12H065DY
STPSC20065DY
STPSC20065GY-TR
STPSC20065WY
STPSC20H065CTY
STPSC20H065CWY
STPSC2H065BY-TR
STPSC40065CWY
STPSC6C065DY
STPSC6H065BY-TR
STPSC8065DY
STPSC8H065BY-TR
STPSC8H065G2Y-TR
STPSC20H065CWLY

Specific devices not expressly listed above are included in this change.

Qualification Report

Wafer Manufacturing & EWS capacity extension in ST Singapore for Automotive 650V SiC diodes

General Information		Locations	
Product Line	Rectifiers	Wafer fab	ST SINGAPORE
Product Description	Silicon Carbide Power Schottky	Assembly plant	ST Shenzhen – CHINA Subcontractor 998G - CHINA
Product perimeter	Refer to list page 4	Reliability Lab	ST TOURS - FRANCE
Product Group	ADG	Reliability assessment	PASS
Product division	Discrete & Filter		
Package	DPAK, D ² PAK, TO-220AB, TO-220AC, I ² PAK, DO247, TO247, TO247LL		
Maturity level step	QUALIFIED		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	30-Sept-2021	16	Christophe GOIN	Julien MICHELON	Initial release. Linked to PCN 13047.

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1	APPLICABLE AND REFERENCE DOCUMENTS	3
2	GLOSSARY	3
3	RELIABILITY EVALUATION OVERVIEW.....	4
3.1	OBJECTIVES.....	4
3.2	CONCLUSION.....	4
4	DEVICE CHARACTERISTICS	5
4.1	DEVICE DESCRIPTION.....	5
4.2	CONSTRUCTION NOTE.....	8
5	TESTS RESULTS SUMMARY	10
5.1	TEST VEHICLES	10
5.2	TEST PLAN	11
5.3	RESULTS SUMMARY	13
6	ANNEXES	14
6.1	PARAMETRIC VERIFICATIONS	14
6.2	TESTS DESCRIPTION	16

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101 Rev.D1	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices
AEC-Q005	Pb-Free Test Requirements

2 GLOSSARY

SS	Sample Size
PC	Pre-Conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
H3TRB	High Humidity High Temperature Reverse Bias
IOLT	Intermittent Operating Life Test
UHAST	Unbiased Highly Accelerated Stress Test
GD	Generic Data
MSL	Moisture Sensitivity Level
T_j	Junction Temperature
BS	Bond Shear
DS	Die Shear
WBS	Wire Bond Strength
DPA	Destructive Physical Analysis (after TC and H3TRB)

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify wafer production & test for 650V Silicon Carbide Power Schottky Rectifier products in ST Singapore.

The involved products are listed in the table here below:

Product	Description	Package	Assembly Location	
STPSC6H065BY-TR	6 A, 650 V	DPAK	ST Shenzhen - China	
STPSC8H065BY-TR	8 A, 650 V			
STPSC10H065BY-TR	10 A, 650 V			
STPSC10H065GY-TR	10 A, 650 V			
STPSC20065GY-TR	20 A, 650 V	D ² PAK	ST Shenzhen - China	
STPSC8H065G2Y-TR	8 A, 650 V			
STPSC20065WY	20 A, 650 V	DO-247	Subcontractor – China (998G)	
STPSC20H065CWY	2x10 A, 650 V	TO-247		
STPSC40065CWY	2x20 A, 650 V			
STPSC20H065CTY	2x10 A, 650 V	TO-220AB		
STPSC10H065DY	10 A, 650 V	TO-220AC	Subcontractor – China (998G)	
STPSC6C065DY	6 A, 650 V			
STPSC20065DY	20 A, 650 V			
STPSC10C065RY	10 A, 650 V	I ² PAK	Subcontractor – China (998G)	
STPSC20H065CWLY	20 A, 650 V	TO247LL		

The reliability test methodology used follows the JESD47: « Stress Test riven Qualification Methodology » and AECQ-101 RevD1 guidelines.

The following reliability tests ensuing are:

- TC and IOLT to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

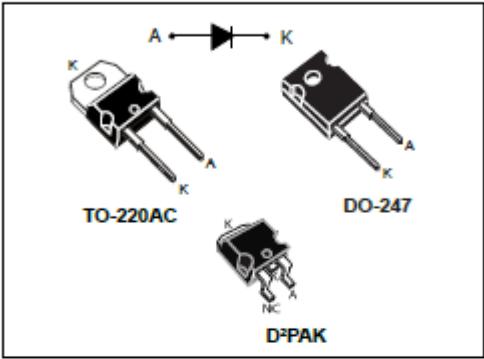
4.1 Device description

Refer to ST specification (examples below for STPSC20065-Y, STPSC10H065BY and STPSC20H065CWLY):

STPSC20065-Y

Automotive 650 V power Schottky silicon carbide diode

Datasheet - production data



Description

The SiC diode is an ultra high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Especially suited for use in PFC applications, this ST SiC diode will boost performance in hard switching conditions. Its high forward surge capability ensures good robustness during transient phases.

Features

- AEC-Q101 qualified
- No reverse recovery charge in application current range
- Switching behavior independent of temperature
- Dedicated to PFC applications
- High forward surge capability
- ECOPACK®2 compliant component
- PPAP capable
- Operating T_j from -40 °C to 175 °C

Table 1: Device summary

Symbol	Value
$I_{F(AV)}$	20 A
V_{RRM}	650 V
T_j (max.)	175 °C
V_F (typ.)	1.30 V

Automotive 650 V power Schottky silicon carbide diode

**Features**

- AEC-Q101 qualified
- No reverse recovery charge in application current range
- Switching behavior independent of temperature
- Recommended to PFC applications
- PPAP capable
- ECOPACK®2 compliant component

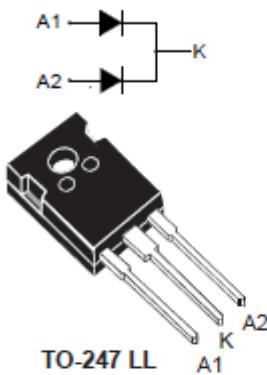
Description

The SiC diode is an ultra-high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Especially suited for use in PFC applications, this ST SiC diode will boost performance in hard switching conditions.

Product status	
STPSC10H065BY-TR	
Product summary	
Symbol	Value
$I_{F(AV)}$	10 A
V_{RRM}	650 V
$T_{J(max.)}$	175 °C

Automotive 20 A 650 V power Schottky silicon carbide diode



Features



- AEC-Q101 qualified
- PPAP capable
- No or negligible reverse recovery
- Switching behavior independent of temperature
- Dedicated to PFC applications
- High forward surge capability
- ECOPACK² compliant component

Applications

- On board charger (OBC)
- Charging stations
- PFC applications
- UPS
- Inverters
- Telecom power supplies

Description

The STPSC20H065CWLY is an ultra-high-performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature and are ideal for automotive applications.

Especially suited for use in PFC applications, UPS, inverters, telecom power supplies and battery chargers (either integrated in the vehicle or in a charging station), this diode will enhance the performance of the targeted application. Its high forward surge capability ensures a good robustness during transient phases.

Product status link	
STPSC20H065CWLY	
Product summary	
$I_{F(AV)}$	2 x 10 A
V_{RRM}	650 V
T_J (max.)	175 °C
V_F (typ.)	1.45 V
Product label	
	

4.2 Construction Note

STPSCxxH065BY-TR	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	DPAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSCxxH065GY-TR	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	D ² PAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20065WY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	DO-247
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CWY - STPSC40065CWY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-247
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CTY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-220AB
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSCxxH065DY - STPSCxx065DY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-220AC
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CWLY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST subcontractor – China (998G)
Package description	TO-247LL
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST subcontractor – China (998G)

STPSC10C065RY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Singapore
Assembly information	
Assembly site	ST Shenzhen – China
Package description	I ² PAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	STPSC10H065BY	DPAK	Qualification lot 1
L2	STPSC20065DY	TO220AC	Qualification lot 2
L3	STPSC10H065DY	TO220AC	Qualification lot 3
L4	STPSC20H065CWLY	TO247LL	Qualification lot 4

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard specification	All qualification parts tested per the requirements of the appropriate device specification			X
Pre-conditioning	PC	JESD22A-113	All qualification parts tested per the requirements of the appropriate device specification		As per targeted MSL	X
MSL research	MSL	J-STD-020	L1	30		X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	All qualification parts tested per the requirements of the appropriate device specification			X
High Temperature Storage Life	HTSL	JESD22B-101			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
High Temperature Gate Bias	HTGB	JESD22A-108			Required for PowerMOSFET – IGBT only.	
High Temperature Reverse Bias	HTRB	JESD22A-108	L1, L2, L4	231		X
High Temperature Forward Bias	HTFB	JESD22A-108			Not required, applicable only to LEDs	
High Temperature Operating Life Test	HTOL	JESD22A-108			Covered by HTRB.	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test B			Required for Voltage Regulator (Zener) only.	
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test A			Required for Thyristor only.	
Temperature Cycling	TC	JESD22A-104	L1, L2, L3, L4	308		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET – IGBT only.	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118	L1, L2, L4	231		X
Autoclave	AC	JESD22A-102			Not recommended	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1, L2, L4	231		X
High Temperature High Humidity Bias	HTHBB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	L1, L2, L3, L4	308	For power devices.	X
Power and Temperature Cycle	PTC	JED22A-105			Covered by IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005		120	For automotive products only	X
ESD Characterization	ESD CDM	AEC Q101-001 and 005		120	For automotive products only	X

Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	L1	4	After H3TRB and TC. For automotive products only	X
Physical Dimension	PD	JESD22B-100			Not relevant for wafer production and test qualification	
Terminal Strength	TS	MIL-STD-750 Method 2036			Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)			Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102			Not relevant for wafer production and test qualification	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate			Required in case of process change.	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	L1, L2, L3, L4	58	Covered during workability trials	X
Bond Shear	BS	AEC-Q101-003	L1, L2, L3, L4	58	Covered during workability trials	X
Die Shear	DS	MIL-STD-750 Method 2017	L1	10	Not Applicable to parts with solder paste die attach	X
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET – IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201			Not relevant for wafer production and test qualification	
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Low Temperature Storage	LTS	JESD-22 A119: 209			AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104			AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037			AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037			AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27			AQG324 test for Modules	
Vibration	V	IEC60068-2-6			AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.			
						Lot 1	Lot 2	Lot 3	Lot 4
Parametric Verifications		ST datasheet	Over part temperature range	120	-	Refer to paragraph 6.1 in Annexes			
External Visual Inspection		JESD22 B-101	-	1309	-	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process			
Pre and Post Electrical Test		ST datasheet	I _R , V _F parameters following product datasheet	1309	-	0/1309			
PC		JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	385	-	0/385			
MSL1 research	N	JESD22 A-113	MSL=1, Reflow=3 Temperature=85°C Humidity (HR)=85%	30	-	0/30			
HTRB	N	JESD22-A108/MIL-STD-750-1 M1038 Method A	Junction Temperature=175°C Voltage=650V	231	1000h	0/77	0/77		0/77
TC	N	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-55°C	231	1000cy		0/77	0/77	0/77
	Y			77	1000cy	0/77			
		AEC-Q101	DPA after TC	2	-	0/2			
H3TRB	N	JESD22-A101	Humidity (HR)=85% Temperature=85°C Voltage=100V	154	1000h		0/77		0/77
	Y			77	1000h	0/77			
		AEC-Q101	DPA after H3TRB	2	-	0/2			
uHAST	Y	JESD22 A-118	Humidity (HR)=85% Pressure=2.3bar Temperature=130°C	77	96h	0/77			
	N			154	96h		0/77		0/77
IOLT	Y	MIL-STD 750 Method 1037	Delta T _j =125°C Intensity (If)=2.1A Time (on/off)=120s/120s	77	500h	0/77			
	N		Delta T _j =100°C Intensity (If)=2A Time (on/off)=120s/120s	77	1000h		0/77		
	N		Delta T _j =125°C Intensity (If)= 2.1A Time (on/off)=210s/210s	77	500h			0/77	
	N		Delta T _j =125°C Intensity (If)=3.5A Time (on/off)=300s/300s	77	500h				0/77
Wire Bond Strength		MIL-STD-750 Method 2037	Pre and Post change 10 bonds from minimum 5parts	58	-	0/10	0/8	0/10	0/30
Bond Shear		AEC-Q101-003	10 bonds from minimum 5parts	58	-	0/10	0/8	0/10	0/30
Die Shear		MIL-STD-750 Method 2037	Pre and Post change	10	-	0/10			

6 ANNEXES

6.1 Parametric Verifications and ESD

- Results on STPSC20H065CWLY product:

TEST	VR	VR	VR	IR	IR	IR
EQUIPMENT	TESEC_881TT_TEST292					
UNIT	-40°C	25°C	150°C	-40°C	25°C	150°C
Condition 1				VR=650V	VR=650V	VR=650V
Condition 2						
Condition 3						
Min. Datasheet	650V	650V	650V			
Typ. Datasheet					9uA	85uA
Max. Datasheet					100uA	425uA
UNIT	V	V	V	nA	nA	uA
N	60	60	60	60	60	60
Min	900.900	910.400	932.000		19.950	0.877
Max	943.900	953.900	976.400		3973.000	11.090
Avg	929.387	939.210	961.568	No value due to frost issue	160.286	1.658

TEST	VF	VF	VF	RTH(J-C)	ESD_CDM	ESD_HBM
EQUIPMENT	TESEC_881TT_TEST292					
UNIT	-40°C	25°C	150°C	RTH(PHASE11) _MESU1150	ESD-CDM TEST SYSTEM	ESS6008
Condition 1	IF=10A	IF=10A	IF=10A		25°C	25°C
Condition 2						
Min. Datasheet						
Typ. Datasheet		1.45V	1.7V	1.25°C/W		
Max. Datasheet		1.65V	2.05V	1.50°C/W		
UNIT	V	V	V	°C/W	KV	KV
N	60	60	60	20	60	60
Min	1.497	1.456	1.650	0.988	>1.0	>8.0
Max	1.544	1.517	1.786	1.078	>1.0	>8.0
Avg	1.526	1.498	1.748	1.026		

- Results on STPSC10H065BY product:

TEST	VR	VR	VR	IR	IR	IR
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	-40°C	24°C	150°C	-40°C	24°C	150°C
Condition 2				VR=650V	VR=650V	VR=650V
Min. Datasheet	650V	650V	650V			
Typ. Datasheet					9uA	85uA
Max. Datasheet					100uA	425uA
UNIT	V	V	V	nA	nA	uA
N	30	30	30	30	30	30
Min	907.200	915.700	934.900		18.550	0.456
Max	937.200	946.200	969.500		625.600	2.690
Avg	920.390	929.123	951.547	No value due to frost issue	106.576	1.002

TEST	VF	VF	VF	RTH(J-C)	ESD_CDM	ESD_HBM
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	-40°C	24°C	150°C	RTH(PHASE11) _MESU1150	ESD-CDM TEST SYSTEM	ESS6008
Condition 2	IF=10A	IF=10A	IF=10A		25°C	23°C
Min. Datasheet						
Typ. Datasheet		1.45V	1.70V	1.25°C/W		
Max. Datasheet		1.65V	2.05V	1.50°C/W		
UNIT	V	V	V	°C/W	KV	KV
N	30	30	30	10	30	30
Min	1.453	1.425	1.579	0.883	>1.0	>8.0
Max	1.493	1.467	1.724	0.992	>1.0	>8.0
Avg	1.472	1.447	1.671	0.946		

- Results on STPSC20065DY product:

TEST	VR	VR	VR	IR	IR	IR
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	-40°C	23°C	150°C	-40°C	23°C	150°C
Condition 2				VR=650V	VR=650V	VR=650V
Min. Datasheet	650V	650V	650V			
Typ. Datasheet					30uA	280uA
Max. Datasheet					300uA	2000uA
UNIT	V	V	V	nA	uA	uA
N	30	30	30	30	30	30
Min	862.000	867.300	884.600	No value due to frost issue	0.336	3.347
Max	898.300	904.800	926.200		6.682	20.000
Avg	885.087	891.440	913.540		1.196	6.865

TEST	VF	VF	VF	RTH(J-C)	ESD_CDM	ESD_HBM
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	-40°C	23°C	150°C	RTH(PHASE11) _MESU1150	ESD-CDM TEST SYSTEM	ESS6008
Condition 2	IF=10A	IF=20A	IF=20A		23°C	23°C
Min. Datasheet		1.30V	1.45V	0.60°C/W		
Typ. Datasheet		1.45V	1.65V	0.90°C/W		
Max. Datasheet						
UNIT	V	V	V	°C/W	KV	KV
N	30	30	30	10	30	30
Min	1.189	1.299	1.390	0.514	>1.0	>8.0
Max	1.200	1.326	1.474	0.565	>1.0	>8.0
Avg	1.193	1.310	1.440	0.535		

6.2 Tests description

Test name	Description	Purpose
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
HTRB High Temperature Reverse	The diode is biased in static reverse mode at targeted junction temperature.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature.	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
DPA Destructive Physical Analysis	Specific construction analysis on random parts that have successfully completed H3TRB or TC.	To investigate on reliability stresses impact on delamination, corrosion and product construction integrity.
WBS Wire Bond Strength	To apply the specified stress to the bond, lead wire, or terminal.	To measure bond strength, evaluate bond strength distributions, or to determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermo-compression, ultrasonic, or related techniques
BS Bond Shear	This test establishes a procedure for determining the strength of the interface between a gold ball bond and a die bonding surface, or an aluminum wedge/stitch bond and a die or package bonding surface, on either pre-encapsulation or post-encapsulation components. This strength measurement is extremely important in determining two features: 1) the integrity of the metallurgical bond which has been formed. 2) the reliability of gold and aluminum wire bonds to die or package bonding surfaces. This test method can be used only when the ball height and diameter for ball bonds, or the wire height (1.25 mil and larger at the compressed bond area) for wedge/stitch bonds, are large enough and adjacent interfering structures are far enough away to allow suitable placement and clearance (e.g., above the bonding	To check the integrity of the metallurgical bond.
DS Die Shear	A sufficient force to shear the die from its mounting shall be applied to the die.	To establish the integrity of the semiconductor die attachment to the package header or other substrate.

Qualification Report

*Top & Back side metallization rationalization for
Automotive SiC diodes 650V in ST Catania*

General Information		Locations	
Product Line	Rectifiers	Wafer fab	ST Catania - ITALY
Product Description	Silicon Carbide Power Schottky	Assembly plant	ST Shenzhen - CHINA Subcontractor 994X - CHINA Subcontractor 998G - CHINA
Product perimeter	Refer to list page 4	Reliability Lab	ST TOURS - FRANCE
Product Group	ADG	Reliability assessment	PASS
Product division	Discrete & Filter		
Package	DPAK, D ² PAK, TO-220AB, TO-220AC, I ² PAK, DO247, TO247, TO247LL		
Maturity level step	QUALIFIED		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	30-Sept-2021	17	Christophe GOIN	Julien MICHELON	Initial release. Linked to PCN 13047.

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1	APPLICABLE AND REFERENCE DOCUMENTS	3
2	GLOSSARY	3
3	RELIABILITY EVALUATION OVERVIEW.....	4
3.1	OBJECTIVES.....	4
3.2	CONCLUSION.....	4
4	DEVICE CHARACTERISTICS	5
4.1	DEVICE DESCRIPTION.....	5
4.2	CONSTRUCTION NOTE.....	8
5	TESTS RESULTS SUMMARY	11
5.1	TEST VEHICLES	11
5.2	TEST PLAN	12
5.3	RESULTS SUMMARY	14
6	ANNEXES	15
6.1	PARAMETRIC VERIFICATIONS	15
6.2	TESTS DESCRIPTION	17

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101 Rev.D1	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices
AEC-Q005	Pb-Free Test Requirements

2 GLOSSARY

SS	Sample Size
PC	Pre-Conditioning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
H3TRB	High Humidity High Temperature Reverse Bias
IOLT	Intermittent Operating Life Test
UHAST	Unbiased Highly Accelerated Stress Test
GD	Generic Data
MSL	Moisture Sensitivity Level
T_j	Junction Temperature
BS	Bond Shear
DS	Die Shear
WBS	Wire Bond Strength
DPA	Destructive Physical Analysis (after TC and H3TRB)

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify Top & Back side metallization rationalization for 650V Silicon Carbide Power Schottky Rectifier products in ST Catania.

The involved products are listed in the table here below:

Product	Description	Package	Assembly Location	
STPSC6H065BY-TR	6 A, 650 V	DPAK	ST Shenzhen - China	
STPSC8H065BY-TR	8 A, 650 V			
STPSC10H065BY-TR	10 A, 650 V			
STPSC10H065GY-TR	10 A, 650 V			
STPSC20065GY-TR	20 A, 650 V	D ² PAK	ST Shenzhen - China	
STPSC8H065G2Y-TR	8 A, 650 V			
STPSC20065WY	20 A, 650 V	DO-247	Subcontractor China (998G)	
STPSC20H065CWY	2x10 A, 650 V	TO-247		
STPSC40065CWY	2x20 A, 650 V			
STPSC20H065CTY	2x10 A, 650 V	TO-220AB		
STPSC10H065DY	10 A, 650 V	TO-220AC	Subcontractor China (998G)	
STPSC6C065DY	6 A, 650 V			
STPSC20065DY	20 A, 650 V			
STPSC10C065RY	10 A, 650 V	I ² PAK	Subcontractor China (998G)	
STPSC20H065CWLY	20 A, 650 V	TO247LL		

The reliability test methodology used follows the JESD47: « Stress Test riven Qualification Methodology » and AECQ-101 RevD1 guidelines.

The following reliability tests ensuing are:

- TC and IOLT to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

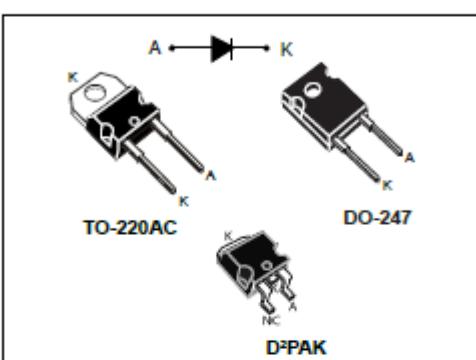
4.1 Device description

Refer to ST specification (examples below for STPSC20065-Y, STPSC10H065BY and STPSC20H065CWLY):

STPSC20065-Y

Automotive 650 V power Schottky silicon carbide diode

Datasheet - production data



Description

The SiC diode is an ultra high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Especially suited for use in PFC applications, this ST SiC diode will boost performance in hard switching conditions. Its high forward surge capability ensures good robustness during transient phases.

Features

- AEC-Q101 qualified
- No reverse recovery charge in application current range
- Switching behavior independent of temperature
- Dedicated to PFC applications
- High forward surge capability
- ECOPACK®2 compliant component
- PPAP capable
- Operating T_j from -40 °C to 175 °C

Table 1: Device summary

Symbol	Value
$I_{F(AV)}$	20 A
V_{RRM}	650 V
T_j (max.)	175 °C
V_F (typ.)	1.30 V

Automotive 650 V power Schottky silicon carbide diode

**Features**

- AEC-Q101 qualified
- No reverse recovery charge in application current range
- Switching behavior independent of temperature
- Recommended to PFC applications
- PPAP capable
- ECOPACK®2 compliant component

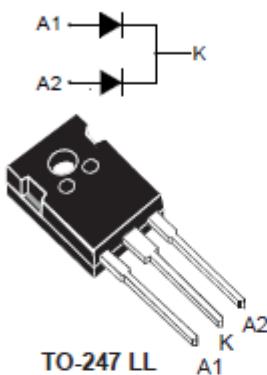
Description

The SiC diode is an ultra-high performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature.

Especially suited for use in PFC applications, this ST SiC diode will boost performance in hard switching conditions.

Product status	
STPSC10H065BY-TR	
Product summary	
Symbol	Value
$I_{F(AV)}$	10 A
V_{RRM}	650 V
$T_{J(max.)}$	175 °C

Automotive 20 A 650 V power Schottky silicon carbide diode



Features



- AEC-Q101 qualified
- PPAP capable
- No or negligible reverse recovery
- Switching behavior independent of temperature
- Dedicated to PFC applications
- High forward surge capability
- ECOPACK² compliant component

Applications

- On board charger (OBC)
- Charging stations
- PFC applications
- UPS
- Inverters
- Telecom power supplies

Description

The STPSC20H065CWLY is an ultra-high-performance power Schottky diode. It is manufactured using a silicon carbide substrate. The wide band gap material allows the design of a Schottky diode structure with a 650 V rating. Due to the Schottky construction, no recovery is shown at turn-off and ringing patterns are negligible. The minimal capacitive turn-off behavior is independent of temperature and are ideal for automotive applications.

Especially suited for use in PFC applications, UPS, inverters, telecom power supplies and battery chargers (either integrated in the vehicle or in a charging station), this diode will enhance the performance of the targeted application. Its high forward surge capability ensures a good robustness during transient phases.

Product status link	
STPSC20H065CWLY	
Product summary	
$I_{F(AV)}$	2 x 10 A
V_{RRM}	650 V
T_J (max.)	175 °C
V_F (typ.)	1.45 V
Product label	
	

4.2 Construction Note

STPSCxxH065BY-TR	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	DPAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSCxxH065GY-TR	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	D ² PAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20065WY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	DO-247
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CWY - STPSC40065CWY

Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-247
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CTY

Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-220AB
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSCxxH065DY - STPSCxx065DY

Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	TO-220AC
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

STPSC20H065CWLY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST subcontractor – China (998G)
Package description	TO-247LL
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST subcontractor – China (998G)

STPSC10C065RY	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania – Italy
Technology / Process family	SiC Power Schottky Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Catania – Italy
Assembly information	
Assembly site	ST Shenzhen – China
Package description	I ² PAK
Molding compound	ECOPACK®2
Lead finishing	Lead free (Pure Tin)
Final testing information	
Testing location	ST Shenzhen – China

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Comments
L1	STPSC10H065BY	DPAK	Qualification lot 1 – back side metallization
L2	STPSC20H12CWY	TO247	Qualification lot 2 – back side metallization
L3	STPSC40H12CWL	TO247LL	Qualification lot 3 – back side metallization
L4	STPSC10H12B	DPAK	Qualification lot 4 – back side metallization
L5	STPSC20065G	D2PAK	Qualification lot 5 – front side metallization
L6	STPSC10H065B	DPAK	Qualification lot 6 – front side metallization
L7	STPSC15H12DY	TO-220	Qualification lot 7 – front side metallization
L8	STPS20H065CWLY	TO247LL	Qualification lot 8 – front & back side metallization

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard specification	All qualification parts tested per the requirements of the appropriate device specification			X
Pre-conditioning	PC	JESD22A-113	All qualification parts tested per the requirements of the appropriate device specification		As per targeted MSL	X
MSL research	MSL	J-STD-020	L1, L4	60		X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	All qualification parts tested per the requirements of the appropriate device specification			X
High Temperature Storage Life	HTSL	JESD22B-101			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
High Temperature Gate Bias	HTGB	JESD22A-108			Required for PowerMOSFET – IGBT only.	
High Temperature Reverse Bias	HTRB	JESD22A-108			Not applicable for metallization change	
High Temperature Forward Bias	HTFB	JESD22A-108			Not required, applicable only to LEDs	
High Temperature Operating Life Test	HTOL	JESD22A-108			Covered by HTRB.	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test B			Required for Voltage Regulator (Zener) only.	
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test A			Required for Thyristor only.	
Temperature Cycling	TC	JESD22A-104	L1, L2, L4, L5, L6, L7, L8	539		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET – IGBT only.	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118			Covered by H3TRB	
Autoclave	AC	JESD22A-102			Not recommended	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1, L2, L3, L8	308		X
High Temperature High Humidity Bias	HTHBB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	L1, L3, L8	231	For power devices.	X
Power and Temperature Cycle	PTC	JED22A-105			Covered by IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005			Not required for metallization change	
ESD Characterization	ESD CDM	AEC Q101-001 and 005			Not required for metallization change	

Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	L1	4	After H3TRB and TC. For automotive products only	X
Physical Dimension	PD	JESD22B-100			Not relevant for wafer production and test qualification	
Terminal Strength	TS	MIL-STD-750 Method 2036			Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	L1, L4	60	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	X
Solderability	SD	J-STD-002 JESD22B102			Not relevant for wafer production and test qualification	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate			Required in case of process change.	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	L5, L6, L7, L8	60	Covered during workability trials	X
Bond Shear	BS	AEC-Q101-003	L5, L6, L7, L8	60	Covered during workability trials	X
Die Shear	DS	MIL-STD-750 Method 2017	L1, L2, L3, L4	60	Not Applicable to parts with solder paste die attach	X
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET – IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201			Not relevant for wafer production and test qualification	
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Low Temperature Storage	LTS	JESD-22 A119: 209			AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104			AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037			AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037			AQG324 test for Modules	
Mechanical shock	MS	IEC 60068-2-27			AQG324 test for Modules	
Vibration	V	IEC60068-2-6			AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Total	Steps	Results/Lot Fail/S.S.							
						Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	Lot 8
Parametric Verifications		ST datasheet	Over part temperature range	120	-	Refer to paragraph 6.1 in Annexes							
External Visual Inspection		JESD22 B-101	-	830	-	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process							
Pre and Post Electrical Test		ST datasheet	I_R , V_F parameters following product datasheet	1138	-	0/1061							
PC		JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	462	-	0/462							
MSL1 research	N	JESD22 A-113	MSL=1 Reflow=3 Temperature=85°C Humidity (HR)=85%	60	-	0/30			0/30				
TC	Y	JESD22-A104	Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	308	1000c	0/77			0/77	0/77	0/77		
	N		Frequency (cy/h)=2cy/h Temperature (high)=150°C Temperature (low)=-65°C	231	1000c		0/77					0/77	0/77
DPA after TC	Y	AEC-Q101	DPA after 1000c of TC	2	-	0/2							
H3TRB	Y	JESD22-A101	Humidity (HR)=85% Temperature=85°C Voltage=100V	77	1000h	0/77							
	N			231	1000h		0/77	0/77					0/77
DPA after H3TRB	Y	AEC-Q101	DPA after 1000h of H3TRB	2	-	0/2							
IOLT	Y	MIL-STD 750 Method 1037	Delta T_j =100°C Intensity (If)=2.1A Time (off)=120s Time (on)=120s	77	1000h	0/77							
	N		Delta T_j =100°C Intensity (If)=2A Time (off)=120s Time (on)=120s	154	1000h			0/77					0/77
RSH	N	JESD22A-111 (SMD) / JESD22B-106 (PTH)	Temperature=260°C Time (on)=10s	60	-	0/30			0/30				
Die Shear		MIL-STD-750 Method 2017	Pre and Post change	60	-	0/15	0/15	0/15	0/15				
Wire Bond Strength		MIL-STD-750 Method 2037	10 bonds from minimum 5 parts	60	-					0/10	0/10	0/10	0/30
Bond Shear		AEC-Q101-003	10 bonds from minimum 5 parts	60	-					0/10	0/10	0/10	0/30

6 ANNEXES

6.1 Parametric Verifications

- Results on STPSC10H065BY product (Back side metallization rationalization):

TEST	VBR	IR	VF	RTH(J-C)
EQUIPMENT	TESEC_881TT_TEST292			MESU1150
Condition 1	24°C	24°C	24°C	
Condition 2		VR=650V	IF=10A	
Min. Datasheet	650V			
Typ. Datasheet		9uA	1.45V	1.25°C/W
Max. Datasheet		100uA	1.65V	1.50°C/W
UNIT	V	uA	V	°C/W
N	30	30	30	10
Min	914.300	0.045	1.393	0.972
Max	934.200	15.400	1.526	1.117
Moy.	927.883	4.051	1.428	1.060

- Results on STPSC20065D product (Back side metallization rationalization):

TEST	VBR	IR	IR	VF	RTH(J-C)
EQUIPMENT	TESEC_881TT_TEST292			MESU1150	
Condition 1	25°C	25°C	25°C	25°C	
Condition 2		VR=600V	VR=650V	IF=20A	
Min. Datasheet	650V				
Typ. Datasheet		15uA	30uA	1.30V	0.60°C/W
Max. Datasheet		150uA	300uA	1.45V	0.90°C/W
UNIT	V	nA	nA	V	°C/W
N	30	30	30	30	10
Min	874.400	126.500	329.100	1.320	0.528
Max	920.200	1743.000	3806.000	1.344	0.596
Moy.	883.327	336.570	838.530	1.326	0.558

- Results on STPSC10H065B product (Front side metallization rationalization):

TEST	VBR	IR	IR	VF	VF
EQUIPMENT	TESEC_881TT_TEST292				
Condition 1	25°C	25°C	150°C	25°C	150°C
Condition 2		VR=650V	VR=650V	IF=10A	IF=10A
Min. Datasheet	650V				
Typ. Datasheet		9uA	85uA	1.56V	1.98V
Max. Datasheet		100uA	425uA	1.75V	2.5V
UNIT	V	nA	uA	V	V
N	30	30	15	30	15
Min	932.200	22.350	0.588	1.450	1.650
Max	958.500	3456.000	2.986	1.682	1.855
Avg	943.603	262.980	1.033	1.518	1.736

- Results on STPSC20065GY product (Front side metallization rationalization):

TEST	VBR	IR	IR	IR	VF	VF
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	25°C	25°C	25°C	150°C	25°C	150°C
Condition 2		VR=600V	VR=650V	VR=650V	IF=20A	IF=20A
Min. Datasheet	650V					
Typ. Datasheet		15uA	30uA	280uA	1.30V	1.45V
Max. Datasheet		150uA	300uA	2000uA	1.45V	1.65V
UNIT	V	uA	uA	uA	V	V
N	30	30	30	15	30	15
Min	857.700	0.102	0.268	2.849	1.311	1.447
Max	921.000	9.135	16.340	131.600	1.340	1.486
Avg	898.960	1.162	2.336	28.572	1.319	1.467

- Results on STPSC20065D product (Front & Back side metallization rationalization):

TEST	VRRM	VRRM	VRRM	VF	VF	VF
EQUIPMENT	TESEC_881TT_TEST292					
Condition 1	-40°C	25°C	150°C	-40°C	25°C	150°C
Condition 2				IF=20A	IF=20A	IF=20A
Min. Datasheet	650V	650V	650V			
Typ. Datasheet					1.30V	1.45V
Max. Datasheet					1.45V	1.65V
UNIT	V	V	V	V	V	V
N	30	30	30	30	30	30
Min	829.300	827.300	852.000	1.336	1.308	1.412
Max	904.400	913.500	931.400	1.370	1.345	1.499
Avg	886.050	891.350	910.390	1.349	1.325	1.469

TEST	IR	IR	IR	IR
EQUIPMENT	TESEC_881TT_TEST292			
Condition 1	-40°C	25°C	25°C	150°C
Condition 2	VR=650V	VR=600V	VR=650V	VR=650V
Min. Datasheet				
Typ. Datasheet		15uA	30uA	280uA
Max. Datasheet		150uA	300uA	2000uA
UNIT	nA	nA	nA	uA
N	30	30	30	30
Min	No value due to frost issue	98.200	282.100	2.480
Max		2049.000	3847.000	20.230
Avg		305.614	707.173	4.689

6.2 Tests description

Test name	Description	Purpose
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
HTRB High Temperature Reverse	The diode is biased in static reverse mode at targeted junction temperature.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
IOLT Intermittent Operating Life Test	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature.	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
DPA Destructive Physical Analysis	Specific construction analysis on random parts that have successfully completed H3TRB or TC.	To investigate on reliability stresses impact on delamination, corrosion and product construction integrity.
WBS Wire Bond Strength	To apply the specified stress to the bond, lead wire, or terminal.	To measure bond strength, evaluate bond strength distributions, or to determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermo-compression, ultrasonic, or related techniques
BS Bond Shear	This test establishes a procedure for determining the strength of the interface between a gold ball bond and a die bonding surface, or an aluminum wedge/stitch bond and a die or package bonding surface, on either pre-encapsulation or post-encapsulation components. This strength measurement is extremely important in determining two features: 1) the integrity of the metallurgical bond which has been formed. 2) the reliability of gold and aluminum wire bonds to die or package bonding surfaces. This test method can be used only when the ball height and diameter for ball bonds, or the wire height (1.25 mil and larger at the compressed bond area) for wedge/stitch bonds, are large enough and adjacent interfering structures are far enough away to allow suitable placement and clearance (e.g., above the bonding)	To check the integrity of the metallurgical bond.
DS Die Shear	A sufficient force to shear the die from its mounting shall be applied to the die.	To establish the integrity of the semiconductor die attachment to the package header or other substrate.



Public Products List

Public Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Wafer Manufacturing & EWS capacity extension in ST Singapore for Automotive SiC 650V products

PCN Reference : ADG/21/13047

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STPSC8065DY	STPSC12065DY	STPSC10H065BY-TR
STPSC20H065CWLY	STPSC12065GY-TR	STPSC8H065G2Y-TR
STPSC6H065BY-TR	STPSC10065GY-TR	STPSC20H065CTY
STPSC10H065GY-TR	STPSC20H065CWY	STPSC10C065RY
STPSC20065GY-TR	STPSC2H065BY-TR	STPSC12065G2Y-TR
STPSC40065CWY	STPSC10H065DY	STPSC20065DY
STPSC20065WY	STPSC10065DY	STPSC8H065BY-TR
STPSC12H065DY	STPSC6C065DY	STPSC12C065DY



IMPORTANT NOTICE – PLEASE READ CAREFULLY

Subject to any contractual arrangement in force with you or to any industry standard implemented by us, STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved