PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/21/13027
1.3 Title of PCN	Molding compound change for ESDZV5-1BU2 & ESDZV5H-1BU2
1.4 Product Category	ST Shenzhen
1.5 Issue date	2021-09-27

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Stephane CHAMARD
2.1.2 Marketing Manager	Philippe LEGER
2.1.3 Quality Manager	Jean-Paul REBRASSE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Materials	New direct material part number (same supplier, different supplier or new supplier), Mold compound	ST Shenzhen

4. Description of change		
	Old	New
4.1 Description	Samsung resin	Nagase resin
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No	

5. Reason / motivation for change	
5.1 Motivation	Product discontinuity from current molding compound supplier
5.2 Customer Benefit	SERVICE CONTINUITY

6. Marking of parts / traceability of change	
6.1 Description	New Finished Good/Type print on carton labels, and also by marking orientation with 180° rotation.

7. Timing / schedule	
7.1 Date of qualification results	2021-09-20
7.2 Intended start of delivery	2021-12-27
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13027 21078QRP-Rev1.0.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-09-27

9. Attachments (additional documentations)

13027 Public product.pdf
13027 Molding ESDZV5-1BU2 ESDZV5H-1BU2.pdf
13027 21078QRP-Rev1.0.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	ESDZV5H-1BU2	

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Qualification Report

Molding compound change

ESDZV5-1BU2 & ESDZV5H-1BU2

General Information	
Product Line	*Protection*
Product Description	*Ultra low clamping single line bidirectional ESD protection*
Product Perimeter	*ESDZV5-1BU2* *ESDZV5H-1BU2*
Product Group	*ADG*
Product Division	*Discrete & Filter*
Packages	*0201 package*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST ANG MO KIO - SINGAPORE*
Assembly Plant	*ST SHENZHEN – CHINA*
Reliability Lab	*ST TOURS – FRANCE*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	17-sept-2021	12	Aude DROMEL	Julien MICHELON	Initial release

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

H3TRB	High Humidity High Temperature Reverse Bias
HTRB	High Temperature Reverse Bias
PC	Preconditioning
PD	Physical Dimensions
PV	Parametric Verification
RS	Repetitive Surges
SS	Sample Size
TC	Temperature Cycling
HTSL	High Temperature Storage Life
UHAST	Unbiased Highly Accelerated Stress Test

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify new molding compound for ESDZV5-1BU2 and ESDZV5H-1BU2 embedded in 0201 package.

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology » .

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

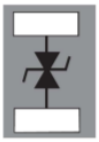
life.augmented

ESDZV5-1BU2

Datasheet

Ultra low clamping single line bidirectional ESD protection

0201 package



Features

- Ultra low clamping voltage: 8 V (IEC 61000-4-2 contact discharge 8 kV at 30 ns/ 16 A TLP)
- Bidirectional device
- Low leakage current
- 0201 package
- ECOPACK2 compliant component
- Complies with IEC 61000-4-2 level 4
  - ±30 kV (air discharge)
  - ±20 kV (contact discharge)

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Product status
ESDZV5-1BU2

Description

The ESDZV5-1BU2 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where reduced line capacitance and board space saving are required.

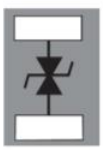
life.augmented

ESDZV5H-1BU2

Datasheet

Ultra low clamping single line bidirectional ESD protection

0201 package



Features

- Ultra low clamping voltage:
  - 10 V (IEC 61000-4-2 contact discharge 8 kV at 30 ns/ 16 A TLP)
- Bidirectional and symmetrical device
- High holding voltage for DC line protection
- 0201 package
- ECOPACK2 compliant component
- Complies with IEC 61000-4-2 level 4
  - ±30 kV (air discharge)
  - ±14 kV (contact discharge)

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Product status link
ESDZV5H-1BU2

Product summary	
Order code	ESDZV5H-1BU2
Package	ST0201
Packing	Tape and reel

Description

The ESDZV5H-1BU2 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where reduced line capacitance and board space saving are required.

4.2 Construction Note

	ESDZV5-1BU2 & ESDZV5H-1BU2
Wafer/Die fab. information	
Wafer fab manufacturing location	ST ANG MO KIO - SINGAPORE
Technology / Process family	Ultra low clamping single line bidirectional ESD protection
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST ANG MO KIO - SINGAPORE
Assembly information	
Assembly site	ST SHENZHEN-CHINA
Package description	0201 PACKAGE
Molding compound	ECOPACK®2 (“Halogen-free”) molding compound
Lead finishing material	Not Applicable
Final testing information	
Testing location	ST SHENZHEN-CHINA

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Finish Good	Assy plant Location	Comments
L1	ESDZV5-1BU2	0201	ESDZV5-1BU2V/C7	ST SHENZHEN	1st Qualification lot
L2	ESDZV5H-1BU2		ESDZV5H-1BU2V/C7		2nd Qualification lot
L3					3rd Qualification lot
L4					4th Qualification lot

GD: Test vehicles used for similarity.

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL Not applicable for PTH and WLCSP without coating	X
MSL research	MSL	J-STD-020	L2	30	Not applicable for PTH and WLCSP without coating	X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L2	30		X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L1, L2, L3, L4	4x77	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A			Required for Thyristor only. Alternative to HTRB	
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for PowerMOSFET – IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104	L1, L2, L3, L4	4x77		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET – IGBT only. Alternative to TCHT	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101	L1	77	Required for SCR/TRIAC RECTIFIER and Protection devices	X
Autoclave	AC	JESD22A-102	Lx or GDx	xx	Alternative to UHAST	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB (same failure mechanisms activation).	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1, L2, L3, L4	4x77	Alternative to HAST	X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	
Power and Temperature Cycle	PTC	JED22A-105	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if $\Delta Tj>100°C$ cannot be achieved with IOL Alternative to IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005	Lx or GDx	xx	Only for automotive products	
ESD Characterization	ESD CDM	AEC Q101-001 and 005	Lx or GDx	xx	Only for automotive products	
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	Lx or GDx	xx	After H3TRB and TC Only for automotive products	
Physical Dimension	PD	JESD22B-100	L1, L2	2x30		X
Terminal Strength	TS	MIL-STD-750 Method 2036	Lx or GDx	xx	Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	Lx or GDx	xx	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102	Lx or GDx	xx	Not applicable as no leads	
Dead Bug Test	DBT	ST Internal specification	Lx or GDx	xx	Mandatory for SMD package Data collection for PTH package	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	Lx or GDx	xx	Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	Lx or GDx	xx	No wires	
Bond Shear	BS	AEC-Q101-003	Lx or GDx	xx	No wires	
Die Shear	DS	MIL-STD-750 Method 2017	Lx or GDx	xx	Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET - IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201	Lx or GDx		No leads	
Early Life Failure Rate	ELFR	JESD74	Lx or GDx	xx	Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,...)	FT	Internal specification	Lx or GDx	xx		
Repetitive Surge	RS	Internal specification	Lx or GDx	xx	Required for protection devices only.	

Low Temperature Storage	LTS	JESD-22 A119: 209	Lx or GDx	xx	AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27	Lx or GDx	xx	AQG324 test for Modules	
Vibration	V	IEC60068-2-6	Lx or GDx	xx	AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS			
						L1	L2	L3	L4
Pre- and Post-Electrical Test	-	ST datasheet	Ir, Vf,parameters following product datasheet	-		0/1339			
PC (for SMD packages)	-	JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	-	770	0/308	0/154	0/154	0/154
MSL1 research (for SMD packages)	N	JESD22-A113	MSL=1 Reflow=3 Temperature=85°C Humidity (HR)=85%	-	30		0/30		
External Visual	-	JESD22 B-101	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process						
Parametric Verification	-	ST datasheet	Over part temperature range (note 1)	-	30	Refer to paragraph 6.1 in Annexes			
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=150°C VR=5.5V	1Khrs	308	0/77	0/77	0/77	0/77
HTSL	N	JESD22 A-103	150°C	1Khrs	308	0/77	0/77	0/77	0/77
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	500cy	308	0/77	0/77	0/77	0/77
UHAST	Y	JESD22 A-118	130°C; 85% RH 2.3bar	96hrs	77	0/77			
H3TRB (Alt to HAST)	Y	JESD22 A-101	85°C; 85% RH VR=80% VRRM (with 100V max.)	1Khrs	308	0/77	0/77	0/77	0/77
PD	-	JESD22 B-100	-	-	30	Refer to paragraph 6.X in Annexes			

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

6 ANNEXES

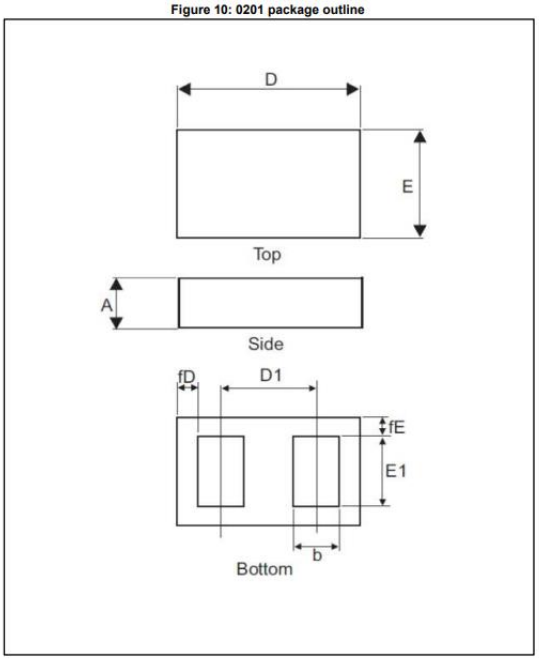
6.1 Parametric Verification

ESDZV5H-1BU2	IR at VRM= 5.5V at 25°C (ST datasheet: 50 nA Max.)			VTrig at 25°C (ST datasheet: 6.5 V min, 10 V Max)			VH at 25°C (ST datasheet: 5.5 V Min.)		
	Min.	Avg.	Max.	Min.	Avg.	Max.	Min.	Avg.	Max.
Current Finish Good ESDZV5H-1BU2T/C7	0.31 nA	0.62 nA	0.77 nA	7.45 V	7.64 V	7.76 V	5.92 V	5.97 V	6 V
New Finish Good ESDZV5H-1BU2V/C7	0.30 nA	0.52 nA	0.88 nA	7.29 V	7.35 V	7.77 V	5.79 V	5.83 V	5.87 V

ESDZV5H-1BU2	VCL @ IPP= 4V (direct) at 25°C (ST datasheet: 11 V Max.)			VCL @ IPP= 4V (reverse) at 25°C (ST datasheet: 11 V Max.)			CLine at 25°C (ST datasheet: 5pF Max.)		
	Min.	Avg.	Max.	Min.	Avg.	Max.	Min.	Avg.	Max.
Current Finish Good ESDZV5H-1BU2T/C7	9.52 V	9.59 V	9.68 V	9.68 V	9.73 V	9.84 V	3.57 pF	3.59 pF	3.61 pF
New Finish Good ESDZV5H-1BU2V/C7	9.16 V	9.23 V	9.4 V	9.24 V	9.34 V	9.48 V	3.8 pF	3.88 pF	4 pF

6.2 Physical Dimensions

Figure 10: 0201 package outline



ESDZV5-1BU2T/C7 (Current)						
Dimensions in mm		A	b	D	E	E1
ST datasheet	Min	0.210	0.140	0.560	0.250	0.170
	Max	0.270	0.200	0.610	0.310	0.230
Min.		0.237	0.182	0.578	0.278	0.209
Max.		0.243	0.188	0.584	0.285	0.216
Avg.		0.240	0.184	0.581	0.282	0.212

ESDZV5-1BU2V/C7 (New)						
Dimensions in mm		A	b	D	E	E1
ST datasheet	Min	0.210	0.140	0.560	0.250	0.170
	Max	0.270	0.200	0.610	0.310	0.230
Min.		0.247	0.168	0.575	0.277	0.191
Max.		0.270	0.200	0.600	0.310	0.230
Avg.		0.249	0.170	0.577	0.279	0.194

ESDZV5H-1BU2T/C7 (Current)						
Dimensions in mm		A	b	D	E	E1
ST datasheet	Min	0.210	0.140	0.550	0.250	0.170
	Max	0.270	0.200	0.610	0.310	0.230
Min.		0.224	0.168	0.576	0.279	0.190
Max.		0.248	0.172	0.582	0.283	0.198
Avg.		0.245	0.170	0.580	0.280	0.194

ESDZV5H-1BU2V/C7 (New)						
Dimensions in mm		A	b	D	E	E1
ST datasheet	Min	0.210	0.140	0.560	0.250	0.170
	Max	0.270	0.200	0.600	0.310	0.230
Min.		0.242	0.177	0.580	0.283	0.202
Max.		0.255	0.184	0.586	0.293	0.211
Avg.		0.247	0.181	0.583	0.286	0.208

6.3 Tests description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias / **HTFB** High Temperature Forward Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations. Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
HTSL **High Temperature Storage Life**	The device is stored at controlled conditions of ambient temperature	To investigate failure mechanisms activated in the die-package environment by high temperature conditions, like migration/diffusion.

PCN
Product/Process Change Notification

Molding compound change for ESDZV5-1BU2 & ESDZV5H-1BU2

Notification number:	ADG/21/13027	**Issue Date**	23-Sep-2021
Issued by	Isabelle BALLON		
Product series affected by the change		ESDZV5-1BU2 ESDZV5H-1BU2	
Type of change		Back-End realization	

Description of the change

Change of molding compound

Reason for change

Product discontinuity from current molding compound supplier

Former versus changed product:	The changed products do not present modified electrical, dimensional, or thermal parameters, leaving unchanged the current information published in the product datasheets The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. Rationalization of the packing mode with no change in the standard delivery quantities. The products remain in full compliance with the ST ECOPACK®2 grade (so called “halogen-free”).

Disposition of former products

Delivery of the current products version will continue until the stock depletion.

Marking and traceability

Marking code is unchanged.
Traceability of the change will be ensured by new Finished Good/Type print on carton labels, and also by marking orientation with 180° rotation.

Commercial part number/Order code	Current Finished Good/Type	New Finished Good/Type
ESDZV5-1BU2	ESDZV5-1BU2T/C7	ESDZV5-1BU2V/C7
ESDZV5H-1BU2	ESDZV5H-1BU2T/C7	ESDZV5H-1BU2V/C7

Former	New
Example for ESDZV5H-1BU2T/C7	Example for ESDZV5H-1BU2V/C7
	

Qualification completion date	20-Sep-2021

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Protection	ESD protection	ESDZV5-1BU2	Week 45-2021
Protection	ESD protection	ESDZV5H-1BU2	Week 45-2021

For sample(s) request, please inform FSE (Field Sales Engineer) in order to insert corresponding **Non-Standard Samples Order** (a single Commercial Product for each request) with **PCN reference** as additional information.

Sales-types	Estimated production start	Estimated first shipments
ESDZV5-1BU2 ESDZV5H-1BU2	Oct-2021	Week 52-2021

Comments:	With early PCN acceptance, possible shipment starting Nov-2021.

(1) ADG: Automotive and Discrete Group

Customer's feedback Please contact your local ST sales representative or quality contact for requests concerning this change notification. Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change. Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change.	
Qualification program and results	21078QRP Attached

Qualification Report

Molding compound change

ESDZV5-1BU2 & ESDZV5H-1BU2

General Information	
Product Line	*Protection*
Product Description	*Ultra low clamping single line bidirectional ESD protection*
Product Perimeter	*ESDZV5-1BU2* *ESDZV5H-1BU2*
Product Group	*ADG*
Product Division	*Discrete & Filter*
Packages	*0201 package*
Maturity level step	*QUALIFIED*

Locations	
Wafer Fab	*ST ANG MO KIO - SINGAPORE*
Assembly Plant	*ST SHENZHEN – CHINA*
Reliability Lab	*ST TOURS – FRANCE*
Reliability Assessment	*PASS*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	17-sept-2021	12	Aude DROMEL	Julien MICHELON	Initial release

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

H3TRB	High Humidity High Temperature Reverse Bias
HTRB	High Temperature Reverse Bias
PC	Preconditioning
PD	Physical Dimensions
PV	Parametric Verification
RS	Repetitive Surges
SS	Sample Size
TC	Temperature Cycling
HTSL	High Temperature Storage Life
UHAST	Unbiased Highly Accelerated Stress Test

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify new molding compound for ESDZV5-1BU2 and ESDZV5H-1BU2 embedded in 0201 package.

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology » .

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.

For some tests, similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

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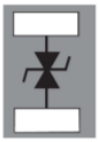
ESDZV5-1BU2

Datasheet

Ultra low clamping single line bidirectional ESD protection

0201 package



Features

- Ultra low clamping voltage: 8 V (IEC 61000-4-2 contact discharge 8 kV at 30 ns/ 16 A TLP)
- Bidirectional device
- Low leakage current
- 0201 package
- ECOPACK2 compliant component
- Complies with IEC 61000-4-2 level 4
  - ±30 kV (air discharge)
  - ±20 kV (contact discharge)

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Product status
ESDZV5-1BU2

Description

The ESDZV5-1BU2 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where reduced line capacitance and board space saving are required.

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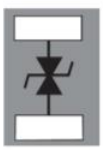
ESDZV5H-1BU2

Datasheet

Ultra low clamping single line bidirectional ESD protection

0201 package



Features

- Ultra low clamping voltage:
  - 10 V (IEC 61000-4-2 contact discharge 8 kV at 30 ns/ 16 A TLP)
- Bidirectional and symmetrical device
- High holding voltage for DC line protection
- 0201 package
- ECOPACK2 compliant component
- Complies with IEC 61000-4-2 level 4
  - ±30 kV (air discharge)
  - ±14 kV (contact discharge)

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Product status link
ESDZV5H-1BU2

Product summary	
Order code	ESDZV5H-1BU2
Package	ST0201
Packing	Tape and reel

Description

The ESDZV5H-1BU2 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where reduced line capacitance and board space saving are required.

4.2 Construction Note

	ESDZV5-1BU2 & ESDZV5H-1BU2
Wafer/Die fab. information	
Wafer fab manufacturing location	ST ANG MO KIO - SINGAPORE
Technology / Process family	Ultra low clamping single line bidirectional ESD protection
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST ANG MO KIO - SINGAPORE
Assembly information	
Assembly site	ST SHENZHEN-CHINA
Package description	0201 PACKAGE
Molding compound	ECOPACK®2 (“Halogen-free”) molding compound
Lead finishing material	Not Applicable
Final testing information	
Testing location	ST SHENZHEN-CHINA

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Finish Good	Assy plant Location	Comments
L1	ESDZV5-1BU2	0201	ESDZV5-1BU2V/C7	ST SHENZHEN	1st Qualification lot
L2	ESDZV5H-1BU2		ESDZV5H-1BU2V/C7		2nd Qualification lot
L3					3rd Qualification lot
L4					4th Qualification lot

GD: Test vehicles used for similarity.

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL Not applicable for PTH and WLCSP without coating	X
MSL research	MSL	J-STD-020	L2	30	Not applicable for PTH and WLCSP without coating	X
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L2	30		X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A (for diodes, rectifiers and Zeners) M1039 Method A (for transistors)	L1, L2, L3, L4	4x77	WBI after HTRB applicable only for dissimilar metal (wire/meta) in case of no Cu wire	X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A			Required for Thyristor only. Alternative to HTRB	
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDS Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACBV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for PowerMOSFET – IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104	L1, L2, L3, L4	4x77		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for PowerMOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for PowerMOSFET – IGBT only. Alternative to TCHT	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101	L1	77	Required for SCR/TRIAC RECTIFIER and Protection devices	X
Autoclave	AC	JESD22A-102	Lx or GDx	xx	Alternative to UHAST	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB (same failure mechanisms activation).	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1, L2, L3, L4	4x77	Alternative to HAST	X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts	
Power and Temperature Cycle	PTC	JED22A-105	Lx or GDx	xx	For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if $\Delta Tj>100°C$ cannot be achieved with IOL Alternative to IOL	
ESD Characterization	ESD HBM	AEC Q101-001 and 005	Lx or GDx	xx	Only for automotive products	
ESD Characterization	ESD CDM	AEC Q101-001 and 005	Lx or GDx	xx	Only for automotive products	
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	Lx or GDx	xx	After H3TRB and TC Only for automotive products	
Physical Dimension	PD	JESD22B-100	L1, L2	2x30		X
Terminal Strength	TS	MIL-STD-750 Method 2036	Lx or GDx	xx	Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	Lx or GDx	xx	Not applicable for SMD pitch < 0.5mm, package size > 5.5*12.5mm and die paddle > 2.5*3.5mm	
Solderability	SD	J-STD-002 JESD22B102	Lx or GDx	xx	Not applicable as no leads	
Dead Bug Test	DBT	ST Internal specification	Lx or GDx	xx	Mandatory for SMD package Data collection for PTH package	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	Lx or GDx	xx	Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	Lx or GDx	xx	No wires	
Bond Shear	BS	AEC-Q101-003	Lx or GDx	xx	No wires	
Die Shear	DS	MIL-STD-750 Method 2017	Lx or GDx	xx	Not Applicable to parts with solder paste die attach	
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for PowerMOSFET - IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201	Lx or GDx		No leads	
Early Life Failure Rate	ELFR	JESD74	Lx or GDx	xx	Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,...)	FT	Internal specification	Lx or GDx	xx		
Repetitive Surge	RS	Internal specification	Lx or GDx	xx	Required for protection devices only.	

Low Temperature Storage	LTS	JESD-22 A119: 209	Lx or GDx	xx	AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037	Lx or GDx	xx	AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27	Lx or GDx	xx	AQG324 test for Modules	
Vibration	V	IEC60068-2-6	Lx or GDx	xx	AQG324 test for Modules	

5.3 Results summary

Test	PC	Std ref.	Conditions	Steps / Duration	SS	Failure/SS			
						L1	L2	L3	L4
Pre- and Post-Electrical Test	-	ST datasheet	Ir, Vf,parameters following product datasheet	-		0/1339			
PC (for SMD packages)	-	JESD22 A-113	Drying 24hrs; 125°C Storage 168hrs; 85°C;85%RH IR reflow 3 times	-	770	0/308	0/154	0/154	0/154
MSL1 research (for SMD packages)	N	JESD22-A113	MSL=1 Reflow=3 Temperature=85°C Humidity (HR)=85%	-	30		0/30		
External Visual	-	JESD22 B-101	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process						
Parametric Verification	-	ST datasheet	Over part temperature range (note 1)	-	30	Refer to paragraph 6.1 in Annexes			
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=150°C VR=5.5V	1Khrs	308	0/77	0/77	0/77	0/77
HTSL	N	JESD22 A-103	150°C	1Khrs	308	0/77	0/77	0/77	0/77
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	500cy	308	0/77	0/77	0/77	0/77
UHAST	Y	JESD22 A-118	130°C; 85% RH 2.3bar	96hrs	77	0/77			
H3TRB (Alt to HAST)	Y	JESD22 A-101	85°C; 85% RH VR=80% VRRM (with 100V max.)	1Khrs	308	0/77	0/77	0/77	0/77
PD	-	JESD22 B-100	-	-	30	Refer to paragraph 6.X in Annexes			

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

6 ANNEXES

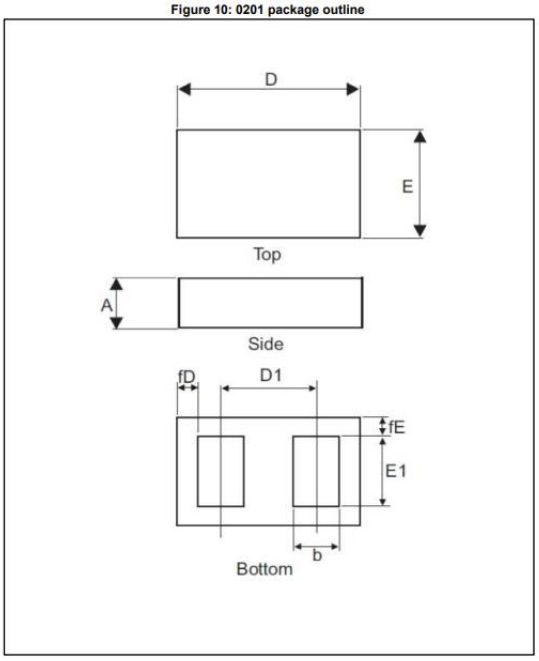
6.1 Parametric Verification

ESDZV5H-1BU2	IR at VRM= 5.5V at 25°C (ST datasheet: 50 nA Max.)			VTrig at 25°C (ST datasheet: 6.5 V min, 10 V Max)			VH at 25°C (ST datasheet: 5.5 V Min.)		
	Min.	Avg.	Max.	Min.	Avg.	Max.	Min.	Avg.	Max.
Current Finish Good ESDZV5H-1BU2T/C7	0.31 nA	0.62 nA	0.77 nA	7.45 V	7.64 V	7.76 V	5.92 V	5.97 V	6 V
New Finish Good ESDZV5H-1BU2V/C7	0.30 nA	0.52 nA	0.88 nA	7.29 V	7.35 V	7.77 V	5.79 V	5.83 V	5.87 V

ESDZV5H-1BU2	VCL @ IPP= 4V (direct) at 25°C (ST datasheet: 11 V Max.)			VCL @ IPP= 4V (reverse) at 25°C (ST datasheet: 11 V Max.)			CLine at 25°C (ST datasheet: 5pF Max.)		
	Min.	Avg.	Max.	Min.	Avg.	Max.	Min.	Avg.	Max.
Current Finish Good ESDZV5H-1BU2T/C7	9.52 V	9.59 V	9.68 V	9.68 V	9.73 V	9.84 V	3.57 pF	3.59 pF	3.61 pF
New Finish Good ESDZV5H-1BU2V/C7	9.16 V	9.23 V	9.4 V	9.24 V	9.34 V	9.48 V	3.8 pF	3.88 pF	4 pF

6.2 Physical Dimensions

Figure 10: 0201 package outline



ESDZV5-1BU2T/C7 (Current)						
Dimensions in mm		A	b	D	E	E1
ST datasheet	Min	0.210	0.140	0.560	0.250	0.170
	Max	0.270	0.200	0.610	0.310	0.230
Min.		0.237	0.182	0.578	0.278	0.209
Max.		0.243	0.188	0.584	0.285	0.216
Avg.		0.240	0.184	0.581	0.282	0.212

ESDZV5-1BU2V/C7 (New)						
Dimensions in mm		A	b	D	E	E1
ST datasheet	Min	0.210	0.140	0.560	0.250	0.170
	Max	0.270	0.200	0.610	0.310	0.230
Min.		0.247	0.168	0.575	0.277	0.191
Max.		0.270	0.200	0.600	0.310	0.230
Avg.		0.249	0.170	0.577	0.279	0.194

ESDZV5H-1BU2T/C7 (Current)						
Dimensions in mm		A	b	D	E	E1
ST datasheet	Min	0.210	0.140	0.550	0.250	0.170
	Max	0.270	0.200	0.610	0.310	0.230
Min.		0.224	0.168	0.576	0.279	0.190
Max.		0.248	0.172	0.582	0.283	0.198
Avg.		0.245	0.170	0.580	0.280	0.194

ESDZV5H-1BU2V/C7 (New)						
Dimensions in mm		A	b	D	E	E1
ST datasheet	Min	0.210	0.140	0.560	0.250	0.170
	Max	0.270	0.200	0.600	0.310	0.230
Min.		0.242	0.177	0.580	0.283	0.202
Max.		0.255	0.184	0.586	0.293	0.211
Avg.		0.247	0.181	0.583	0.286	0.208

6.3 Tests description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias / **HTFB** High Temperature Forward Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations. Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
HTSL **High Temperature Storage Life**	The device is stored at controlled conditions of ambient temperature	To investigate failure mechanisms activated in the die-package environment by high temperature conditions, like migration/diffusion.

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Molding compound change for ESDZV5-1BU2 & ESDZV5H-1BU2

PCN Reference : ADG/21/13027

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

ESDZV5H-1BU2	ESDZV5-1BU2	

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