PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/21/12751
1.3 Title of PCN	SPC572L64F2BC6AR / SPC572L64F2BC6AY (FE64): Transfer of Assembly and Final Testing to ST Muar Plant
1.4 Product Category	see list
1.5 Issue date	2021-05-07

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Luca RODESCHINI
2.1.2 Marketing Manager	Matteo MOIOLI
2.1.3 Quality Manager	Alberto MERVIC

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617)	ST Muar Plant (Malaysia) - receiving Plant

4. Description of change		
	Old	New
4.1 Description	Assembly and Final Testing in ST Malta Plant	Assembly and Final Testing in ST Muar Plant Transfer includes: - Implementation of High Density (HD) Leadframe - Implementation of 0.7 mil wires - Central top gate resin Injection - Marking re-layout
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact	

5. Reason / motivation for change	
5.1 Motivation	Capacity Improvement
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change	
6.1 Description	Dedicated Finished Good code (internal part number)

7. Timing / schedule	
7.1 Date of qualification results	2021-06-30
7.2 Intended start of delivery	2021-11-30
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	12751 FE64_Lavaredo_eTQFP80_Muar_Preliminary_Reliability_Report_RR001621_01_rev1.0.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2021-05-07

9. Attachments (additional documentations)
12751 Public product.pdf 12751 FE64_Lavaredo_eTQFP80_Muar_Preliminary_Reliability_Report_RR001621_01_rev1.0.pdf 12751 Details.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	SPC572L64F2BC6AR	

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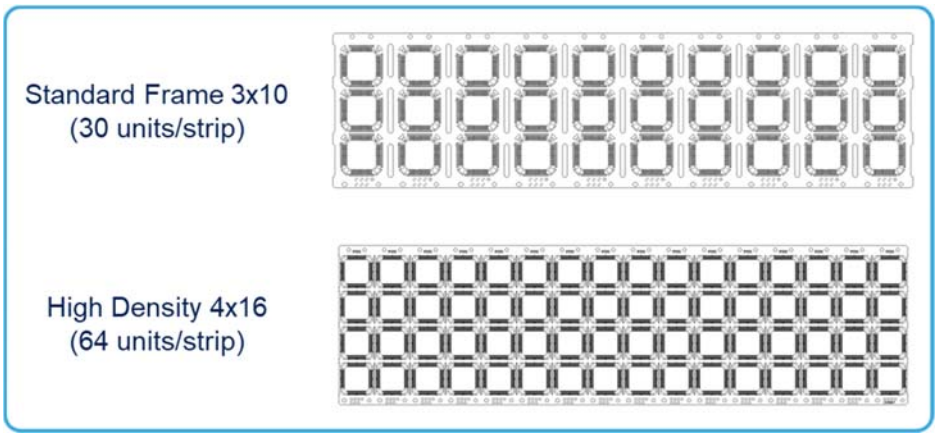
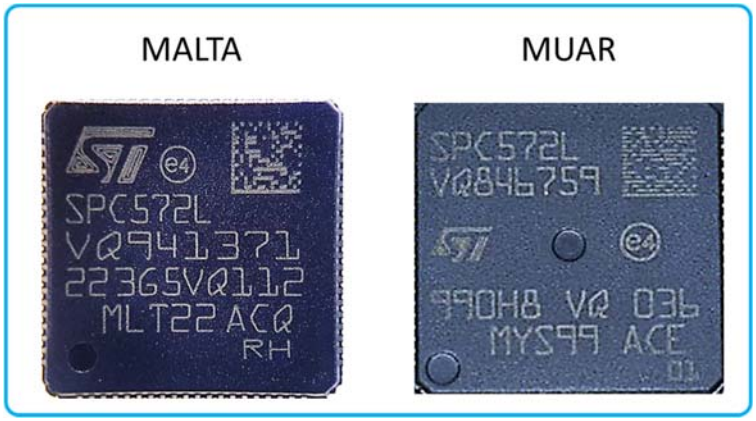
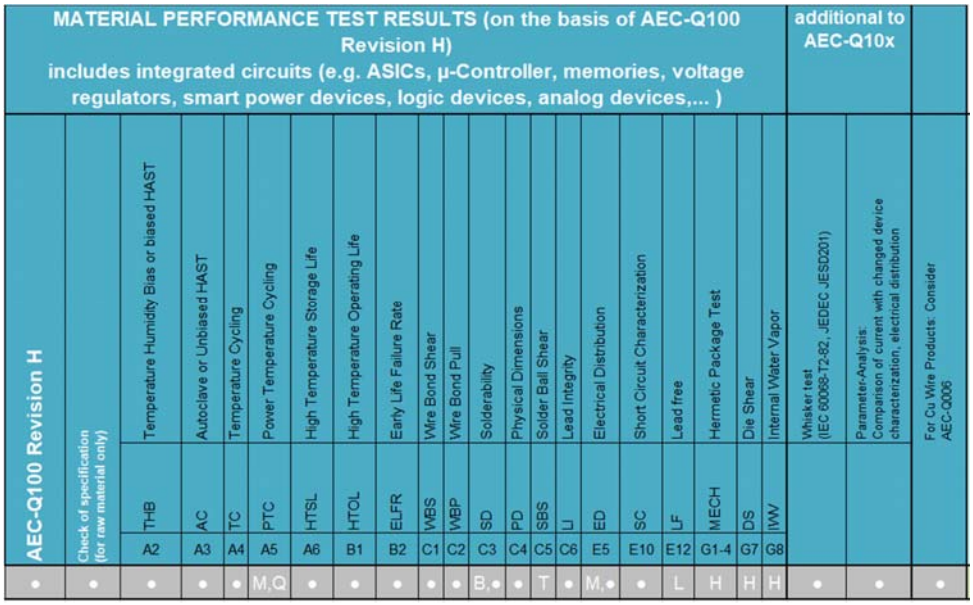
PRODUCT/PROCESS CHANGE NOTIFICATION

TITLE	**SPC572L64F2BC6AR / SPC572L64F2BC6AY (FE64): Transfer of Assembly and Final Testing to ST Muar Plant**
IMPACTED PRODUCTS	ST silicon line FE64 assembled in TQFP 80L 10X10X1.0 Exposed Pad package:
MANUFACT. STEP	Assembly and Electrical Final Test
INVOLVED PLANT	ST Muar Plant (Malaysia)
CHANGE REASON	Service – Capacity Improvement

CHANGE DESCRIPTION	Transfer of Back End related activities from ST Malta to ST Muar plant, including both assembly and electrical final test.
	Assembly transfer includeds specific product's improvements linked to new solutions and processes avaliability, such as:
	- Package Bill of Material:
	  o move to High Density (HD) leadframe (different supplier;
	  o move to 0.7mil wires diameter;
	- Molding Process: move to central top gate resin injection;
	- Marking: re-layout linked to central top gate mark.
	Final Test transfer does not concern changes in test flow or equipment.
	As far as assembly is concerned, additional details are here below provided.

Commercial Product	Current FG Code	New FG Code
SPC572L64F2BC6AR	572L64F2ABC6-ACR	572L64F2M0C6-ACR
SPC572L64F2BC6AY	572L64F2ABC6-ACY	572L64F2M0C6-ACY

	High Density (HD) Leadframe: increased number of units per strip, from 30 to 64 units/strip.  Unit level drawing (pad size, etc.) remains unchanged. Central Top Gate Mold Injection: reduces stress and possible wire sweeping during molding process. Package visual appearance is modified as follows: 
TRACEABILITY	Dedicated Finished Good code (internal part number)
VALIDATION	Full validation is in progress, based on ZVEI (AEC-Q100/Q006) recommendations corresponding to the following items: - SEM-PA-08 Change of wire bonding - SEM-PA-13 Change of product marking - SEM-PA-16 Change of direct material supplier

	▪ SEM-PA-18 Move all or parts of production to a different assembly site ▪ SEM-PA-21 Molding / Encapsulation process  With reference to the above qualification plan, following trials are not performed: ▪ ELFR: silicon related, not applicable to assembly changes; ▪ EM: silicon related, not applicable to assembly changes; ▪ LI: not applicable to surface mount packages; ▪ SC: not applicable to microcontrollers; ▪ SBS: not applicable to leadframe packages. <u>Electrical Final Test transfer</u> validation is based on standard correlation exercise (data comparison)
CURRENT PRODUCTS	Upon completion of the transition phase, products will be produced in Muar Plant only
REPORTS	Transfer validation is presently in progress. AEC-Q100 Reliability Report is attached. Complete set of qualification reports (including AEC-Q006 results) will be provided upon activity completion, foreseen by end of 2021Q2
IMPLEMENTATION	Change activation is proposed early 2021-Q4

Preliminary Reliability Report Lavaredo eTQFP80 Muar Assy M55

FAB transfer

General Information	
Product Line	*FE64*
Product Description	*Lavaredo 1.5M*
Product Group	*ADG*
Product division	*ADS*
Silicon process technology	*CMOS M55*

Locations	
Wafer fab location	*Crolles 2*
Final Assessment	
Reliability assessment	*Reliability trials on Lavaredo eTQFP80 assembled in Muar completed up to AEC-Q100 Grade 1 milestone with positive results. Extension required by Q006 ongoing*

DOCUMENT HISTORY

Version	Date	Author	Comment
1.0	09/04/2021	P.Epigrafi	First release. Preliminary results

RELEASED DOCUMENT

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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this document is to report the preliminary reliability trials results for Lavaredo Cut1.2 eTQFP80 assy transfer from Malta to Muar.

Lavaredo1.5M is processed in Crolles FAB using CMOS M55 technology (55nm technology with embedded Flash) and it is assembled in Malta-ST assy line in eTQFP80 and eTQFP100 packages with Cu wires.

Purpose of the change is to transfer Back End site from ST Malta to ST Muar plant.
Assembly transfer includes specific product improvements linked to new solutions and processes availability, such as:

- Package Bill of Material:
  - change from standard matrix to High Density (HD) matrix leadframe (different supplier) with increased number of units per strip. Unit level drawing (pad size, etc.) remains unchanged
  - change wire diameter from 0.8mils to 0.7mils
- Central top gate resin injection with the purpose to reduce stress and wire sweeping during molding process.

Qualification of Lavaredo 1.5M eTQFP80 assembled in Muar takes similarities with Velvety eTQFP64 assembled in Muar (Same Assy line), which is already in mass production in Muar since Q2 2020 (RR001120AG6050).
Full qualification performed on 1 assy lot of Lavaredo 1M5, due to different resin with respect to Velvety.
BOM comparison between Malta and Muar assy is reported in table at paragraph 1.4.

Assy reports are available for all qualification lots.

The qualification exercise for this change is in line with ZVEI Delta Qualification Matrix (ESD CDM performed in addition to ZVEI Requirements according to internal common practice) and it is in respect of AEC-Q100 rev.H Grade 1 and AEC-Q006 rev.A for copper wire qualification.

1.2 Conclusions

Preliminary results of reliability trials are presented.
AEC-Q100 rev. H Grade 1 milestone has been positively achieved on Lavaredo 1.5M eTQFP80 assembled in Muar.
Reliability trials are still ongoing to reach AEC-Q006 rev.A milestone.

1.3 Wafer fab information

DIE FEATURES	
Product Code	*FE64*
Diffusion Site	*Crolles 2*
Wafer Diameter (inches)	*12*
Process Technology	*CMOS M55*
Passivation	*PSG + Nitride*
Die finishing back side	*Lapped Silicon*

1.4 Package outline/Mechanical data

	Lavaredo eTQFP80 Malta Assy	*Lavaredo eTQFP80 Muar Assy*	*Velvety eTQFP64 Muar Assy*
Package Description	*TQFP-EP 80L 10X10X1.0 ExpadDown*	*TQFP-EP 80L 10X10X1.0 ExpadDown*	*TQFP-EP 64L 10X10X1.0 ExpadDown*
Assembly Site	*ST KIRKOP – MALTA*	*ST MUAR*	*ST MUAR*
Die Attach material	*QMI9507*	*QMI9507*	*QMI9507*
Molding compound	*G700LS*	*G700LS*	*G700SLS*
Substrate/Leadframe	*Preplated (TnPd3)*	*HD Pre-plated*	*HD Pre-plated*
Wires bonding materials/diameters	*Cu 0.8 mils*	*Cu 0.7mil*	*Cu 0.7mil*

1.5 Final testing information:

PACKAGE FEATURES		
Electrical Testing manufacturing location	**:**	ST MUAR
Tester	**:**	Teradyne J750

2 RELIABILITY PLAN AND TESTS RESULTS

2.1 Conditions

Room test temperature is 25°C
Hot test temperature is 150°C
Cold test temperature is -40°C

2.2 Tables entry legend

Symbol	How to read
☐	Action or condition has not to be considered
☒	The action/condition has been done/applied during the trial
N.P.	The trial or readout is not in the Qualification Plan and thus has not been performed
N.A.	Not applicable
N.C.	Trial not completed yet

2.3 Accelerated Environmental Stress Test (Q100 Group A)

Test			Step	Results eTQFP80	Notes
N	TEST NAME	CONDITIONS [SPEC]			
A1	**Pre Conditioning MSL 3**	[J-STD-020] ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Die visual inspection post trial ☒ 100 Temperature Cycles 24h bake@125°C, 192h@30°C/60%RH 3x Reflow simulation 260°C Peak Temp	**Pre/Post**	0/231 x 1 0/231 x 3 Velvety eTQFP64	Similarities with Velvety eTQFP64 assembled in Muar

A2	**THB** Temperature Humidity Bias	[JESD22-A101/A110] ☒ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section Ta=85°C, 85%RH, 1000hrs 2000hrs AEC-Q006	**1000 hrs**	0/77 x 1 0/77 x 3 Velvety eTQFP64	Similarities with Velvety eTQFP64 assembled in Muar
			2000hrs	N.C. 0/77 x 3 Velvety eTQFP64	
A3.a	**THS** Temperature Humidity Storage	[JESD22-A101/A110] ☒ After Jedec PC MSL3 ☒ Testing at Room ☐ Testing at Hot ☐ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post) ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section Ta=85°C, 85%RH, 1000hrs	**2000 hrs**	N.P.	
A3.b	**AC** Autoclave	[JESD22-A102/A118] ☒ After Jedec PC MSL3 ☒ Testing at Room ☐ Testing at Hot ☐ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section P=2.08atm Ta=121°C, 96hrs	**96 hrs**	0/77 x 1 0/77 x 3 Velvety eTQFP64	Similarities with Velvety eTQFP64 assembled in Muar

A4	**TC** Temperature Cycling	[JESD22-A104] ☒ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold ☒ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section Ta=-55°C /+150 °C, 1000cyc 2000cyc AEC-Q006	**1000cyc**	0/77 x 1 0/77 x 3 Velvety eTQFP64	Similarities with Velvety eTQFP64 assembled in Muar
			2000cyc	N.C. 0/77 x 3 Velvety eTQFP64	
A5	**PTC** Power Temperature Cycle	[JESD22-A105] ☒ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold Ta=-40°C /+125 °C 1000 cyc 2000cyc AEC-Q006	**2000cyc**	N.P.	Not required on Lavaredo

A6	**HTSL** High Temperature Storage Lifetime	[JESD22-A103] ☐ After Jedec PC MSL3 ☒ Testing at Room ☒ Testing at Hot ☐ Testing at Cold ☐ Sonoscan pre / post ☒ WPT pre / post ☒ WBS pre / post ☒ Visual Inspection ☒ Cross section Ta= 150ºC, 1000hrs 2000hrs AEC-Q006	**1000hrs**	0/77 x 1 0/77 x 3 Velvety eTQFP64	Similarities with Velvety eTQFP64 assembled in Muar
			2000hrs	N.C. 0/77 x 3 Velvety eTQFP64	

2.4 Accelerated Lifetime Simulation Test (Q100 Group B)

Test			Step	Results	Notes
N	**TEST NAME**	**CONDITIONS [SPEC]**		**Lots**	
1	**HTOL** High Temp. Operating Life	[JESD22-A108] ☐ After Jedec PC MSL3 ☒ After 1k W/E cyc @125°C ☒ Testing at Room, Hot, Cold ☒ Drift Analysis on Key parameters Ta=125ºC, Tj=150°C VDD+20% 168hrs (1000hrs monitor)	**168 hrs**	0/77 x 1	
2	**ELFR** Early Life Failure Rate	[AEC Q100-008] ☒ Testing at Room, Hot, Cold Ta= 125ºC, Tj=150°C BI+24 hrs	**BI +24hrs**	N.P.	Silicon stress trial, not significant for assembly changes.

3	**HTDR** High Temp. Data Retention	[AEC Q100-005] ☐ After Jedec PC MSL3 ☒ Testing at Room ☐ Testing at Hot ☐ Testing at Cold ☒ After 1k W/E cyc @125°C ☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 1000hrs	**1000 hrs**	N.P.	
4.a	**FET @25°C**	[AEC Q100-005] ☒ Testing at Room ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 25ºC 100k Write/Erase cyc	**100k cyc**	N.P.	
4.b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	N.P.	
5.a	**FET @125°C**	[AEC Q100-005] ☒ Testing at Room ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 125ºC 100k Write/Erase cyc	**100k cyc**	N.P.	
5.b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	N.P.	
6.a	**FET @-40°C**	[AEC Q100-005] ☒ Testing at Room ☒ Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= -40ºC 100k Write/Erase cyc	**100k cyc**	N.P.	
6.b	**HTDR After FET**	☒ Vth Drift Analysis Ta= 150ºC, All0 Pattern 168hrs	**168 hrs**	N.P.	
7	**LTDR** Low Temp. Data Retention	[AEC Q100-005] ☒ Vth Drift Analysis After 1k W/E cyc @25°C Ta= 60ºC, All0 Pattern 1000hrs	**1000 hrs**	N.P.	

8	**LTDR** Low Temp. Data Retention	[AEC Q100-005] ☒ Vth Drift Analysis After 10k W/E cyc @25°C Ta= 60ºC, All0 Pattern 1000hrs	**1000 hrs**	N.P.	
9	**LTDR** Low Temp. Data Retention	[AEC Q100-005] ☒ Vth Drift Analysis After 100k W/E cyc @25°C Ta= 60ºC, All0 Pattern 1000hrs	**1000 hrs**	N.P.	
10	**Flip Bit**	[AEC Q100-005] ☒ Vth Drift Analysis After 1 W/E cyc @25°C Ta= 25ºC, Chk Pattern 1000hrs	**1000 hrs**	N.P.	
11	**Read Disturb**	After 10 W/E cyc @125°C Ta= 125ºC; 4,5V Stress <1ppm after 6000hrs with ECC	**Final**	N.P.	
12	**Read Disturb**	After 10k W/E cyc @125°C Ta= 125ºC; 4,5V Stress <1ppm after 1 sec with ECC	**Final**	N.P.	

2.5 Package Assembly Integrity Test (Q100 Group C)

Test			Step	Results	
N	**TEST NAME**	**CONDITIONS [SPEC]**		**eTQFP64**	
C1	**WBS** Wire Bond Shear	[AEC Q100-001] At appropriate time interval for each bonder to be used 30 bonds x 5 devices	**Final result**	Passed	Assy Report
C2	**WBP** Wire Bond Pull	[MIL-STD883 method 2011] 30 bonds x 5 devices	**Final result**	Passed	Assy Report
C3	**SD** Solderability	[JEDEC J-STD-002D] > 95% lead coverage	**Final result**	Passed	Assy Report
C4	**PD** Physical Dimension	[JEDEC JEDES22-B100 and B108]	**Final result**	Passed	Assy Report
C5	**SBS** Solder Ball Shear	[AEC Q100-010]	**Final result**	N.A.	
C6	**LI** Lead Integrity	[JEDEC JEDES22-B105]	**Final result**	N.A.	

2.6 Die Fabrication Reliability Test (Q100 Group D)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS			
D1	**EM** Electromigration	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
D2	**TDDB** Time Dependent Dielectric Breakdown	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
D3	**HCI** Hot Carrier Injection	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
D4	**NBTI** Negative Bias Temperature Instability	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification
D5	**SM** Stress Migration	The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies	**Final result**	DONE	Process qualification

2.7 Electrical Verification Test (Q100 Group E)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS [AEC Q100]			
E2	**ESD HBM**	HBM = 2kV	**Final result**	N.P.	
E3	**ESD CDM**	CDM = 500V / 750V corner only	**Final result**	PASSED 0/3 per V level	
E4	**LU**	Current Injection Power supply sequence Overvoltage on power supply @Room & Hot	**Final result**	N.P.	
E5	**ED** Electrical Distribution	[AEC Q100-009] ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold	**Final result**	DONE	
E6	**FG** Fault Grading	[AEC Q100-007] FG shall be = or > 90% for qual units	**Final result**	DONE	

E7	**CHAR** Characterization	[AEC Q103] Performed on new technologies and part families. ☒ Testing at Room ☒ Testing at Hot ☒ Testing at Cold	**Final result**	N.P.	
E9	**EMC** Electromagnetic Compatibility	[SAE J1752/3 – radiated Emission]	**Final result**	N.P.	
E10	**SC** Short Circuit Characterization	[AEC Q100-012] Applicable to all smart power devices. This test and statistical evaluation shall be performed per agreement between user and supplier on a case-by-case basis.	**Final result**	N.A.	
E11	**SER** Soft Error Rate	[JEDEC Un-accelerated: JESD89-1 or Accelerated: JESD89-2 & JESD89-3] Applicable to devices with memory sizes 1Mbit SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications. This test and its accept criteria is performed	**Final result**	DONE	Process qualification
E12	**LF** Lead (Pb) Free [AEC Q005]	/	/	YES	

2.8 Defect Screening Test (Q100 Group F)

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS			
F1	**PAT** Process Average testing	[AEC Q101]	**Final result**	IMPLEMENTED	
F2	**SBA** Statistical Bin/Yield Analysis	[AEC Q102]	**Final result**	IMPLEMENTED	

3 REVISION TRACKING

Rev 1.0

1. First Release

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PCN Reference : ADG/21/12751

Subject : Public Products List

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