


PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data

| | | |
|----------------------|---|--------------------------------------|
| 1.1 Company |  | STMicroelectronics International N.V |
| 1.2 PCN No. | ADG/21/12576 | |
| 1.3 Title of PCN | SPC584BxxE1xx (FC70): Activation of Muar as Assembly and Final Testing Location | |
| 1.4 Product Category | see list | |
| 1.5 Issue date | 2021-02-02 | |

2. PCN Team

| | |
|----------------------------------|--------------------------|
| 2.1 Contact supplier | |
| 2.1.1 Name | ROBERTSON HEATHER |
| 2.1.2 Phone | +1 8475853058 |
| 2.1.3 Email | heather.robertson@st.com |
| 2.2 Change responsibility | |
| 2.2.1 Product Manager | Luca RODESCHINI |
| 2.1.2 Marketing Manager | Matteo MOIOLI |
| 2.1.3 Quality Manager | Alberto MERVIC |

3. Change

| | | |
|--------------|---|----------------------------|
| 3.1 Category | 3.2 Type of change | 3.3 Manufacturing Location |
| Transfer | Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Assembly site (SOP 2617) | ST Muar - Malaysia |

4. Description of change

| | | |
|---|--|---|
| | Old | New |
| 4.1 Description | ST Kirkop-Malta as Assembly and Final Testing Location | ST Kirkop-Malta and ST Muar as Assembly and Final Testing Locations |
| 4.2 Anticipated Impact on form,fit, function, quality, reliability or processability? | No Impact | |

5. Reason / motivation for change

| | |
|----------------------|-------------------|
| 5.1 Motivation | Capacity Increase |
| 5.2 Customer Benefit | CAPACITY INCREASE |

6. Marking of parts / traceability of change

| | |
|-----------------|-------------------------------|
| 6.1 Description | Dedicated Finished Good Codes |
|-----------------|-------------------------------|

7. Timing / schedule

| | |
|-------------------------------------|--------------|
| 7.1 Date of qualification results | 2021-03-31 |
| 7.2 Intended start of delivery | 2021-04-30 |
| 7.3 Qualification sample available? | Upon Request |

8. Qualification / Validation

| | | | |
|--|-------------|------------|--|
| 8.1 Description | | | |
| 8.2 Qualification report and qualification results | In progress | Issue Date | |

9. Attachments (additional documentations)

| |
|--------------------------|
| 12576 Public product.pdf |
| 12576 Details.pdf |

| 10. Affected parts | | |
|-------------------------|-------------------------|--------------------------|
| 10. 1 Current | | 10.2 New (if applicable) |
| 10.1.1 Customer Part No | 10.1.2 Supplier Part No | 10.1.2 Supplier Part No |
| | SPC584B70E1NHC0X | |

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Public Products List

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PCN Title : SPC584BxxE1xx (FC70): Activation of Muar as Assembly and Final Testing Location

PCN Reference : ADG/21/12576

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

| | | |
|------------------|------------------|------------------|
| SPC584B60E1EG00X | SPC584B70E1NHC0X | SPC584B70E1EDC0X |
| SPC584B64E1NH00X | | |



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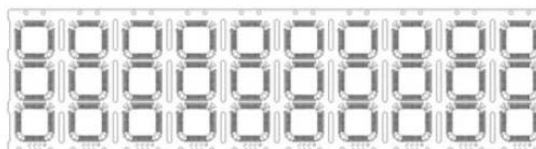
PRODUCT/PROCESS CHANGE NOTIFICATION

| | |
|---------------------------|--|
| TITLE | SPC584BxxE1xx (FC70): Activation of Muar as Assembly and Final Testing Location |
| IMPACTED PRODUCTS | <p>ST silicon line FC70 assembled in TQFP 64 10x10x1.0 Exposed Pad Package:</p> <ul style="list-style-type: none"> • SPC584B60E1EG00X • SPC584B64E1DD00X • SPC584B64E1NH00X • SPC584B70E1ED01X • SPC584B70E1EDC0X • SPC584B70E1EH00X • SPC584B70E1NHC0X |
| MANUFACTURING STEP | Assembly and Electrical Final Test |
| INVOLVED PLANT | ST Muar (Malaysia) |
| CHANGE REASON | Capacity Increase |
| CHANGE DESCRIPTION | <p>ST Muar will be activated for Assembly and electrical Final Test</p> <p>Assembly transfer includes specific product's improvements linked to new solutions and processes availability, such as:</p> <ul style="list-style-type: none"> • Package Bill of Material: move to High Density (HD) leadframe (different supplier) move to 0.7mil wires diameter • Molding Process: move to central top gate resin injection move to new molding compound (Sumitomo EME-G700SLS) • Marking: re-layout and addition of 2D identifier. <p>Final Test transfer does not concern changes in test flow or equipment</p> |

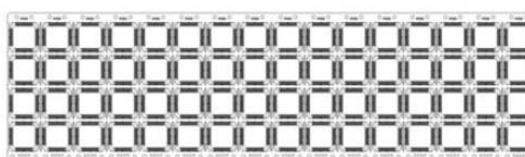
As far as assembly is concerned, additional details are here below provided.

High Density (HD) Leadframe: increased number of units per strip, from 30 to 64 units/strip.

Standard Frame 3x10
(30 units/strip)



High Density 4x16
(64 units/strip)



Unit level drawing (pad size, etc.) remains unchanged.

Central Top Gate Mold Injection: reduces stress and possible wire sweeping during molding process

2D Marking: improves product's internal traceability.

Both changes are visible on package as shown:

Malta



Muar



Muar: Central Top Gate is visible at package's center
2D Marking positioned at right top corner

TRACEABILITY

New Finished Good (internal part number) code and Date Code

| | | | | |
|----------------|---|--|----|---|
| VALIDATION | Validation report included in this communication based on ZVEI (AEC-Q100/Q006) recommendations reported in the following table: | | | |
| | SEM-PA-08 | Change of wire bonding | P | P |
| | SEM-PA-11 | Change of mold compound / encapsulation material | P | P |
| | SEM-PA-13 | Change of product marking | I | P |
| | SEM-PA-16 | Change of direct material supplier | -- | P |
| | SEM-PA-18 | Move all or parts of production to a different assembly site. | P | P |
| | SEM-PA-21 | Molding / Encapsulation process | -- | P |
| | PACKING/SHIPPING | | | |
| | EQUIPMENT | | | |
| | TEST FLOW | | | |
| | SEM-TF-01 | Move of all or part of electrical wafer test and/or final test to a different test site. | P | P |
| | With reference to the above qualification plan, following trials are not performed: | | | |
| | <ul style="list-style-type: none">• ELFR: silicon related, not applicable to assembly changes;• EM: silicon related, not applicable to assembly changes;• LI: not applicable to surface mount packages;• SC: not applicable to microcontrollers;• PTC: not applicable | | | |
| IMPLEMENTATION | Change will be implemented upon customer approval | | | |
| REPORT | Validation report will be provided within March 2021 Here enclosed the qualification Plan | | | |



Preliminary Reliability Report

Chorus2M eTQFP64 Muar Assy

M40

FAB transfer

| General Information | |
|----------------------------|----------|
| Product Line | FC70 |
| Product Description | Chorus2M |
| Product Group | ADG |
| Product division | ADS |
| Silicon process technology | CMOS M40 |

| Locations | |
|------------------------|---|
| Wafer fab location | Crolles 2 |
| Final Assessment | |
| Reliability assessment | Reliability trials on Chorus2M eTQFP64 assembled in Muar completed up to Q100 milestone with positive results. Extension required by Q006 ongoing |

DOCUMENT HISTORY

| Version | Date | Author | Comment |
|---------|------------|------------|------------------------------------|
| 1.0 | 19/01/2021 | P.Epigrati | First release. Preliminary results |

RELEASED DOCUMENT



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1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this document is to report the preliminary reliability trials results for Chorus2M Cut1.2 eTQFP64 assy transfer from Malta to Muar.
Chorus2M eTQFP64 product diffused in Crolles and assembled in Malta is in mass production since 2018.

Purpose of the change is to transfer Back End site from ST Malta to ST Muar plant. Assembly transfer includes specific product improvements linked to new solutions and processes availability, such as:

- Package Bill of Material:
 - o change from standard matrix to High Density (HD) matrix leadframe (different supplier) with increased number of units per strip. Unit level drawing (pad size, etc.) remains unchanged
 - o change wire diameter from 0.8mils to 0.7mils
 - o change of molding compound
- Molding Process: change to central top gate resin injection with the purpose to reduce stress and wire sweeping during molding process.

Qualification of Chorus2M eTQFP64 assembled in Muar takes similarities with Chorus4M eTQFP64 assembled in Muar.
BOM comparison between Malta and Muar assy is reported in table at paragraph 1.4.

Assy reports are available for all qualification lots.

The qualification exercise for this change is in line with ZVEI Delta Qualification Matrix (ESD CDM performed in addition to ZVEI Requirements according to internal common practice) and it is in respect of AEC-Q100 rev.H and AEC-Q006 rev.A for copper wire qualification.

1.2 Conclusions

Preliminary results of reliability trials are presented.
AEC-Q100 rev. H milestone has been positively achieved on Chorus2M eTQFP64 assembled in Muar.
Reliability trials are still ongoing to reach AEC-Q006 rev.A milestone.

1.3 Wafer fab information

| DIE FEATURES | |
|-------------------------|----------------|
| Product Code | FC70 |
| Diffusion Site | Crolles 2 |
| Wafer Diameter (inches) | 12 |
| Process Technology | CMOS M40 |
| Passivation | PSG + Nitride |
| Die finishing back side | Lapped Silicon |

1.4 Package outline/Mechanical data

| | Chorus2M eTQFP64 Malta Assy | Chorus2M eTQFP64 Muar Assy | Chorus4M eTQFP64 Muar Assy |
|--------------------------------------|-----------------------------------|------------------------------------|------------------------------------|
| Package Description | TQFP-EP 64 10X10X1.0 ExpadDown | TQFP-EP 64L 10X10X1.0 ExpadDown | TQFP-EP 64L 10X10X1.0 ExpadDown |
| Assembly Site | ST KIRKOP – MALTA | ST MUAR | ST MUAR |
| Die Attach material | QMI9507 | QMI9507 | QMI9507 |
| Molding compound | G700LS | G700SLS | G700SLS |
| Substrate/Leadframe | Standard Pre-plated | HD Pre-plated | HD Pre-plated |
| Wires bonding materials/diameters | Cu 0.8mil | Cu 0.7mil | Cu 0.7mil |

1.5 Final testing information:

| PACKAGE FEATURES | |
|--|----------------------|
| Electrical Testing manufacturing location | : ST MUAR / ST MALTA |
| Tester | : Teradyne J750 |



2 RELIABILITY PLAN AND TESTS RESULTS

2.1 Conditions

Room test temperature is 25°C

Hot test temperature is 150°C

Cold test temperature is -40°C

2.2 Tables entry legend

| Symbol | How to read |
|-------------------------------------|---|
| <input type="checkbox"/> | Action or condition has not to be considered |
| <input checked="" type="checkbox"/> | The action/condition has been done/applied during the trial |
| N.P. | The trial or readout is not in the Qualification Plan and thus has not been performed |
| N.A. | Not applicable |
| N.C. | Trial not completed yet |

2.3 Accelerated Environmental Stress Test (Q100 Group A)

| Test | | | Step | Results eTQFP64 | Notes |
|------|---------------------------------------|---|-----------------|--|--|
| N | TEST NAME | CONDITIONS [SPEC] | | | |
| A1 | Pre Conditioning MSL 3 | [J-STD-020] <input checked="" type="checkbox"/> Testing at Room <input checked="" type="checkbox"/> Testing at Hot <input checked="" type="checkbox"/> Testing at Cold <input checked="" type="checkbox"/> Sonoscan pre / post <input checked="" type="checkbox"/> WPT pre / post <input checked="" type="checkbox"/> WBS pre / post <input checked="" type="checkbox"/> Die visual inspection post trial <input checked="" type="checkbox"/> 100 Temperature Cycles 24h bake@125°C, 192h@30°C/60%RH 3x Reflow simulation 260°C Peak Temp | Pre/Post | 0/77 x 1 0/231 x 3 Chorus4M eTQFP64 | Similarities with Chorus4M eTQFP64 assembled in Muar |

| | | | | | |
|------|---|--|----------|---|--|
| A2 | THB Temperature Humidity Bias | [JESD22-A101/A110] <input checked="" type="checkbox"/> After Jedec PC MSL3 <input checked="" type="checkbox"/> Testing at Room <input checked="" type="checkbox"/> Testing at Hot <input type="checkbox"/> Testing at Cold <input checked="" type="checkbox"/> Sonoscan pre / post <input checked="" type="checkbox"/> WPT pre / post <input checked="" type="checkbox"/> WBS pre / post <input checked="" type="checkbox"/> Visual Inspection <input checked="" type="checkbox"/> Cross section Ta=85°C, 85%RH, 1000hrs 2000hrs AEC-Q006 | 1000 hrs | N.P. 0/77 x 3 Chorus4M eTQFP64 | Similarities with Chorus4M eTQFP64 assembled in Muar |
| | | | 2000hrs | N.P. N.C. 77 x 3 Chorus4M eTQFP64 | |
| A3.a | THS Temperature Humidity Storage | [JESD22-A101/A110] <input checked="" type="checkbox"/> After Jedec PC MSL3 <input checked="" type="checkbox"/> Testing at Room <input type="checkbox"/> Testing at Hot <input type="checkbox"/> Testing at Cold <input checked="" type="checkbox"/> Sonoscan pre / post <input checked="" type="checkbox"/> WPT pre / post <input checked="" type="checkbox"/> WBS pre / post <input checked="" type="checkbox"/> Visual Inspection <input checked="" type="checkbox"/> Cross section Ta=85°C, 85%RH, 1000hrs | 2000 hrs | N.P. | |
| A3.b | AC Autoclave | [JESD22-A102/A118] <input checked="" type="checkbox"/> After Jedec PC MSL3 <input checked="" type="checkbox"/> Testing at Room <input type="checkbox"/> Testing at Hot <input type="checkbox"/> Testing at Cold <input checked="" type="checkbox"/> Sonoscan pre / post <input checked="" type="checkbox"/> WPT pre / post <input checked="" type="checkbox"/> WBS pre / post <input checked="" type="checkbox"/> Visual Inspection <input checked="" type="checkbox"/> Cross section P=2.08atm Ta=121°C, 96hrs | 96 hrs | N.P. 0/77 x 3 Chorus4M eTQFP64 | Similarities with Chorus4M eTQFP64 assembled in Muar |

| | | | | | |
|----|---|---|-----------------|--|--|
| A4 | TC Temperature Cycling | <p>[JESD22-A104]</p> <p> <input checked="" type="checkbox"/> After Jedec PC MSL3 <input checked="" type="checkbox"/> Testing at Room <input checked="" type="checkbox"/> Testing at Hot <input checked="" type="checkbox"/> Testing at Cold <input checked="" type="checkbox"/> Sonoscan pre / post <input checked="" type="checkbox"/> WPT pre / post <input checked="" type="checkbox"/> WBS pre / post <input checked="" type="checkbox"/> Visual Inspection <input checked="" type="checkbox"/> Cross section </p> <p> Ta=-55°C /+150 °C, 1000cyc 2000cyc AEC-Q006 </p> | 1000cyc | <p>0/77 x 1 Chorus2M eTQFP64</p> <p>0/77 x 3 Chorus4M eTQFP64</p> | Similarities with Chorus4M eTQFP64 assembled in Muar |
| | | | 2000cyc | <p>N.C. Chorus2M eTQFP64</p> <p>N.C. 77 x 3 Chorus4M eTQFP64</p> | |
| A5 | PTC Power Temperature Cycle | <p>[JESD22-A105]</p> <p> <input checked="" type="checkbox"/> After Jedec PC MSL3 <input checked="" type="checkbox"/> Testing at Room <input checked="" type="checkbox"/> Testing at Hot <input checked="" type="checkbox"/> Testing at Cold </p> <p> Ta=-40°C /+125 °C 1000 cyc 2000cyc AEC-Q006 </p> | 1000 cyc | <p>N.P.</p> <p>0/45 x 1 Chorus4M eTQFP64</p> | Similarities with Chorus4M eTQFP64 assembled in Muar |
| | | | 2000cyc | <p>N.P.</p> <p>N.C. Chorus4M eTQFP64</p> | |

| | | | | | |
|----|---|--|---------|---|--|
| A6 | HTSL High Temperature Storage Lifetime | <p>[JESD22-A103]</p> <p> <input type="checkbox"/> After Jedec PC MSL3 <input checked="" type="checkbox"/> Testing at Room <input checked="" type="checkbox"/> Testing at Hot <input type="checkbox"/> Testing at Cold <input type="checkbox"/> Sonoscan pre / post <input checked="" type="checkbox"/> WPT pre / post <input checked="" type="checkbox"/> WBS pre / post <input checked="" type="checkbox"/> Visual Inspection <input checked="" type="checkbox"/> Cross section </p> <p>Ta= 150°C, 1000hrs 2000hrs AEC-Q006</p> | 1000hrs | <p>N.P.</p> <p>0/77x 3 Chorus4M eTQFP64</p> | Similarities with Chorus4M eTQFP64 assembled in Muar |
| | | | 2000hrs | <p>N.P.</p> <p>N.C. Chorus4M eTQFP64</p> | |

2.4 Accelerated Lifetime Simulation Test (Q100 Group B)

| Test | | | Step | Results | Notes |
|------|---|---|---------|--|--|
| N | TEST NAME | CONDITIONS [SPEC] | | Lot 1 | |
| B1.a | HTOL High Temp. Operating Life | <p>[JESD22-A108]</p> <p> <input type="checkbox"/> After Jedec PC MSL3 <input checked="" type="checkbox"/> After 1k W/E cyc @125°C <input checked="" type="checkbox"/> Testing at Room, Hot, Cold <input checked="" type="checkbox"/> Drift Analysis on Key parameters </p> <p>Ta=125°C, VDD_HV=5.5V, VDD_LV=1.44V 168hrs (1000hrs monitor)</p> | 168 hrs | <p>N.P.</p> <p>0/77 x 1 Chorus4M eTQFP64 assembled in Muar</p> | Similarities with Chorus4M eTQFP64 assembled in Muar |



RELIABILITY REPORT

ADG – Q&R Digital
Products

RR000021_01

Chorus2M eTQFP64 Muar–M40

| | | | | | |
|-------|---|--|------------------|------|---|
| B1.b | LTOL High Temp. Operating Life | [JESD22-A108] <input type="checkbox"/> After Jedec PC MSL3 <input checked="" type="checkbox"/> After 1k W/E cyc @ 125°C <input checked="" type="checkbox"/> Testing at Room, Hot, Cold <input checked="" type="checkbox"/> Drift Analysis on Key parameters Ta=-40°C, VDD_LV=1.44V 1000hrs | 1000hrs | N.P. | |
| B2 | ELFR Early Life Failure Rate | [AEC Q100-008] <input checked="" type="checkbox"/> Testing at Room, Hot Ta= 125°C, Tj=150°C BI+24 hrs | BI +24hrs | N.P. | Silicon stress trial, not significant for assembly changes. Line Stress performed instead |
| B3.1 | HTDR High Temp. Data Retention | [AEC Q100-005] <input checked="" type="checkbox"/> After Jedec PC MSL3 <input checked="" type="checkbox"/> Testing at Room <input type="checkbox"/> Testing at Hot <input type="checkbox"/> Testing at Cold <input checked="" type="checkbox"/> After 1k W/E cyc @ 125°C <input checked="" type="checkbox"/> Vth Drift Analysis All0, Ta=150°C, 1000hrs (2000hrs <i>monitoring</i>) | 2000 hrs | N.P. | |
| B3.2a | FET @25°C | [AEC Q100-005] <input checked="" type="checkbox"/> Testing at Room <input checked="" type="checkbox"/> Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 25°C 100k Write/Erase cyc | 100k cyc | N.P. | |
| B3.2b | HTDR After FET | <input checked="" type="checkbox"/> Vth Drift Analysis Ta= 150°C, All0 Pattern 168hrs | 168 hrs | N.P. | |
| B3.3a | FET @125°C | [AEC Q100-005] <input checked="" type="checkbox"/> Testing at Room <input checked="" type="checkbox"/> Drift Analysis on Flash key parameters at Room, Hot, Cold Ta= 125°C 100k Write/Erase cyc | 100k cyc | N.P. | |
| B3.3b | HTDR After FET | <input checked="" type="checkbox"/> Vth Drift Analysis Ta= 150°C, All0 Pattern 168hrs | 168 hrs | N.P. | |



RELIABILITY REPORT

ADG – Q&R Digital
Products

RR000021_01

Chorus2M eTQFP64 Muar–M40

| | | | | | |
|-------|----------------|--|----------|------|--|
| B3.4a | FET @-40°C | <p>[AEC Q100-005]</p> <p><input checked="" type="checkbox"/> Testing at Room</p> <p><input checked="" type="checkbox"/> Drift Analysis on Flash key parameters at Room, Hot, Cold</p> <p>Ta= -40°C</p> <p>100k Write/Erase cyc</p> | 100k cyc | N.P. | |
| B3.4b | HTDR After FET | <p><input checked="" type="checkbox"/> Vth Drift Analysis</p> <p>Ta= 150°C, All0 Pattern</p> <p>168hrs</p> | 168 hrs | N.P. | |
| B3.5 | Read Disturb | <p>After 10 W/E cyc @125°C</p> <p>Ta= 125°C; 4,5V Stress</p> <p><1ppm after 6000hrs with ECC</p> | Final | N.P. | |
| B3.6 | Read Disturb | <p>After 10k W/E cyc @125°C</p> <p>Ta= 125°C; 4,5V Stress</p> <p><1ppm after 1 sec with ECC</p> | Final | N.P. | |

2.5 Package Assembly Integrity Test (Q100 Group C)

| Test | | | Step | Results | |
|------|---------------------------------|---|---------------------|---------|-------------|
| N | TEST NAME | CONDITIONS [SPEC] | | eTQFP64 | |
| C1 | WBS Wire Bond Shear | [AEC Q100-001] At appropriate time interval for each bonder to be used 30 bonds x 5 devices | Final result | Passed | Assy Report |
| C2 | WBP Wire Bond Pull | [MIL-STD883 method 2011] 30 bonds x 5 devices | Final result | Passed | Assy Report |
| C3 | SD Solderability | [JEDEC JEDES22-B102] > 95% lead coverage | Final result | Passed | Assy Report |
| C4 | PD Physical Dimension | [JEDEC JEDES22-B100 and B108] | Final result | Passed | Assy Report |
| C5 | SBS Solder Ball Shear | [AEC Q100-010] | Final result | N.A. | |
| C6 | LI Lead Integrity | [JEDEC JEDES22-B105] | Final result | N.A. | |

2.6 Die Fabrication Reliability Test (Q100 Group D)

| Test | | | Step | RESULTS | Notes |
|------|--|--|---------------------|---------|-----------------------|
| N | TEST NAME | CONDITIONS | | | |
| D1 | EM Electromigration | The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies | Final result | DONE | Process qualification |
| D2 | Tddb Time Dependent Dielectric Breakdown | The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies | Final result | DONE | Process qualification |
| D3 | HCI Hot Carrier Injection | The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies | Final result | DONE | Process qualification |
| D4 | NBTI Negative Bias Temperature Instability | The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies | Final result | DONE | Process qualification |
| D5 | SM Stress Migration | The data, test method, calculation and internal criteria should be available to the customer upon request for new technologies | Final result | DONE | Process qualification |



2.7 Electrical Verification Test (Q100 Group E)

| Test | | | Step | RESULTS | Notes |
|------|--|---|---------------------|---------------------------|-----------------------|
| N | TEST NAME | CONDITIONS [AEC Q100] | | | |
| E2 | ESD HBM | HBM = 2kV | Final result | N.P. | |
| E3 | ESD CDM | CDM = 500V / 750V corner only | Final result | PASSED 0/3 per V level | |
| E4 | LU | Current Injection Power supply sequence Overvoltage on power supply @Room & Hot | Final result | N.P. | |
| E5 | ED Electrical Distribution | [AEC Q100-009] <input checked="" type="checkbox"/> Testing at Room <input checked="" type="checkbox"/> Testing at Hot <input checked="" type="checkbox"/> Testing at Cold | Final result | DONE | |
| E6 | FG Fault Grading | [AEC Q100-007] FG shall be = or > 90% for qual units | Final result | DONE | |
| E7 | CHAR Characterization | [AEC Q103] Performed on new technologies and part families. <input checked="" type="checkbox"/> Testing at Room <input checked="" type="checkbox"/> Testing at Hot <input checked="" type="checkbox"/> Testing at Cold | Final result | N.P. | |
| E9 | EMC Electromagnetic Compatibility | [SAE J1752/3 – radiated Emission] | Final result | N.P. | |
| E10 | SC Short Circuit Characterization | [AEC Q100-012] Applicable to all smart power devices. This test and statistical evaluation shall be performed per agreement between user and supplier on a case-by-case basis. | Final result | N.A. | |
| E11 | SER Soft Error Rate | [JEDEC Un-accelerated: JESD89-1 or Accelerated: JESD89-2 & JESD89-3] Applicable to devices with memory sizes 1Mbit SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications. This test and its accept criteria is performed | Final result | DONE | Process qualification |
| E12 | LF Lead (Pb) Free [AEC Q005] | / | / | YES | |



2.8 Defect Screening Test (Q100 Group F)

| Test | | | Step | RESULTS | Notes |
|------|--|------------|-------------------------|-------------|-------|
| N | TEST NAME | CONDITIONS | | | |
| F1 | PAT Process Average testing | [AEC Q101] | Final result | IMPLEMENTED | |
| F2 | SBA Statistical Bin/Yield Analysis | [AEC Q102] | Final result | IMPLEMENTED | |



3 REVISION TRACKING

Rev 1.0

1. First Release