PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/23/14294
1.3 Title of PCN	VN9D30Q100FTR (XV99): Product Optimization (EC silicon revision)
1.4 Product Category	VN9D30Q100FTR
1.5 Issue date	2023-09-15

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Mario ASTUTI,Carmelo PISTRITTO
2.1.2 Marketing Manager	Rosario RUGGERI
2.1.3 Quality Manager	Daniela FAZIO

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Die redesign : Mask or mask set change with new die design like metallization (specifically chip frontside) or bug fix	ST CT8 Catania (Italy) 8” Wafer Fab

4. Description of change		
	Old	New
4.1 Description	Silicon rev. EA	Silicon rev. EC
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No impact	

5. Reason / motivation for change	
5.1 Motivation	Product Optimization
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Dedicated Finished Good Code

7. Timing / schedule	
7.1 Date of qualification results	2023-09-07
7.2 Intended start of delivery	2023-12-21
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	14294 RRLGS20030_VN9D30Q100F_XV99_QFN6x6_CLB_M0A9_5.0.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2023-09-15

9. Attachments (additional documentations)
14294 Public product.pdf 14294 details.pdf 14294 RRLGS20030_VN9D30Q100F_XV99_QFN6x6_CLB_M0A9_5.0.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	VN9D30Q100FTR	

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Product/process change notification: VN9D30Q100FTR (XV99): Product Optimization (EC silicon revision)

ADG/23/14294

Product family	Technology	Package
VN9D30Q100FTR		VFQFPN 6X6X1

(optional)

Description of the change
Due to product optimization new silicon revision (revision EC) has been qualified

Reason
Product optimization

Date of implementation
From December 2023

Impact of the change	
Form	No Impact
Fit	No Impact
Function	No Impact
Reliability	No Impact
Processibility	No Impact

Qualification of the change

Qualification report included in this communication.

14294 RRLGS20030_VN9D30Q100F_XV99_QFN6x6_CLB_M0A9_5.0.pdf

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : VN9D30Q100FTR (XV99): Product Optimization (EC silicon revision)

PCN Reference : ADG/23/14294

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

VN9D30Q100FTR		

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Reliability Evaluation Report
VN9D30Q100F (XV99)_QFN6x6
New Product Qualification

General Information	
Commercial Product:	VN9D30Q100F
Product Line:	XV99
Package:	QFN6x6
Silicon Technology:	VIPower® M0A9

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile for Automotive Application. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Revision history

Rev.	Changes description	Author	Date
1.0	- Preliminary with full results except for Power Temperature Cycling	F. Ceraulo	Dec 18, 2020
2.0	- With Power Temperature Cycling result	F. Ceraulo	Mar 11, 2021
3.0	- Physical Analysis on stresses parts after 1x AEC-Q100	F. Ceraulo	Jul 21, 2021
4.0	- To specify cumulative fails on summary short circuit table	F. Ceraulo	Aug 8, 2021
5.0	- To align ESD values	F. Ceraulo	Aug 30, 2023

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Catania (Italy)	A. Marmoni	Aug 8, 2021

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1. Reliability Evaluation Overview

1.1. Objective

Aim of this report is to present the results of the reliability evaluations performed on **VN9D30Q100F** (XV99 as ST internal silicon line) to release the product in production.

The device is 6-channel high-side driver for Automotive application, manufactured with proprietary ST VIPower M0A9 Technology in ST CT8 Catania (Italy) 8" Wafer Fab and assembled in QFN6x6 package by ST Calamba (Philippines).

1.2. Reliability Strategy and Test Plan

1.2.1. Reliability strategy

Reliability trials performed as part of this reliability evaluation are in agreement with ST 0061692 and **AEC Q100 rev. H Grade 1** specification and are listed in below *Test Plan*. For details on test conditions, generic data used and specifications references refer to test results summary in section 3.

The VIPower M0A9 silicon Technology was fully AEC-Q100 qualified and released at mass production by means product **VN9D30Q100J** assembled in package PSSO16 (ST reference report #RRABDCT1910).

The VIPower M0A10 silicon Technology was fully AEC-Q100 qualified and released at mass production by means product **VN9D5D20FN** assembled in package QFN6x6 (ST reference report #RRLGS20025).

The **VN9D30Q100F** was classified Derivative of the above-mentioned test vehicle due to:

- from a silicon Technology standpoint **VN9D30Q100J** and **VN9D30Q100F** are exactly the same die;
- from a Package standpoint **VN9D5D20FN** is the max die size in package QFN6x6, gap between M0A9 and M0A10 Technologies is related only to a different EPY substrate.

Consequently, the qualification plan of **VN9D30Q100F** was based on 1 lot full AEC-Q100 using family data by the previous mentioned qualification activities.

1.2.2 Test Plan

AEC-Q100 TEST PLAN

TEST GROUP	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
A Accelerated Environment Stress Tests	PC (JL3)	Preconditioning (JL3+3 reflows simulation)	Yes
	THB	Temperature Humidity Bias	Yes
	AC	Autoclave at 2atm	Yes
	TC	Temperature Cycling	Yes
	PTC	Power Temperature Cycling	Yes
	HTSL	High Temperature Storage Life	Yes
B Accelerated Lifetime Simulation Tests	HTOL	High Temperature Operating Life	Yes
	ELFR	Early Life Failure Rate	Yes
	EDR	Endurance Data Retention	Not Applicable
C Package Assembly Integrity Tests	WBS	Wire Bond Shear	Yes
	WBP	Wire Bond Pull	Yes
	SD	Solderability	Yes
	PD	Physical Dimension	Yes
	SBS	Solder Ball Shear	Not Applicable
	LI	Lead Integrity	Not Applicable
D Die Fabrication Reliability Tests	Test list is reported in section 5	Performed during process qualification	Similarity (generic data)
E Electrical Verification Tests	ESD (HBM)	Electrostatic Discharge (Human Body Model)	Yes
	ESD (CDM)	Electrostatic Discharge (Charged Device Model)	Yes
	LU	Latch Up	Yes
	ED	Electrical distribution	Yes
	FG	Fault grading	Not Applicable
	CHAR	Characterization	Yes
	EMC	Electromagnetic Compatibility	Yes
	SC	Short Circuit Characterization	Yes
	SER	Soft Error Rate	Not Applicable
	LF	Lead(Pb) Free: (see AEC-Q005)	Yes
F Defect Screening Tests		To be implemented starting from first production lot	No
G Cavity Package Integrity Tests		N/A: not for plastic packaged devices	Not Applicable

1.3. Conclusion

All reliability tests have been completed with positive results, neither functional nor parametric rejects were detected at final electrical testing, parameter drift analysis showed a good stability for all the tested parameters.

Based on the overall results obtained, VN9D30Q100F (XV99) product diffused in ST CT8 Catania (Italy) 8" Wafer Fab and assembled by ST Calamba (Shenzhen) has positively passed reliability evaluation performed in agreement to AEC_Q100 Rev. H specification Grade 1.

2. Product Characteristics

2.1. Generalities

life.augmented

VN9D30Q100F

Datasheet

6-channel high-side driver with 24-bit SPI interface for automotive applications

QFN 6x6

Product status link
VN9D30Q100F

Product summary	
Order code	VN9D30Q100FTR
Package	QFN 6X6
Packing	Tape and reel

Features

Channel	V_{CC}	R_{ON} typ.	I_{LIMH} typ.
0, 5	28 V	33 mΩ	31.5 A
1, 2, 3, 4	28 V	90 mΩ	14 A

- AEC-Q100 qualified
- General
  - Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
  - 24-bit ST-SPI for full diagnostic and digital current sense feedback
  - Integrated 10-bit ADC for digital current sense
  - Integrated PWM engine with independent phase shift and frequency generation (for each channel)
  - Programmable Bulb/LED mode for all channels
  - Advanced limp-home functions for robust fail-safe system
  - Very low standby current
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - Control through direct inputs and/or SPI
  - Compliant with European directive 2002/95/EC
- Diagnostic functions
  - Digital proportional load current sense
  - Synchronous diagnostic of over load and short to GND, output shorted to V_{CC} and OFF-state open-load
  - Programmable case overtemperature warning
- Protection
  - Two levels load current limitation
  - Self limiting of fast thermal transients
  - Undervoltage shutdown
  - Overvoltage clamp
  - Latch-off or programmable time limited auto restart (power limitation and overtemperature shutdown)
  - Load dump protected
  - Protection against loss of ground

Description

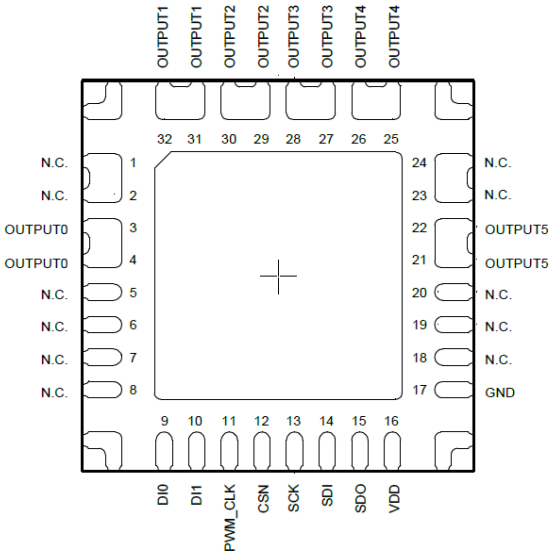
The VN9D30Q100F is a device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads directly connected to ground. The device is protected against voltage transient on V_{CC} pin.

Programming, control and diagnostics are implemented via the SPI bus.

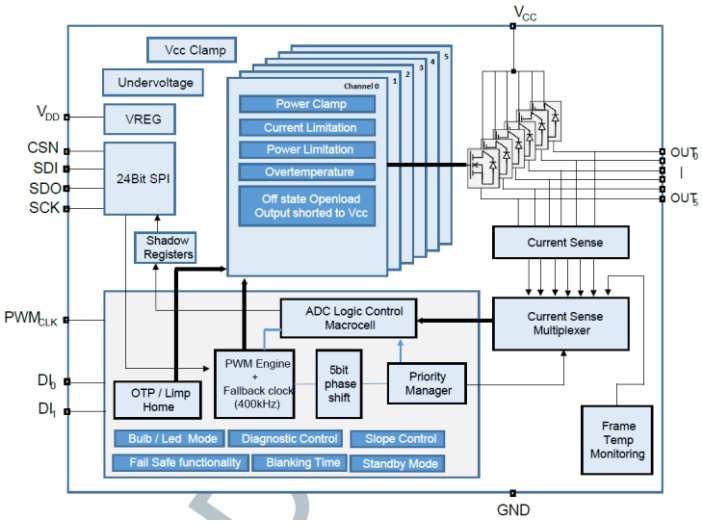
A digital current sense feedback for each channel is provided through an integrated 10-bit ADC with 0.1% of FSR. Dedicated trimming bits allow to adjust the ADC reference current.

DS13246 - Rev 6 - August 2023
For further information contact your local STMicroelectronics sales office.
www.st.com

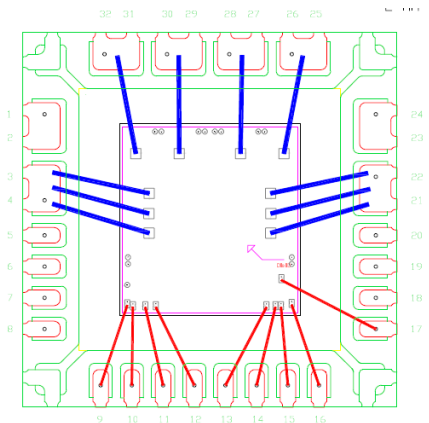
2.2. Pin connection



2.3. Block diagram



2.4. Bonding diagram



2.5. Traceability

2.5.1. Wafer Fab information

Wafer fab name / location	ST Catania CTM8 (Italy)
Wafer diameter (inches)	8”
Silicon process technology	VIPower M0A9
Die finishing front side	Teos + SiN + Polymide
Die finishing back side	Ti-NiV-Ag
Die size (micron)	3070 x 2895 um
Metal levels/ materials/ thicknesses	3 levels Ti/AlCu/TiN (3.06 µm last level)

2.5.2. Assembly information (used only for Silicon Technology qualification)

Assembly plant name / location	ST Calamba (Philippines)
Package descrition	FRAME QFN 32L 6x6
Die attach material	Glue ATROX 800HT2V-P1
Wire bonding material/diameter	Cu 1.2mils, Cu 2.5mils
Molding compound material	RESIN HITACHI CEL 9240ZHF10W
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL3

2.5.3. Reliability Testing information

Reliability laboratory location	STM Catania (Italy)

2.5.4. Lot Information

Lot1	59316YM	780290N201	

3.Tests Results Summary

3.1. Test results summary (table)

Test method revision reference is the one active at the date of reliability trial execution.

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
PC	A1	JESD22-A113 J-STD-020	24h bake@125°C, including 5 Temperature Cycling Ta=-40°C/+60°C MSL3 3x Reflow simulation Peak Reflow Temp= 260°C 100 Temperature Cycling Ta=-50°C/+150°C	1	550	550	0/550/1	Before THB/AC/TC/PTC/HTOL
THB	A2	JESD22 A101 JESD22 A110	Ta=85°C, 85%RH, Duration= 1000hrs	1	77	77	0/77/1	
AC	A3	JESD22 A102 or JESD22 A118 or JESD22- A101	**ENV. SEQ.** **Environmental Sequence** TC (Ta=-55°C / +150°C for 100 cycles) + AC (Ta=121°C, Pa=2atm for 96 hours)	1	77	77	0/77/1	
TC	A4	JESD22 A104	Ta=-55°C /+150 °C Duration= 1000cy	1	77	77	0/77/1	
PTC	A5	JESD22 A105	V_{CC}: 16V; PWM: 100Hz Duty Cycle: 68% Load: 1x10W for CH1-CH4 Load: 1x P27W for CH0, CH5 Ta=-40°C /+125 °C Duration=1000 cyc	1	45	45	0/45/1	
HTSL	A6	JESD22 A103	Ta= 150°C Duration= 1000hrs	1	45	45	0/45/1	

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
HTOL	B1	JESD22 A108	Bias dynamic stress (**OLT**) TJ=150°C Duration= 1000hrs	1	77	77	0/77/1	V_{CC}: 16V Load: 1x10W for CH1-CH4 Load: 1x P27W for CH0, CH5 PWM: 100Hz Duty Cycle: 68% Duration: 1000 hours
HTOL	B1	JESD22 A108	Bias static stress (**HTB**) Ta=150°C, Vcc=28V Duration= 1000hrs	-	-	-	-	Family approach **VN9D30Q100J**
ELFR	B2	AEC-Q100-008	Ta max=150°C Duration=24hrs	3	800	2400	0/800/3	Family data
EDR	B3	AEC-Q100-005	Specific tests and conditions to be defined in case of NVM	-	-	-	-	Not Applicable

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
WBS	C1	AEC-Q100-001 AEC-Q003	Wire Bond Shear: (Cpk > 1.67)	1	min 5 units	min 5 units	All measurement within spec limits	30 bonds/minimum 5 units
WBP	C2	Mil-STD-883, Method 2011 AEC-Q003	Wire Bond Pull: (Cpk > 1.67)	1	min 5 units	min 5 units	All measurement within spec limits	30 bonds/minimum 5 units
SD	C3	JESD22 B102 JSTD-002D	Solderability: (>95% coverage) 8hr steam aging prior to testing	1	15	15	All measurement within spec limits	
PD	C4	JESD22 B100, JESD22 B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	1	10	10	All measurement within spec limits	
SBS	C5	AEC-Q100-010 AEC-Q003	Only for BGA package	-	-	-	-	Not Applicable
LI	C6	JESD22 B105	Not required for Surface Mount Devices	-	-	-	-	Not Applicable

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
EM	D1	JESD61	Data, test method and criteria available upon request	–	–	–	–	Technology Family data
TDDB	D2	JESD35	Data, test method and criteria available upon request	–	–	–	–	
HCI	D3	JESD60 & 28	Data, test method and criteria available upon request	–	–	–	–	
NBTI	D4	JESD90	Data, test method and criteria available upon request	–	–	–	–	
SM	D5	JESD61, 87, & 202	Data, test method and criteria available upon request	–	–	–	–	

TEST GROUP E – ELECTRICAL VERIFICATION

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test	All	All	All	Passed	All parametric and functional tests
HBM	E2	AEC-Q100-002	Target: ±2kV	1	See test method		VCC; $OUT_{0,1,2,3,4,5}$: +/-4KV DI0, DI1: +/-1.5KV PMW_CLK, VDD, SDO, SCK, SDI CSN: +/-1.5KV	
CDM	E3	AEC-Q100-011	Target: ±750V on corner pins ± 500V all others	1	See test method		All pins: ±1000V	
LU	E4	AEC-Q100-004	Current Injection Class I – Level B (see notes for criteria)	1	6	6	Device passes class II level B ±50mA at V_{CC}=28V Overvoltage: passed	
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk >1.67)	1	30	30	Passed	Performed with testing program applied on present silicon cut
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	–	–	–	–	
SC	E10	AEC Q100-012	Short Circuit Characterization	3	40	120	See results in section 4 of this report	
SER	E11	JESD89-1 JESD89-2 JESD89-3	Applicable to devices with memory	–	–	–		Not Applicable
LF	E12	AEC-Q005	Lead(Pb) Free: (see AEC-Q005)	–	–	–		Covered by Test Group A&C

TEST GROUP F – DEFECT SCREENING TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	Not performed on qualification lots. It will be implemented starting from first production lot				
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)					

TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS

Test	#	Reference	AEC-Q100 STM Test Conditions	Lots	S.S.	Total	Results FAIL/SS/Lots	Comments
MS	G1	JESD22 B104	Mechanical Shock	Not Applicable: not for plastic packaged devices				
VFV	G2	JESD22 B103	Variable Frequency Vibration					
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration					
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak					
DROP	G5		Drop Test, Package Drop					
LT	G6	MIL-STD-883 Method 2004	Lid Torque					
DS	G7	MIL-STD-883 Method 2019	Die Shear					
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor					

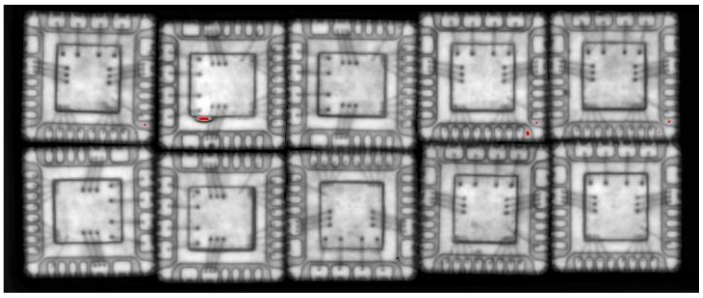
4.ANNEXES

4.1. SHORT CIRCUIT TEST RESULTS

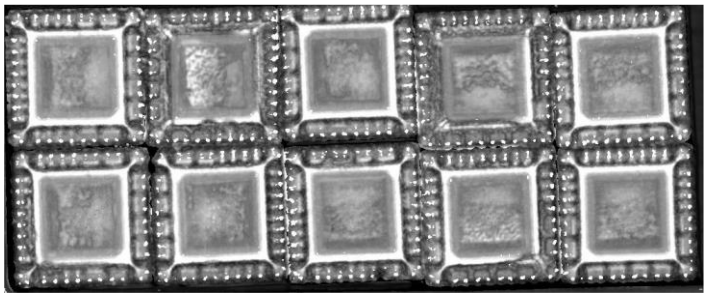
AEC-Q100 STM `Test Conditions	Stressed Output	Samples Size/Lots	Cumulative Failures	# of Cycles	Grade
Cold Short Circuit, Autorestart, Long Pulse (300ms), Tc_start=+25°C, Load	All channels 5units/channel	30/3	No fail	>1M	Grade A
Cold Short Circuit, Autorestart, Long Pulse (300ms), Tc_start=-40°C, Load	All channels 5units/channel	30/3	No fail	>300K	Grade B
Hot Repetitive Short Circuit,Load	All channels 5units/channel	30/3	No fail	>1K hours	
Latch mode Tc-start=+85°C, Load	All channels 5units/channel	30/3	No fail	>1M	Grade A

4.2. PHYSICAL ANALYSIS AFTER 1x STRESS TEST DURATION

The Scanning Acoustic Microscopy (SAM) analysis after ES, TC, HTSL and THB stress tests show no significant delamination at the die and lead-frame interfaces with molding compound:

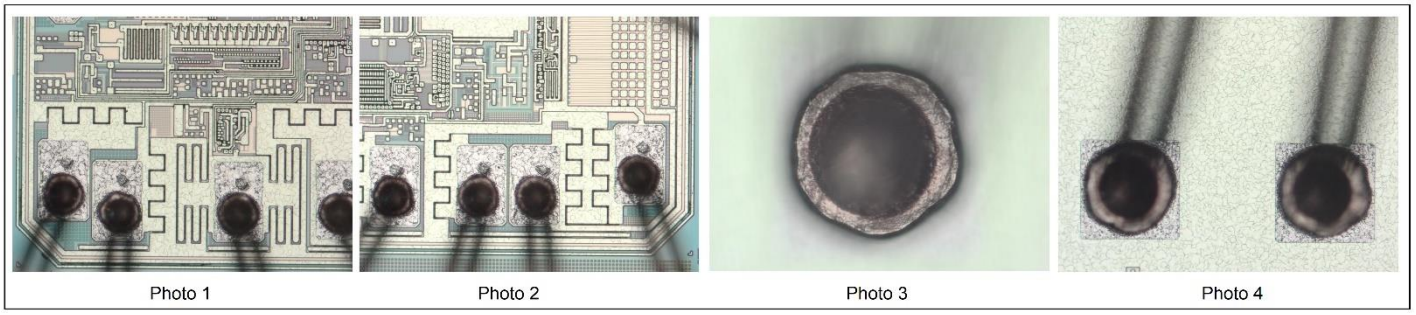


SAM (TOP) after Thermal Cycles (TC)



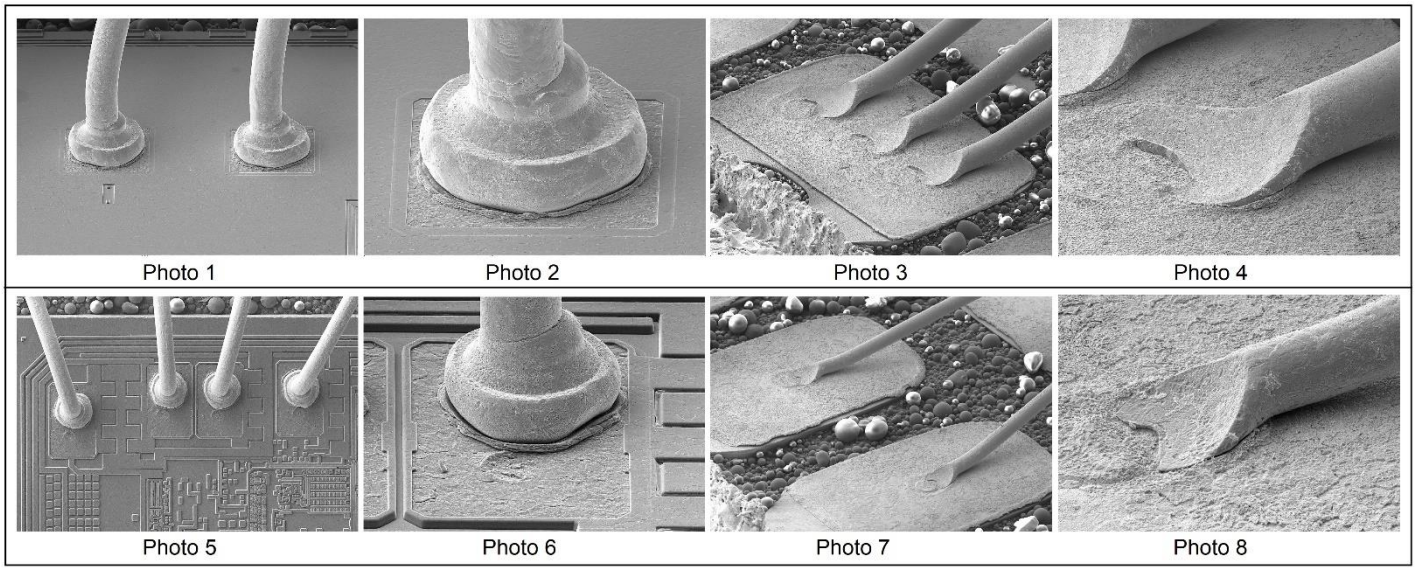
SAM (BTM) after Thermal Cycles (TC)

The internal visual inspection performed by Optical Microscopy pointed out neither significant degradation of metals or passivation nor corrosion/oxidation or remarkable passivation cracks:



VI after Thermal Cycles (TC): Cu 1.2mils pictures 1÷2, Cu 2.5mils pictures 3÷4

The Scanning Electron Microscopy (SEM) inspection after Thermal Cycles (TC) didn't show any significant wire-bonds degradation / fatigue:



SEM after Thermal Cycles (TC): Cu 2.5mils pictures 1÷4, Cu1.2mils pictures 5÷8

Wire bonding strength after Thermal Cycles (TC), Temperature Humidity Bias (THB), High Thermal Storage (HTS) and Environmetal Sequence (ES) stress tests has been successfully verified through Wire Bond Pull (WBP) and Wire Bond Shear (WBS) test:

Wire Bond Pull (WBP)					
Stress test	**Wire typology**	**Low Spec Limit (g)**	**Sample size**	**Result**	**Lot 1**
Thermal Cycles	Cu 2.5mils	23	30 bonds from minimum 5 units	Avg value (g)	70.7
				Min value (g)	56.9
	Cu 1.2mils	5.5	30 bonds from minimum 5 units	Avg value (g)	13.0
				Min value (g)	10.7
Temperature Humidity Bias	Cu 2.5mils	23	30 bonds from minimum 5 units	Avg value (g)	64.9
				Min value (g)	46.9
	Cu 1.2mils	5.5	30 bonds from minimum 5 units	Avg value (g)	15.1
				Min value (g)	11.5
High Thermal Storage	Cu 2.5mils	23	30 bonds from minimum 5 units	Avg value (g)	73.2
				Min value (g)	53.4
	Cu 1.2mils	5.5	30 bonds from minimum 5 units	Avg value (g)	15.0
				Min value (g)	11.2
Environmental Sequence	Cu 2.5mils	23	30 bonds from minimum 5 units	Avg value (g)	67.9
				Min value (g)	56.9
	Cu 1.2mils	5.5	30 bonds from minimum 5 units	Avg value (g)	14.6
				Min value (g)	11.4

Wire Bond Shear (WBS)					
Stress test	**Wire typology**	**Low Spec Limit (g)**	**Sample size**	**Result**	**Lot 1**
Thermal Cycles	Cu 2.5mils	114.7	30 bonds from minimum 5 units	Avg value (g)	208.6
				Min value (g)	185.0
	Cu 1.2mils	26.9	30 bonds from minimum 5 units	Avg value (g)	39.6
				Min value (g)	32.5
Temperature Humidity Bias	Cu 2.5mils	117	30 bonds from minimum 5 units	Avg value (g)	219.3
				Min value (g)	208.0
	Cu 1.2mils	26	30 bonds from minimum 5 units	Avg value (g)	43.7
				Min value (g)	41.0
High Thermal Storage	Cu 2.5mils	117	30 bonds from minimum 5 units	Avg value (g)	225.2
				Min value (g)	205.0
	Cu 1.2mils	26	30 bonds from minimum 5 units	Avg value (g)	44.4
				Min value (g)	41.4
Environmental Sequence	Cu 2.5mils	117	30 bonds from minimum 5 units	Avg value (g)	217.3
				Min value (g)	201.0
	Cu 1.2mils	26	30 bonds from minimum 5 units	Avg value (g)	43.2
				Min value (g)	37.7

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