PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	ADG/22/13867
1.3 Title of PCN	STH10N80K5-2AG Wafer Front-end Capacity Extension (SG8" Singapore)
1.4 Product Category	Power MOSFET HV
1.5 Issue date	2022-12-23

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Maurizio GIUDICE
2.1.2 Marketing Manager	Paolo PETRALI
2.1.3 Quality Manager	Vincenzo MILITANO

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Transfer	Line transfer for a full process or process brick (process step, control plan, recipes) from one site to another site: Wafer fabrication	Singapore SG8 8"

4. Description of change		
	Old	New
4.1 Description	STH10N80K5-2AG is manufactured in the 8" wafer line of (CTM8 Catania)	STH10N80K5-2AG is manufactured in the 8" wafer line of (SG8" Singapore)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	no impact	

5. Reason / motivation for change	
5.1 Motivation	STH10N80K5-2AG front-end Capacity Extension
5.2 Customer Benefit	CAPACITY INCREASE

6. Marking of parts / traceability of change	
6.1 Description	By internal traceability and dedicated FG code

7. Timing / schedule	
7.1 Date of qualification results	2022-12-21
7.2 Intended start of delivery	2023-06-30
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13867 RERPTD22058_2.0__STH10N80K5-2AG_VK9HA1_SG8_H2PAK-2_STS.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2022-12-23

9. Attachments (additional documentations)
13867 Public product.pdf 13867 13867.pdf 13867 RERPTD22058_2.0__STH10N80K5-2AG_VK9HA1_SG8_H2PAK-2_STS.pdf

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	STH10N80K5-2AG	

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Product/process change notification: ADG/22/13867

Power Transistor Sub-Group

High Voltage Division

Automotive & Discrete Group (ADG)

STH10N80K5-2AG Wafer Front-end Capacity Extension (SG8" Singapore)
Automotive

Product family	Technology	Package
Power MOSFET HV	MDmesh K5	H²PAK-2

Description of the change

Following the continuous improvement of our service and to increase Front-end Capacity, this document is announcing the new 8" wafer line for MDMesh K5 Technology of Power MOSFET Transistors in ST's SG8" Singapore FAB.
STH10N80K5-2AG manufactured in 8" wafer size of SG8" Singapore FAB, guarantees the same quality and electrical characteristics as per current production.

Yours faithfully
Catania, 30 December 2022

Reason

to increase Front-end Capacity.

Date of implementation

06/30/2023

Impact of the change	
Form	
Fit	
Function	
Reliability	
Processibility	Yes

APPENDIX 2: QUALIFICATION PLAN

#	Product	Package	Sample size	Criteria
1	STH10N80K5-2AG	H^2PAK-2		
2				
3				
4				
5				
…				

Samples availability:
Any other sample request will be processed and scheduled by HV Business Unit upon request.

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Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : STH10N80K5-2AG Wafer Front-end Capacity Extension (SG8” Singapore)

PCN Reference : ADG/22/13867

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STH10N80K5-2AG		

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STH10N80K5-2AG (VK9HA1)
ST SG8 (Singapore) Wafer FAB
K5 Technology Second source activation H2PAK ST Shenzhen (China)
Reliability Evaluation Report

General Information	
Commercial Product	STH10N80K5-2AG
Product Line	VK9HA1
Silicon process Technology	MDmesh™ K5
Package	H2PAK-2

Note: *this document is a summary of the qualification plan that will be performed in good faith by STMicroelectronics to evaluate the electronic devices conformance to its specific mission profile and release them to mass production for Automotive Application. This document and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Revision history

Rev.	Changes description	Author	Date
1.0	First release	A.Settinieri	04th July 2022
2.0	Final release		29th July 2022

Approved by

Function	Location	Name	Date
Division Reliability Manager	ST Catania (Italy)	V. Giuffrida	29th July 2022

Table of Contents

1. Reliability Evaluation Overview

1.1. Objective

Aim of this report is to present the results of the reliability evaluations performed to activate ST SG8 Ang Mo Kio (Singapore) 8" Wafer Fab to manufacture **STH10N80K5-2AG** (VK9HA1 as ST internal silicon line), chosen as test vehicle to release in production the Power MOSFET High Voltage product family designed in MDmesh™ K5 Technology, as second source in addition to ST CT8 (Italy) Wafer Fab. The selected test vehicle is assembled in package H2PAK-2 in ST Shenzhen (China) Assembly Plant.

Reliability Strategy and Test Plan

1.2. Reliability strategy

Reliability trials performed as part of this reliability evaluation are in agreement with **AEC-Q101 Rev.E** and **ST 0061692** specification and are listed in below Test Plan.
For details on test conditions, generic data used and specifications references, refer to test results summary in section 3.

1.2.1. Test Plan

AEC-Q101 Test Plan Table (1x mission profile coverage)

TEST GROUP	#	Data Type	TEST NAME	DESCRIPTION / COMMENTS	TEST FLAG
A ACCELERATED ENVIRONMENT STRESS TESTS	A1	1	PC	Preconditioning	Yes
	A2	1	HAST	Highly Accelerated Stress Test	No
	A2 alt	1	H3TRB	High Humidity High Temp. Reverse Bias	Yes
	A3	1	UHAST	Unbiased Highly Accelerated Stress Test	No
	A3 alt	1	AC	Autoclave	Yes
	A4	1	TC	Temperature Cycling	Yes
	A4a	1	TCHT	Temperature Cycling Hot Test	Yes
	A4a alt	1	TCDT	Temperature Cycling Delamination Test	Yes
	A5	1	IOL	Intermittent Operational Life	Yes
	A5alt	1	PTC	Power Temperature Cycling	No
B ACCELERATED LIFETIME SIMULATION TESTS	B1	1	HTRB	High Temperature Reverse Bias	Yes
	B1a	1	ACBV	AC blocking voltage	Not Applicable
	B1b	1	SSOP	Steady State Operational	Not Applicable
	B2	1	HTGB	High Temperature Gate Bias	Yes
C PACKAGE ASSEMBLY INTEGRITY TESTS	C1	1	DPA	Destructive Physical Analysis	Yes
	C2	2	PD	Physical Dimension	Yes
	C3	3	WBP	Wire Bond Pull Strength	Yes
	C4	3	WBS	Wire Bond Shear Strength	Yes
	C5	3	DS	Die Shear	Not Applicable
	C6	2	TS	Terminal Strength	Not Applicable
	C7	2	RTS	Resistance to Solvents	Not Applicable
	C8	2	RSH	Resistance to Solder Heat	Not Applicable

	C9	3	TR	Thermal Resistance	Yes
	C10	2	SD	Solderability	Not Applicable
	C11	3	WG	Whisker Growth Evaluation	Not Applicable
	C12	2	CA	Constant Acceleration	Not Applicable
	C13	2	VVF	Vibration Variable Frequency	Not Applicable
	C14	2	MS	Mechanical Shock	Not Applicable
	C15	2	HER	Hermeticity	Not Applicable
D DIE FABRICATION RELIABILITY TESTS	D1	3	DI	Dielectric Integrity	Yes
E ELECTRICAL VERIFICATION TESTS	E0	1	EV	External Visual	Yes
	E1	1	TEST	Pre- and Post-Stress Electrical Test	Yes
	E2	1	PV	Parametric Verification	Yes
	E3	1	ESDH	ESD HBM Characterization	Yes
	E4	2	ESDC	ESD CDM Characterization	Yes
	E5	3	UIS	Unclamped Inductive Switching	Yes
	E6	3	SC	Short Circuit Characterization	No

1.3. Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

Based on the overall results obtained on3 lots of the product **STH10N80K5-2AG** (VK9HA1 as ST internal silicon line), designed in MDmesh K5 Technology, diffused in ST Ang Mo Kio SG8 8" (Singapore) Wafer Fab, assembled in package H2PAK in ST Shenzhen (China) Assembly Plant, has positively passed reliability evaluation performed in agreement with **AEC-Q101 Rev.E** and **ST 0061692** specification.

2. Product Characteristics

2.1. Generalities

2.1.1. Test vehicle

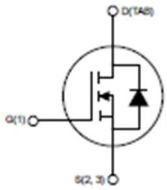
life.augmented

STH10N80K5-2AG

Datasheet

Automotive-grade N-channel 800 V, 0.60 Ω typ., 8 A MDmesh K5 Power MOSFET in an H²PAK-2 package

H²PAK-2



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH10N80K5-2AG	800 V	0.68 Ω	8 A

- AEC-Q101 qualified
- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested

Applications

- Switching applications

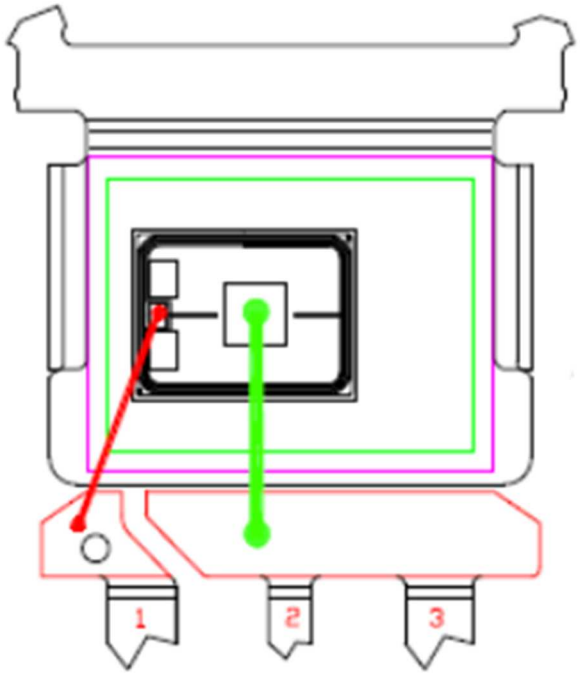
Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
STH10N80K5-2AG

Product summary	
Order code	STH10N80K5-2AG
Marking	10N80K5
Package	H²PAK-2
Packing	Tape and reel

2.2. Pin Connection/Bonding Diagram



2.3. Traceability

2.3.1. Wafer Fab information

Wafer fab name / location	ST Ang Mo Kio SG8 (Singapore)
Wafer diameter (inches)	8”
Silicon process technology	MDmesh K5
Die finishing front side	TEOS/SiN/Polyimide
Die finishing back side	Ti-NiV-Ag
Die size (micron)	4130x3180 um
Metal levels/ materials/ thicknesses	Ti/TiN/TiAlCu (4.6um)

2.3.2. Assembly Information

Assembly plant name / location	ST Shenzhen (China)
Package description	H2PAK 2L
Lead frame/Substrate	FRAME D2PAK 3L Mon HC Ve1 SelNi/NiP
Die attach material	PREFORM Pb/Ag/Sn 95.5/2.5/2
Wire bonding material/diameter	Wires: (Gate) Al/Mg 5 mils (Gate), (Source) Al 10mils
Molding compound material	RESIN SUMITOMO EME7026
Package Moisture Sensitivity Level (JEDEC J-STD020D)	MSL1

2.3.3. Reliability Testing Information

Reliability laboratory location	STM Catania (Italy)

3. Test summary details

3.1. Lot Information:

Lot #	Diffusion Lot	Trececode	Note
Lot1	VC113F92	GK1321VS	
Lot2	VC113F90	GK1321VQ	
Lot3	VC113F91	GK1321VR	

3.2. Test Summary table results

Test method revision reference is the one active at the date of reliability trial execution.

Test	#	Reference	**AEC-Q101 (Group A)** STM Test Conditions	Lots	S.S.	Total	Results Fail/SS/lots	Comments
PC	A1	JEDEC/IPC J-STD-020 JESD22-A-113	- 24h bake@125°C - MSL1: 168h moisture soak @ TA=85°C RH=85% - 3x Reflow simulation with Peak Reflow Temp= 245°C	3	308	924	Passed	All devices for H3TRB, AC, TC and IOL tests
HAST	A2	-	-	-	-	-		covered by H3TRB
H3TRB	A2 alt	JESD22A-101	Ta=85°C, RH=85% Vds =100V, 1000h	3	77	231	0/77/3	
UHAST	A3	-	-	-	-	-		covered by AC
AC	A3 alt	JESD22 A-102	**ENV. SEQ. (ES)** **Environmental Sequence** TC: Ta=-55/150°C, 100cy + AC: Ta=121°C, RH100%, Pa=2atm for 96 hours	3	77	231	0/77/3	
TC	A4	JESD22A-104 Appendix 6 J-STD-035	Ta=-55°C /+150°C, 1000cy	3	77	231	0/77/3	
TCHT	A4a		125°C TEST after TC					
TCDT	A4a alt		100% AM inspection after TC					
IOL	A5	MIL-STD-750 Method 1037	15Kcy / ΔTj ≥ 100°C	3	77	231	0/77/3	
PTC	A5alt	-	-	-	-	-		covered by IOL
Test	#	Reference	**AEC-Q101 (Group B)** STM Test Conditions	Lots	S.S.	Total	Results Fail/SS/lots	Comments
HTRB	B1	JESD22 A-108	Tj=150°C, Vds=800V 1000h	3	77	231	0/77/3	
ACBV	B1a	-	-	-	-	-		Not Applicable Thyristors only
SSOP	B1b	-	-	-	-	-		Not Applicable Voltage Regulator only
HTGB	B2	JESD22 A-108	Tj=150°C, Vgs= +30V, 1000h	3	77	231	0/77/3	

			Tj=150°C, Vgs= -30V, 1000h	3	77	231	0/77/3	
Test	#	Reference	**AEC-Q101 (Group C)** STM Test Conditions	Lots	S.S.	Total	Results Fail/SS/lots	Comments
DPA	C1	AECQ101-004 Section 4		1	4	4	Done	After H3TRB, TC
PD	C2	JEDEC JESD22-B-100		1	30	30	Done	From assembly data
WBP	C3	AEC Q006		1	5	5	Passed	From assembly data
WBS	C4	AEC Q101- 003 JESD22 B116		1	5	5	Passed	From assembly data
DS	C5	MIL-STD- 750-2 Method 2017	Not applicable: only for new package.	-	-	-	-	Data type 2
TS	C6	MIL-STD- 750-2 Method 2017		-	-	-	-	
RTS	C7	JEDEC JESD22-B-106		-	-	-	-	
RSH	C8	JEDEC JESD22-A- 111(SMD), or B-106 (PTH)		-	-	-	-	
TR	C9	JEDEC JESD 24-3,24- 4,24-6 as appropriate		1	10	10	Passed	From assembly data
SD	C10	JEDEC J-STD-002	Not applicable: only for new package.	-	-	-	-	Data type 2
WG	C11	Not applicable: only for new package. Items C12 through C15 are sequential tests for hermetic packages.		-	-	-	-	Not applicable: only for new package
CA	C12			-	-	-	-	
VVF	C13			-	-	-	-	
MS	C14			-	-	-	-	
HER	C15			-	-	-	-	
Test	#	Reference	**AEC-Q101 (Group D)** STM Test Conditions	Lots	S.S.	Total	Results Fail/SS/lots	Comments
DI	D1	AEC Q101-004 Section 3		1	5	5	Done	

Test	#	Reference	**AEC-Q101 (Group E)** STM Test Conditions	Lots	S.S.	Total	Results Fail/SS/lots	Comments
EV	E0	JEDEC JESD22-B101	All qualification parts submitted for testing	3	539	1617	0/539/3	
TEST	E1	User specification or supplier's standard specification	All qualification parts tested per the requirements of the appropriate part specification	3	539	1617	0/539/3	
PV	E2		All parameters according to user specification	3	25	75	Done	
ESDH	E3	AEC-Q101-001	ESD HBM Characterization	1	30	30	Done	
ESDC	E4	AEC-Q101-005	ESD CDM Characterization	1	30	30	Done	
UIS	E5	AEC-Q101-004 Section 2		1	5	5	Done	
SC	E6	-	-	-	-	-	-	

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