


PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data

1.1 Company		STMicroelectronics International N.V
1.2 PCN No.	APG/14/9004	
1.3 Title of PCN	VIPower housed in PowerSO-30: Wire Sagging Improvement	
1.4 Product Category	VIPower products housed in PowerSSO-36 (VH01/VH02/VH21 lines)	
1.5 Issue date	2014-12-03	

2. PCN Team

2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
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2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Riccardo NICOLOSO
2.1.2 Marketing Manager	Nicola LIPORACE
2.1.3 Quality Manager	Francesco MINERVA

3. Change

3.1 Category	3.2 Type of change	3.3 Manufacturing Location
Materials	New direct material part number (same supplier, different supplier or new supplier), lead frame, resin, wire, ?)	MU1A---ST MUAR - MALAYSIA

4. Description of change

	Old	New
4.1 Description	Lead frame design: Floating die attach paddle - Corner leads not fused together	Lead frame design: Corner leads fused together
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	No Impact in Functionand Realiability	

5. Reason / motivation for change

5.1 Motivation	In ordert o improve quality a modification of lead frame has been implemented. Corner leads are fused together in order to improve wire sagging and to avoid pad tilt/movement during handling
5.2 Customer Benefit	QUALITY IMPROVEMENT

6. Marking of parts / traceability of change

6.1 Description	Dedicated Finished-Good codes
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7. Timing / schedule

7.1 Date of qualification results	2014-11-13
7.2 Intended start of delivery	2015-05-13
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation

8.1 Description	RR002714CT2235_01_VH01_MP3030_Frame change for sagging wires.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	Issue Date	2014-12-03

9. Attachments (additional documentations)	
9004PpPrdtLst.pdf	RR002714CT2235_01_VH01_MPSO30_Frame change for sagging wires.pdf
description.pdf	

10. Affected parts		
10. 1 Current		10.2 New (if applicable)
10.1.1 Customer Part No	10.1.2 Supplier Part No	10.1.2 Supplier Part No
	VND5E004A30-E	
	VNH2SP30-E	
	VNH2SP30TR-E	
	VNH3ASP30-E	
	VNH3SP30-E	
	VNH3SP30TR-E	
	VNH5019A-E	
	VNH5019ATR-E	

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VIPower housed in PowerSO-30: Wire Sagging Improvement

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WHAT:

In order to improve quality a modification of lead frame has been implemented. Corner leads are fused together in order to improve wire sagging and to avoid pad tilt/movement during handling

WHY:

Quality Improvement

HOW:

See enclosed description of the change and qualification report RR002714CT2235

HOW:

Change will be implemented according the following schedule

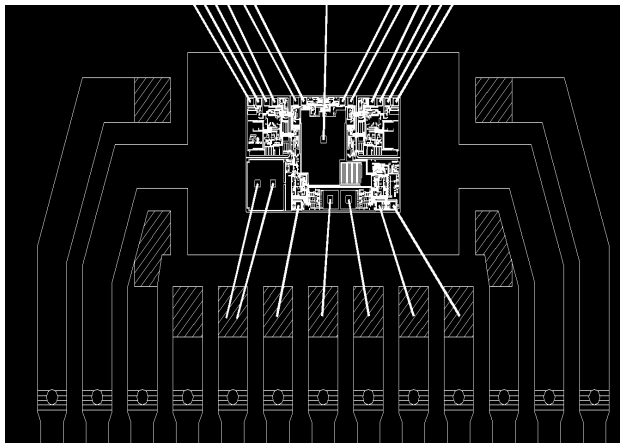
Samples: Available on demand

Qualification results: enclosed to this communication

Implementation: May 2015, but we are ready to implement the change prior this date upon Customer agreement

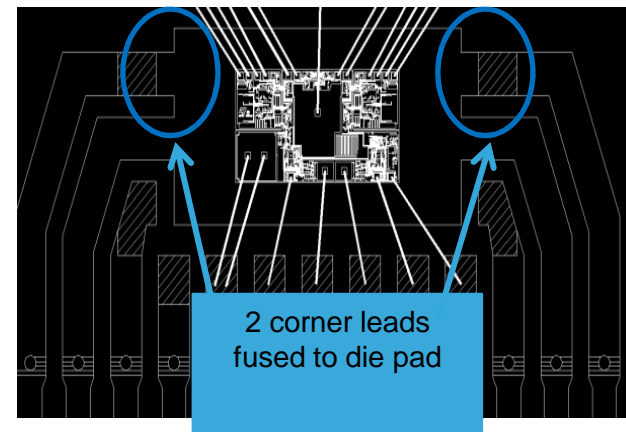
VIPower housed in PowerSO-30: Wire Sagging Improvement

Current



No corner leads are fused together in

New



Corner leads are fused together in order to improve wire sagging and to avoid pad tilt/movement during handling

VND5004ASP30-E (VH01)

Package MultiPowerSO30

New frame for sagging wire improvement

Revision history			
Rev.	Date of Release	Author	Changes description
0.1	September 4 th 2014	F. Ceraulo - APG Q&R Catania	Creation

Table of contents		
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3.3	6	Blocks diagram
4	7	Reliability qualification plan and results – Summary table

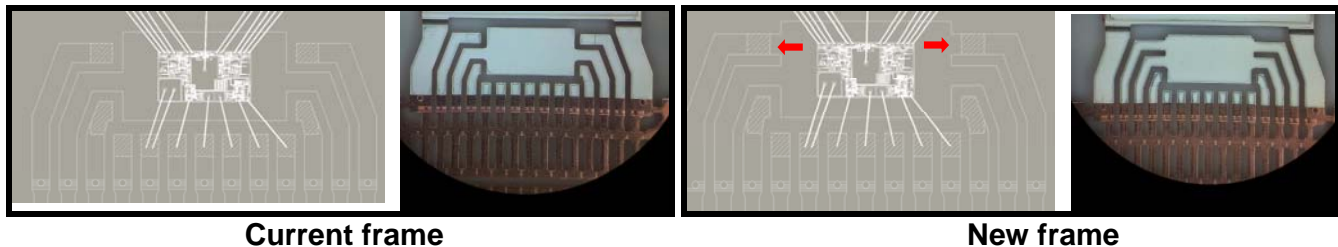
- 1. Reliability evaluations overview

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on **VND5004ASP30-E** (VH01 as ST internal code) chosen as test vehicle to release in production a new frame for package MultiPowerSO30.

This product is a 4mohm Dual Channel High Side Driver with analog current sense for Automotive Applications designed in VIPower M05 technology, composed by two power dice (VNI4 as ST internal silicon line) and one signal die (VNG4 as ST internal silicon line) both diffused in ST AMK6 Ang Mo Kio (Singapore) 6" wafer fab.

The new frame is introduced for sagging wire improvement and was designed to make the floating paddle more rigid reducing the vertical vibration during handling.



Change between the current and the new frames occurs only in a geometry dimension (see red arrows for details) but not in the material or in the assembly configuration.

The qualification was done according to **AEC_Q100 Rev.G** specification following the path described here below:

Test group as per AEC-Q100 Rev.G		Performed (Y/N)	Comment
A	Accelerated Environment Stress	Y	
B	Accelerated Lifetime Simulation	N	Not applicable
C	Package Assembly Integrity	Y	
D	Die Fabrication Reliability	N	Not applicable
E	Electrical Verification	N	Not applicable
F	Defect Screening	N	Not applicable
G	Cavity Package Integrity	N	N/A: not for plastic packaged devices

See details per each test group in section 4 of this report.

In the below table a comparison between the AEC-Q100 and ZVEI requirements for this kind of change (lead frame dimension) vs the applied ST qualification plan is reported:

	Test Group A					Test Group B		Test Group C				Test Group D					Test Group E							
	THB	AC	TC	PTC	HTSL	HTOL	ELFR	WBS	WBP	SD	PD	EM	TDDb	HCI	NBTI	SM	HBM	CDM	LU	ED	GL	EMC	SC	
AEC-Q100		x	x	x						x	x												x	
ZVEI		x	x	x						x	x												x	
ST		x	x					x	x	x	x													

The applied qualification plan was addressed to investigate about failure mechanisms related to the thermo mechanical and humidity stress while the impact of the change is considered negligible vs the failure mechanism related to PTC and SC (no change in wires/assembly configuration/die attach).

1.2 Results

All reliability tests have been completed with positive results neither functional nor parametric rejects were detected at final electrical testing.

The Package Assembly Integrity (test Group C) pointed out neither abnormal break loads nor forbidden failure modes.

Based on the overall positive results we consider the products qualified from a reliability point of view.

- 2. Traceability

Wafer fab information	
Wafer fab manufacturing location	ST AMK6 Ang Mo Kio (Singapore)
Wafer diameter (inches)	6
Silicon process technology	VIPOWER M05
Die finishing back side	Ti-Ni-Au
Die size (micron)	VNG4 (signal): 2800 x 1560 VNI4 (power) : 7990 x 4000
Metal levels / materials	VNG4 (signal): 2 levels / Ti/TiN/Ti/AlSiCu (3.2 µm last level) VNI4 (power) : 1 level / Ti/AlSiCu (4.5 µm)
Die finishing front side	SiN/POLYIMIDE
Diffusion Lots #	VNG4 (signal): 61431X3, VNI4 (power): 63245T5

Assembly Information	
Assembly plant location	ST Muar (Malaysia)
Package description	Multi PowerSO_30
Molding compound	RESIN SUMITOMO EME-G600C
Wires bonding materials/diameters	Au 1.2mils (on signal) / Al 15mils (on power)
Die attach material	GLUE QMI9507 PREFORM Pb/Ag/Sn 97.5/1.5/1
Assembly Lots #	993360NR01 (old frame), 993360NR02 (new frame)

Reliability Information	
Reliability test execution location	ST Catania (Italy)

- 3. Device characteristics

3.1 Generalities



VND5004A-E VND5004ASP30-E

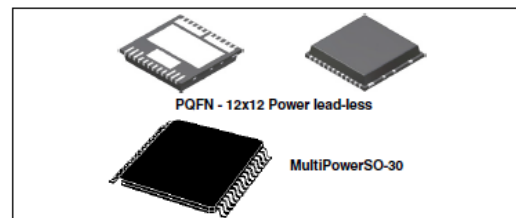
Double 4mΩ high side driver with analog current sense
for automotive applications

Features

Max transient supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 27V
Max On-State resistance (per ch.)	R_{ON}	4 mΩ
Current limitation (typ)	I_{LIMH}	100A
Off state supply current	I_S	2 μA ⁽¹⁾

1. Typical value with all loads connected

- General
 - Inrush current active management by power limitation
 - Very low stand-by current
 - 3.0V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - In compliance with the 2002/95/EC European directive
- Diagnostic functions
 - Proportional load current sense
 - Current sense disable
 - Thermal shutdown indication
- Protection
 - Undervoltage shut-down
 - Overvoltage clamp
 - Load current limitation
 - Thermal shut down
 - Self limiting of fast thermal transients
 - Protection against loss of ground and loss of V_{CC}
 - Reverse battery protection with self switch on of the PowerMOS (see [Application schematic on page 18](#))
 - Electrostatic discharge protection



Application

- All types of resistive, inductive and capacitive loads
- Suitable for power management applications

Description

The VND5004ATR-E and VND5004ASP30-E are devices made using STMicroelectronics VIPower technology. They are intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp and load dump protection circuit protect the devices against transients on the V_{CC} pin (see ISO7637 transient compatibility table). These devices integrate an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the CURRENT SENSE pin is high impedance. Output current limitation protects the devices in overload condition. In case of long duration overload, the devices limit the dissipated power to a safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as a fault condition disappears.

Table 1. Devices summary

Package	Order codes		
	Tube	Tape and Reel	Tray
PQFN-12x12 Power lead-less	-	VND5004ATR-E	VND5004A-E
MultiPowerSO-30	VND5004ASP30-E	VND5004ASP30TR-E	-

Pinout diagram for the ADXL345 (8-Pin WSON) package. The package is shown with pins 1 through 16. Pin 1 is labeled V_{CC} . Pin 2 is labeled NC. Pin 3 is labeled FOR TEST ONLY. Pin 4 is labeled NC. Pin 5 is labeled NC. Pin 6 is labeled GND. Pin 7 is labeled CS_DIS. Pin 8 is labeled CURRENT SENSE 2. Pin 9 is labeled CURRENT SENSE 1. Pin 10 is labeled INPUT 2. Pin 11 is labeled INPUT 1. Pin 12 is labeled NC. Pin 13 is labeled FOR TEST ONLY. Pin 14 is labeled NC. Pin 15 is labeled V_{CC} . Pin 16 is labeled V_{CC} . Pin 17 is labeled V_{CC} . Pin 18 is labeled OUTPUT 2. Pin 19 is labeled OUTPUT 2. Pin 20 is labeled OUTPUT 2. Pin 21 is labeled OUTPUT 2. Pin 22 is labeled OUTPUT 2. Pin 23 is labeled OUTPUT 2. Pin 24 is labeled NC. Pin 25 is labeled OUTPUT 1. Pin 26 is labeled OUTPUT 1. Pin 27 is labeled OUTPUT 1. Pin 28 is labeled OUTPUT 1. Pin 29 is labeled OUTPUT 1. Pin 30 is labeled OUTPUT 1. Pin 31 is labeled V_{CC} . A dashed box labeled V_{CC} Heat Slug covers pins 1 through 16.

The diagram illustrates a dual-channel DC-DC converter system. It features two input channels, INPUT1 and INPUT2, each connected to a GND rail. A CS_DIS signal is also present. The system is powered by a V_{CC} supply and includes a Reverse battery protection block and a V_{CC} clamp. A central LOGIC block manages the system, including Under voltage protection. Each channel has a DRIVER block that controls a power MOSFET and a diode. The MOSFETs are connected to the V_{CC} rail and the output rails, OUTPUT1 and OUTPUT2. The diodes are connected to the output rails and the GND rail. The output current is limited by I_{LIM} and the power dissipation is limited by Pwr_{LIM}. Overtemp. protection is also implemented. The output current is sensed by a current sense resistor (CS_DIS) and the sense voltage is amplified by a gain K to produce CURRENT SENSE1 and CURRENT SENSE2 signals.

- 4. Reliability qualification plan and results

Test group A: Accelerated Environment Stress					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
A1	PC Pre Cond	- Preconditioning according to Jedec JESD22-A113F including 5 Temperature Cycling Ta=-40°C/+60°C - Reflow according to level 3 Jedec JSTD020D-1 - 100 Temperature Cycling Ta=-50°C/+150°C	Before AC, TC		
A2	THB Temp Humidity Bias	Ta=85°C, RH=85%, Vcc=24V for 1000 hours	-	-	Not Applicable
A3	AC Autoclave	ENV. SEQ. Enviromental Sequence TC (Ta=-65°C / +150°C for 100 cycles) + AC (Ta=121°C, Pa=2atm for 96 hours)	77/2	0/77/2	1 Lot old frame 1 Lot new frame
A4	TC Temp. Cycling	Ta=-65°C / +150°C for 500 cycles	77/2	0/77/2	1 Lot old frame 1 Lot new frame
A5	PTC Power Temp. Cycling	Ta=-40°C / +125°C for 1000 cycles.	-	-	Not Applicable
A6	HTSL High Temp. Storage Life	Ta=150°C for 1000 hours.	-	-	Not Applicable

Test group A: Accelerated Environment Stress Robustness activity					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
A4	TC Temp. Cycling	Ta=-50°C / +150°C for 1000 cycles	77/2	0/77/2	1 Lot old frame 1 Lot new frame

Test group B: Accelerated Lifetime Simulation					
AEC #	Test Name	STM Test Conditions	Sample Size/Lots	Results Fails/SS/Lots	Comments
B1	HTOL High Temp. Op. Life	Bias Static stress (JESD22-A108): HTB Tamb=125°C, Vcc=28V for 1000 hours	-	-	Not Applicable
B2	ELFR Early Life Failure Rate	Parts submitted to HTOL per JESD22-A108 requirements; GRADE 1: 24 hours at 150°C	-	-	Not Applicable
B3	EDR Endurance Data Retention	Only for memory devices	-	-	Not Applicable

Test group C: Package Assembly Integrity					
AEC #	Test Name	STM Test Conditions	Sample Size/Lots	Results Fails/SS/Lots	Comments
C1	WBS Wire Bond Shear		30 bonds /minimum 5 units/1 lot	All measurement within spec limits	1 Lot old frame 1 Lot new frame
C2	WBP Wire Bond Pull		30 bonds /minimum 5 units/1 lot	All measurement within spec limits	1 Lot old frame 1 Lot new frame
C3	SD Solderability		15/4	Passed	1 Lot old frame 1 Lot new frame
C4	PD Physical Dimensions		10/4	Passed	1 Lot old frame 1 Lot new frame
C5	SBS Solder Ball Shear	Only for BGA package	-	-	Not Applicable
C6	LI Lead Integrity	Not required for Surface Mount Devices	-	-	Not Applicable

Test group D: Die Fabrication Reliability					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
D1	EM Electromigration		-	-	Not Applicable
D2	TDDB Time Dependent Dielectric Breakdown		-	-	Not Applicable
D3	HCI Hot Carrier Injection		-	-	Not Applicable
D4	NBTI Negative Bias Temperature Instability		-	-	Not Applicable
D5	SM Stress Migration		-	-	Not Applicable

Test group E: Electrical Verification					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
E2	ESD HBM / MM		-	-	Not Applicable
E3	ESD CDM		-	-	Not Applicable
E4	LU Latch-Up		-	-	Not Applicable
E5	ED Electrical Distributions		-	-	Not Applicable
E7	CHAR Characterization		-	-	Not Applicable
E8	GL Gate Leakage		-	-	Not Applicable
E9	EMC Electromagnetic Compatibility		-	-	Not Applicable

E10	SC Short Circuit Characterization	According to AEC-Q100-012	-	Not Applicable
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Test group F: Defects Screening Tests					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
F1	PAT Process Average Testing		Not Applicable		
F2	SBA Statistical Bin/Yield Analysis				

Test group G: Cavity Package Integrity Tests					
AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
G1	MS Mechanical Shock	Not applicable: not for plastic packaged devices			
G2	VFV Variable Frequency Vibration				
G3	CA Constant Acceleration				
G4	GFL Gross/Fine Leak				
G5	DROP Package Drop				
G6	LT Lid Torque				
G7	DS Die Shear				
G8	IWV Internal Water Vapor				