



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-HES/14/8697
Dated 06 Oct 2014

**Qualification of UTAC Fabrication plant as second
source for production flexibility**

Table 1. Change Implementation Schedule

Forecasted implementation date for change	15-Dec-2014
Forecasted availability date of samples for customer	29-Sep-2014
Forecasted date for STMicroelectronics change Qualification Plan results availability	29-Sep-2014
Estimated date of changed product first shipment	05-Jan-2015

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Assembly additional location
Reason for change	To have two back-end sites to support any upside on volume
Description of the change	Additional qualified back-end plant is activated to allow more flexibility and to prepare for potential demand upside
Change Product Identification	See FG
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
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Reliability Evaluation Report

Qualification Subcontract

STTS2004 TDFN 8L 2X3X0.75

General Information		Locations	
Product Line	V829	Wafer fab Front-End 1	Rousset
Product Description	Temperature Sensor with SPD EEPROM	Wafer fab Front-End 2	Crolles 200
P/N	STTS2004B2DN3F	Assembly plant	UTAC Thai Limited
Product Group	AMS	Reliability Lab	Catania Reliability Lab
Product division	HIGH-END SENSOR and ANALOG	Reliability assessment	Pass.
Package	TDFN 8L 2X3X0.75		
Silicon Process technology Front-End 1	CMOSF8HP4		
Silicon Process technology Front-End 2	HCMOS6S		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.1	22-Nov-2013	7	Vito Gisabella	G.Presti	Final Report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
RER6043-386-W-12	Report <i>STTS2002R UMC dice with Global Foundry EEPROM</i>

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the subcontractor as additional source of fabrication of STTS2004. Considering the subcontractor has been already qualified for similar product (STTS2002R) in same package, qualification was based on previous STTS2002 qualification plus MSL assessment on STTS2004.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

2.2 V memory module temperature sensor with a 4 Kb SPD EEPROM.

4.2 Construction note

STTS2004(TEMP SENSOR)	
Wafer/Die fab. information	
Wafer fab manufacturing location	Crolles
Technology	HCMOS6S
Die finishing back side	RAW SILICON
Die size	1454 um x 934 um
Passivation type	PSG + NITRIDE + PIX
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APEE TPY
Tester	J750
Assembly information	
Assembly site	UTAC
Package description	TDFN 8L 2 x 3 x 0.75 pitch 0.50 mm
Molding compound	Epoxy
Die pad size	1.80 x 2.00
Wires bonding materials/diameters	Au 0,8MIL
Final testing information	
Testing location	UTAC Thai Limited
Tester	Maverick (Nextest)

F34E41TP (EEPROM)	
Wafer/Die fab. information	
Wafer fab manufacturing location	Rousset
Technology	CMOSF8HP4
Die finishing back side	Raw Silicon - Back Grinding
Die size	582 x 604 um
Passivation type	USG + NitUV (HFP USG+UV Nitride)

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Process/ Package	Product Line	Comments
1	J243ZFP1	3A078460	FN34000K	HCMOS6S/CMOSF8HP4 TDFN 8L 2x3x0.75	V829	

5.2 Test plan and results summary

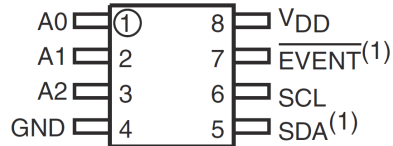
STTS2004

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
						Lot 1	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	100	Final	0/100	

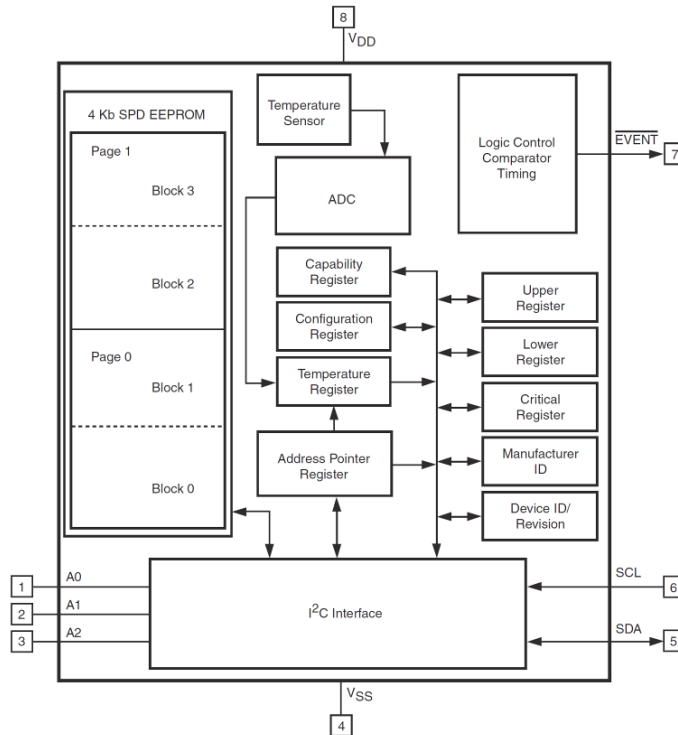
6 ANNEXES

6.1 Device details

6.1.1 Pin connection



6.1.2 Block diagram



6.2 Tests Description

Test name	Description	Purpose
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.



Public Products List

PCN Title : Qualification of UTAC Fabrication plant as second source for production flexibility

PCN Reference : AMS-HES/14/8697

PCN Created on : 28-OCT-2014

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

STTS2004B2DN3F

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