



## PRODUCT/PROCESS CHANGE NOTIFICATION

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PCN IPG-IPC/14/8653  
Dated 18 Aug 2014

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**ST1CC40 : Metal mask change**

**Table 1. Change Implementation Schedule**

Forecasted implementation date for change	01-Nov-2014
Forecasted availability date of samples for customer	15-Oct-2014
Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability	11-Aug-2014
Estimated date of changed product first shipment	01-Jan-2015

**Table 2. Change Identification**

Product Identification (Product Family/Commercial Product)	ST1CC40DR and ST1CC40PUR
Type of change	Product design change
Reason for change	Yield improvement
Description of the change	We have introduced a metal mask modification on the product line UI94 in order to improve the yield. This change will not affect any conditions related to form, fit, function, quality and reliability of this product.
Change Product Identification	By a new Finished Goods code
Manufacturing Location(s)	

## DOCUMENT APPROVAL

Name	Function
Merisio, Massimiliano	Marketing Manager
Merisio, Massimiliano	Product Manager
Moretti, Paolo	Q.A. Manager



## ATTACHMENT TO PCN IPG-IPC/14/8653

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### **WHAT:**

We have introduced a metal mask modification on product line UI94. The involved products are ST1CC40DR and ST1CC40PUR. This change will not affect any conditions related to form, fit, function, quality and reliability of these products.

### **WHY:**

In order to improve the yield.

### **HOW:**

The new revision has been qualified by extension on the former version, see attached Product Reliability Certificate. A new internal part number (Finished Goods code) will identify the change.

### **WHEN:**

The change should be implemented starting November 2014, based on material availability and relevant version phase out and phase in. Samples can be delivered upon request, in 6/8 weeks A.R.O.



## Reliability Report

*New Product*  
**ST1S40P-UA27Y1P**

**VFDFPN 4X4X1.0 8L PITCH 0.8 package**

### General Information

Product Line	UA27X1P
Product Description	4A, 900KHz, MONOLITHIC SYNCHRONOUS STEP-DOWN REGULATOR
P/N	ST1S40IPUR
Product Group	MSH-IPC
Product division	LINEAR & INTERFACE
Package	VFDFPN 4X4X1.0 8L PITCH
Silicon Process technology	0,8 BCD6S
Production mask set rev	AY19A

### Locations

Wafer fab	CATANIA
Assembly plant	Carsem S
Reliability Lab	Catania Site
Reliability assessment	Pass

## DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.1	21-Sept-2010	7	Angelo Donzuso Giuseppe Giacopello	Giovanni Presti	Second issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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## **1 APPLICABLE AND REFERENCE DOCUMENTS**

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

## **2 GLOSSARY**

DUT	Device Under Test
SS	Sample Size

## **3 RELIABILITY EVALUATION OVERVIEW**

### **3.1 Objectives**

ST1S40-UA27X1P in VFDFPN 4X4X1.0 8L (New Product Qualification)

### **3.2 Conclusion**

Final reliability results are positive.

Present evaluation is valid for ST1S40I, ST1CC40 and ST1S41 versions



## 4 DEVICE CHARACTERISTICS

### 4.1 Device description

#### ST1S40 V13 Datasheet

The ST1S40 is a step-down high-efficiency PWM current mode switching regulator able to provide up to 4A of output current. The device operates with an input supply range from 4V to 18V and provide an adjustable output voltage from 0.8V (VFB) to  $0.85 \times V_{IN\_SW}$  [ $V_{OUT} = V_{FB} \times (1 + R1/R2)$ ]. It either operates with 800KHz fixed frequency. The high switching frequency allows the use of tiny SMD external components, while the integrated synchronous rectifier saves the use of the schottky diode. The ST1S40 provides excellent transient response. The device is protected against thermal overheating, switching over current and output short circuit. The ST1S40 is the ideal choice for Point of Load regulators or for LDO pre-regulation.

### 4.2 Construction note

P/N ST1S40IPUR	
<b>Wafer/Die fab. information</b>	
Wafer fab manufacturing location	CATANIA
Technology	BCD6S
Process family	BCD6S-3M_AB
Die finishing back side	Cr/NiV/Au
Die size	1725 X 1840 UM
Bond pad metallization layers	3
Passivation type	P-VAPOX/NITRIDE/POLYIMIDE(PIQ)
Poly silicon layers	3
<b>Assembly information</b>	
Assembly site	CARSEM S
Package description	VFDFPN 4X4X1.0 8L PITCH 0.8
Molding compound	Sumitomo G770H
Die attach material	Loctite QMI519
Die pad size	91x91 UM
Wire bonding process	n.a.
Wires bonding materials/diameters	Au 1.3mils
<b>Final testing information</b>	
Testing location	CATANIA
Tester	ASL3K
Test program	UA27_FT



## 5 TESTS RESULTS SUMMARY

### 5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Trace Code	Package	Product Line	Comments
1	P9204XHA	S314611991	MY3I*UA27X1P	VFDFPN 4X4X1.0 8L PITCH 0.8	UA27	946

### 5.2 Test plan and results summary

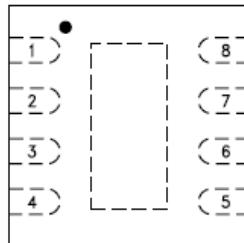
P/N ST1S40IPUR

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		Note
						Lot 1		
<b>Die Oriented Tests</b>								
HTOL	N	JESD22 A-108	Ta = 125°C, BIAS: Vin =+20V VFB = +2,5V	77	168 H	0/77		
					500 H	0/77		
					1000 H	0/77		
HTSL	N	JESD22 A-103	Ta = 150°C	45	168 H	0/45		
					500 H	0/45		
					1000 H	0/45		
<b>Package Oriented Tests</b>								
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	232	Final	Pass	No die delamination	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	77	96 H	0/77		
					168 H	0/77		
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	77	100 cy	0/77		
					200 cy	0/77		
					500 cy	0/77		
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS: Vin =+20V VFB = +2,5V	77	168 H	0/77		
					500 H	0/77		
					1000 H	0/77		

## 6 ANNEXES

### 6.1 Device details

#### 6.1.1 Pin connection

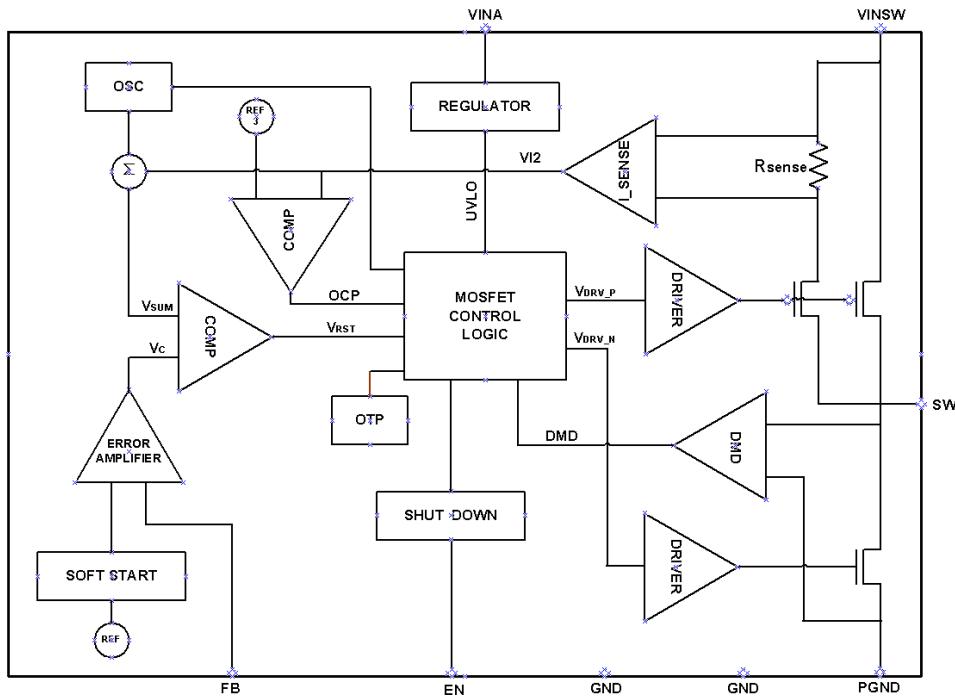


Symbol	Pin Number		Function
	SO8-EP MLP-8L	SO8-BW	
SW	7	1	Switching node to be connected to the inductor
PGND	8	2	Power Ground
VIN_A	1	3	Analog Input Supply Voltage to be tied to VIN power supply source
PG/INH	2	4	Power Good/Inhibit pin active low. Connect to VIN_A if not used
V <sub>FB</sub>	3	5	Feedback Voltage to be connected to external voltage divider to set the Vout from 0.8V up to 0.85*VIN_SW
AGND	4	6	Analog Ground
GND		7	Ground
VIN_SW	6	8	Power Input Supply Voltage to be tied to VIN power supply source
NC	5		No Connected
GND	Epad	---	Ground

MLP-8L

#### 6.1.2 Block diagram

Fig. 2: Block Diagram (INH Versions)



## 6.2 Tests Description

Test name	Description	Purpose
<b>Die Oriented</b>		
<b>HTOL</b> High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
<b>HTSL</b> High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
<b>Package Oriented</b>		
<b>PC</b> Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
<b>AC</b> Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
<b>TC</b> Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
<b>THB</b> Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

## 6.3 Drift Analysis

No parameter deviation.



## Public Products List

PCN Title : ST1CC40 : Metal mask change

PCN Reference : IPG-IPC/14/8653

PCN Created on : 13-AUG-2014

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

### ST COMMERCIAL PRODUCT

ST1CC40DR

ST1CC40PUR

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