PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-PTS/14/8573
Dated 11 Jul 2014

L9958 Family : Activation of Catania 8" Wafer Fab and

Copper Wire Conversion (Au 3mils to Cu 2.5mils)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	30-Sep-2014
Forecasted availability date of samples for customer	31-Jul-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-Sep-2014
Estimated date of changed product first shipment	10-Oct-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	L9958, L9958XP
Type of change	Package assembly process change, Waferfab additional location
Reason for change	Company RoadMap
Description of the change	We are going to activate Catania 8 inchs wafer fab (CT8) on line UP41 (products L9958, L9958XP) and change the wire bonding replacing 3 mils gold (Au) wires with 2.5 mils copper (Cu) wires. Package involved are PowerSO-20 (L9958) and PowerSSO-24 (L9958XP)
Change Product Identification	Dedicated Finished-Good Codes
Manufacturing Location(s)	1]Agrate Ag8 2]St Muar - Malaysia

DOCUMENT APPROVAL

Name	Function
Pernigotti, Elena Maria	Marketing Manager
Cassani, Fabrizio	Product Manager
Pintus, Alberto	Q.A. Manager

L9958 Family: Activation of Catania 8" Wafer Fab and Copper Wire Conversion (Au 3mils to Cu 2.5mils)

WHAT:

We are going to activate Catania 8 inchs wafer fab (CT8) on line UP41 (products L9958, L9958XP) and change the wire bonding replacing 3 mils gold (Au) wires with 2.5 mils copper (Cu) wires. Package involved are PowerSO-20 (L9958) and PowerSSO-24 (L9958XP) .
Together with Catania dual source activation, we are going to release a new silicon version (Metal Change) in order to improve the CPK for one specific parameter. The same metal change has already been implemented on the metal option product (running at rate 2Mpcs/Y) on both Agrate and Catania silicon, showing good CPK.

Risk Assessment: the performance of the metal option product currently in production did not show any issue. Based on this evaluation we are planning to apply the same metal change modification together with the Dual Source activation.

WHY:

Company Roadmap

HOW:

-ESD/LU tests and Electrical distributions will be performed in order to qualify the change.
See enclosed document for details.

WHEN:

Change will be implemented according the following schedule:

Availability of samples:	End of July 2014
Qualification results:	Mid of September 2014
Implementation date for change:	End of September 2014

UP41

L9958 & L9958XP

- Copper Wire Conversion (Au 3mil to Cu 2.5mil)
- Activation of Catania Diffusion Plant

July 2014

UP41 – L9958 & L9958XP

ID Card

UP41

- Commercial Product: L9958 & L9958XP
- Technology: BCD6s (Agrate Diffusion Plant)
- Package: PowerSO20 & PowerSSO24 (Muar Assy Plant)
- Bonding: 3.0mil Au & 1.3mil Au

☐ UP41 is a metal option of UM31 product.

☐ UM31 is diffused in Agrate and Catania Plants, and assembled in Muar Plant in PowerSO20 and PowerSSO24 packages.

UP41 – L9958 & L9958XP

Description of the change

- ☐ For capacity increase and manufacturing flexibility we are going to activate Catania WaferFab as additional diffusion Plant beside Agrate

- ☐ In order to improve the CPK for one specific parameter, we take the opportunity of the dual source activation to release a new silicon version (Metal Change), already implemented on the metal option product (UM31).

- ☐ Progressing on the activities related to copper wire bonding introduction, we are going to replace all 3mil Au wires with 2.5mil Cu wires.
  Thin Au wires (1.3mil) will not be converted to Cu.

- ☐ As announced in PCN APG/13/7949 "Standardization of second bond tip design for PowerSO20 leadframe", we are going to adopt this solution in combination with copper wire bonding introduction on UP41 PowerSO20 package

Qualification Plan

- 2.5mil copper wire on BCD6s technology (Agrate & Catania Plant) on both PowerSO20 and PowerSSO24 packages is already qualified (Test Vehicle: UM31)
  No need to perform any reliability exercise for copper wire introduction on UP41, as full similarity is applicable.

- BCD6s technology is already qualified in Catania diffusion Plant (Test Vehicle: UM31).
  For UP41 Catania silicon validation, the only required stress tests according to AEC-Q100 guidelines, for each package, are:

  - ESD & Latch-Up
  - Electrical Characterization

UM31 (PSO20) – Catania silicon qualification

Reliability results summary

The reliability results are summarized in the following paragraphs.
All the parts have been tested in according to AEC-Q100.

UM31-CG5 BCD6S-CTM8 / PSO20 Hitachi resin – Muar (lot 5138582)

Test name	Conditions		Results Fails/Samples	Note
PC (JL3)	24h bake at 125℃, 192h at 30℃ / 60% R.H., 3 reflow (T_{peak}=245℃)		0/430	Before HTOL, PTC, THB, HTRB, TC, AC
HTOL	See schematic	T_j=150℃, t=1000 h	0/77	1
PTC	See schematic	T_j= -40℃ / +150℃, t=1000 h	0/45	1
THB	See schematic	T_a= 85℃, R.H.= 85%, t=1000 h	0/77	
HTRB	See schematic	T_j=150℃, t=1000 h	0/45	1
TC		T_a= -50℃ / 150℃, n=1000 cy	0/77	2, 3
AC		T_a= 121℃, P=2.08 atm, t=96h	0/77	2
HTSL		T_a= 150℃, t=1000 h	0/45	4
ESD	**HBM**		>3	5
ESD	**CDM**		>3	6
LU	**CI / SO**	JEDEC 78 Class 1, I=+/-100 mA T=125℃	>3	

Notes

[1] No significant drift observed after drift analysis
[2] Visual inspection showed good results
[3] SAM analysis and WBP after TC 1000 cy: passed
[4] WBP after HTSL 1000 h: passed

[5] HBM details

± 4kV	cumulative stress only pins 6,8,13	passed
± 2kV	cumulative stress	passed
± 1kV	cumulative stress	passed
± 2kV	Allpins vs GND	passed
± 2kV	Allpins vs VPS	passed
± 2kV	Allpins vs VDD	passed
± 2kV	Allpins vs VDDIO	passed
± 2kV	IO vs IO	passed
± 2kV	IO,NC vs IO,NC	passed
± 2kV	NC vs PW	passed

[6] CDM details

±750V	corner pins (1, 10, 11, 20)	passed
±500V	Allpins	3 FAIL
±400V	Allpins	3 FAIL

The reliability results are summarized in the following paragraphs.
All the parts have been tested in according to AEC-Q100.

UM31-CG5 BCD6S-CTM8 / PwSSO24 Hitachi resin – Muar (lot 5129744)

Test name	Conditions		Results Fails/Samples	Note
PC (JL3)	24h bake at 125℃, 192h at 30℃ / 60% R.H., 3 reflo w (T_{peak}=260℃)		0/430	Before HTOL, PTC, THB, HTRB, TC, AC
HTOL	See schematic	T_j=150℃, t=1000 h	0/77	1
PTC	See schematic	T_j= -40℃ / +150℃, t=1000 h	0/45	1
THB	See schematic	T_a= 85℃, R.H.= 85%, t=1000 h	0/77	
HTRB	See schematic	T_j=150℃, t=1000 h	0/45	1
TC		T_a= -50℃ / 150℃, n=1000 cy	0/77	2, 3
AC		T_a= 121℃, P=2.08 atm, t=96h	0/77	
HTSL		T_a= 150℃, t=1000 h	0/45	
ESD	**CDM**		>3	4

Notes

[1] No significant drift observed after drift analysis
[2] Visual inspection showed good results
[3] SAM analysis and WBP after TC 1000 cy: passed

[4] CDM details

±750V	corner pins	passed
±500V	Allpins	FAIL
±400V	Allpins	passed
±300V	Allpins	passed

Reliability test conditions and results

TEST NAME	**CONDITIONS [SPEC]**	**REJ / S.S.**				**NOTES**
		AG8 NN	**CT 8 LL**	**CT 8 HH**	**CT 8 NN**	
JL3	24h bake @ 125°C 192h @ 30°C / 60% RH reflow simulation (3 times) at T_{MAX}=245°C [IPC/Jedec J-STD-020D]	0/164	0/164	0/164	0/85	1
JL3 + TC	T_A=-50/+150°C, 1000 cycles T_A=-50/+150°C, 1000 cycles	0/87 0/77	0/87 0/77	0/87 0/77	-	1, 2, 3
HTSL	T_A=150°C, 1000 h T_A=150°C, 2000 h	0/55 0/45	0/55 0/45	0/55 0/45	-	2
JL3 + ES	100 TC (-65/+150°C) + 96h AC (2atm, 121°C)	0/77	0/77	0/77	-	2, 3
JL3 + THB	T_A=85°C, RH=85% 2000h	-	-	-	0/77	
WBP	As per reference specification	0/5	0/5	0/5	-	
WBS	As per reference specification	0/5	0/5	0/5	-	

NOTES:

[1] SAM analysis after JL3 preconditioning and TC shows no delamination at the molding compound interfaces with chip passivation and inner lead fingers. Physiological and uncritical delamination has been observed at die-pad interface (no down-bonding).

[2] Wire bonding strength after the stress has been successfully verified through wire-pull test: neither abnormal break loads, nor forbidden failure modes have been detected.

[3] Visual and/or SEM inspection after the stress test have pointed out no remarkable degradation of silicon passivation, metal interconnects and wire bonds.

Reliability test conditions and results

TEST NAME	**CONDITIONS [SPEC]**	**REJ / S.S.**		**NOTES**
		AG8 NN	**CT 8 NN**	
JL3	24h bake @ 125°C 192h @ 30°C / 60% RH reflow simulation (3 times) at T_{MAX}=245°C [IPC/Jedec J-STD-020D]	0/259	0/259	1
JL3 + TC	T_A=-50/+150°C, 1000 cycles T_A=-50/+150°C, 2000 cycles	0/87 0/77	0/87 0/77	1, 2, 3, 4
HTSL	T_A=150°C, 1000 h T_A=150°C, 2000 h	0/55 0/45	0/55 0/45	2
JL3 + ES	100 TC (-65/+150°C) + 96h AC (2atm, 121°C)	0/77	0/77	2, 3
JL3 + THB	T_A=85°C, RH=85% 1000h	-	0/80	
WBP	As per reference specification	0/5	0/5	
WBS	As per reference specification	0/5	0/5	

NOTES:

[1] SAM analysis after JL3 preconditioning and TC shows no delamination at the molding compound interfaces with chip passivation, and a minor delamination on lead-frame Ag-plated inner tips later assessed through the below-reported destructive items. Physiological and uncritical delamination has been also observed at the die-pad interface (no down-bonding allowed).

[2] Wire bonding strength after the stress has been successfully verified through wire-pull test: neither abnormal break loads, nor forbidden failure modes have been detected.

[3] Visual and/or SEM inspection after the stress test have pointed out no remarkable degradation of silicon passivation, metal interconnects and wire bonds.

[4] Bond-pads of stressed units have been de-layered (so-called “cratering test”) until the base insulating oxide (BPSG) in order to exclude latent cracks propagation to the underlying silicon.

Public Products List

PCN Title : L9958 Family : Activation of Catania 8" Wafer Fab and Copper Wire Conversion (Au 3mils to Cu 2.5mils)
PCN Reference : APG-PTS/14/8573
PCN Created on : 05-AUG-2014

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

L9958
L9958TR
L9958XP
L9958XPTR

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