



## PRODUCT/PROCESS CHANGE NOTIFICATION

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PCN IPG-IPC/14/8450  
Dated 25 Apr 2014

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**VIMIT10, VIPER12AS, VIPER22AS and VN751S :  
Introduction of MSL3 (Moisture Sensitive Level)**

**Table 1. Change Implementation Schedule**

|  |             |
|--|-------------|
| Forecasted implementation date for change  | 01-Jul-2014 |
| Forecasted availability date of samples for customer   | 15-May-2014 |
| Forecasted date for <b>STMicroelectronics</b> change Qualification Plan results availability | 18-Apr-2014 |
| Estimated date of changed product first shipment   | 25-Jul-2014 |

**Table 2. Change Identification**

|   |   |
|---|---|
| Product Identification<br>(Product Family/Commercial Product) | See attached list   |
| Type of change  | Logistics material (label & box)  |
| Reason for change   | Process standardization   |
| Description of the change                                     | As a consequence of PCN IPD-IPC/12/7348 dated 31 July 2012, the products VIMIT10, VIPER12AS, VIPER22AS and VN751S in SO 8 package, manufactured in ST Shenzhen (China) will be JEDEC- MSL3 compliant. |
| Change Product Identification                                 | New Finished Goods code and MSL3 shown on box labels  |
| Manufacturing Location(s)                                     |   |

## DOCUMENT APPROVAL

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## ATTACHMENT TO PCN IPG-IPC/14/8450

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### **WHAT:**

Reference is made to PCN IPD-IPC/12/7348 dated 31 July 2012 about "SO 08/14/16 Narrow BACK-END plant optimization in ST Shenzhen (China)".

As a consequence of this PCN, the products VIMIT10, VIPER12AS, VIPER22AS and VN751S assembled in SO 8 package with SHD frame and green resin, will be JEDEC-MSL3 compliant starting July, 2014.

### **WHY:**

Process standardization in accordance with JEDEC MSL 3 dry packing requirements.

### **HOW:**

See the attached report.

The change to MSL 3 will be identified by a new Finished Goods code and the MSL 3 classification stated on the box labels.

### **WHEN:**

The MSL 3 will be introduced at the beginning of July, 2014.  
Samples of the new products can be delivered upon request.

# Preliminary Reliability Evaluation Report

## Assembly change

| General Information               |                                  | Locations                         |                |
|-----------------------------------|----------------------------------|-----------------------------------|----------------|
| <b>Product Line</b>               | VNA4                             | <b>Wafer fab location</b>         | AMK6 6         |
| <b>Product Description</b>        | SMPS PRIMARY I.C, VIPER          | <b>Assembly plant location</b>    | SHENZHEN CHINA |
| <b>Finished Good Code</b>         | VIPER12AS\$8-E<br>VIPER12AS\$7-E | <b>Reliability plant location</b> | CATANIA        |
| <b>Product division</b>           | IND.& POWER CONV.                | <b>Reliability assessment</b>     | POSITIVE       |
| <b>Package</b>                    | SO 8                             |                                   |                |
| <b>Silicon process technology</b> | VIPOWER                          |                                   |                |
| <b>Raw Line Code :</b>            | UC07*VNA4XCB<br>UC07*VNA4X3B     |                                   |                |

## DOCUMENT HISTORY

| Version | Date       | Pages | Author     | Comment |
|---------|------------|-------|------------|---------|
| 1.0     | 10/04/2014 | 11    | A. Vilardo | -       |
|         |            |       |            |         |
|         |            |       |            |         |

Issued by **Antonio Vilardo**  
IPG Rel Dept.– APG Support

## TABLE OF CONTENTS

- 1 APPLICABLE AND REFERENCE DOCUMENTS**
- 2 TEST GLOSSARY**
- 3 RELIABILITY REPORT OVERVIEW**
  - 3.1 OBJECTIVES
  - 3.2 CONCLUSION
- 4 DEVICE CHARACTERISTICS**
  - 4.1 DEVICE DESCRIPTION
    - 4.1.1 *Generalities*
    - 4.1.2 *Pin connection*
    - 4.1.3 *Block diagram*
    - 4.1.4 *Package outline/Mechanical data*
  - 4.2 TRACEABILITY
- 5 TEST RESULTS SUMMARY**
  - 5.1 LOT INFORMATION
  - 5.2 TEST PLAN AND RESULTS SUMMARY
- 6 TEST DESCRIPTION**
  - 6.1 DIE AND PACKAGE TESTS DESCRIPTION

## 1 APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description   |
|--------------------|---|
| AEC-Q100           | Stress test qualification for integrated circuits         |
| SOP 2.6.11         | Project management for product development                |
| SOP 2.6.19         | Front-end technology platform development & qualification |
| SOP 2.6.2          | Internal change management                                |
| SOP 2.6.7          | Product maturity level                                    |
| SOP 2.6.9          | Package and process maturity management in Back End       |
| SOP 2.7.5          | Automotive products definition and status                 |
| 0061692            | Reliability tests and criteria for product qualification  |
| 8160601            | Internal reliability evaluation report template           |
| 8161393            | General specification for product development             |

## 2 TEST GLOSSARY

| TEST NAME | DESCRIPTION                         | NOTE |
|-----------|-------------------------------------|------|
| PC (JL3): | Preconditioning (solder simulation) | 1    |
| AC:       | Autoclave at 2atm                   |      |
| HTSL:     | High Temperature Storage Life       |      |
| TC:       | Temperature Cycling                 |      |
| HTRB:     | High Temperature Reverse Bias Test  |      |

NOTE:

1) To be done before AC, TC, HTRB

## 3 RELIABILITY REPORT OVERVIEW

### 3.1 Objectives

Aim of this report is to present the preliminary results of the reliability evaluation performed on VNA4 device (VIPER12) due to assembly change with frame SHD and green resin.

It was also evaluated the change from MSL1 to MSL3.

VNA4 is processed in VIPOWER diffused in AMK6 and assembled in SO8 - in ST SHENZHEN -CHINA.

For the reliability evaluation the following tests were carried out:

AC, TC, HTSL, HTRB

In particular two different lots were used, one for AC, TC and HTSL tests ( R.L. UCO7\*VNA4XCB) and one for HTHB test (R.L. UCO7\*VNA4X3B)

Regarding HTRB test, samples of first lot were submitted only to 12h bake @ 125°C and IR reflow (1 times) 260°C; for second lot instead, half samples were submitted to standard ML3 flow and half samples only to 12h bake @ 125°C and IR reflow (1 times), without humidity treatment.

This choice has been taken to verify the behavior of the device with or without humidity insertion.

### 3.2 Conclusion

All reliability tests have been completed with positive at final electrical.

In particular, for HTRB, no differences to underline between samples for submitted to standard ML3 flow and the others not submitted to humidity treatment.

**On the ground of the overall positive results, from a reliability point of view, the new assembly with SHD frame and green resin with ML3 flow can be judged positively.**



## 4 DEVICE CHARACTERISTICS

### 4.1 Device description

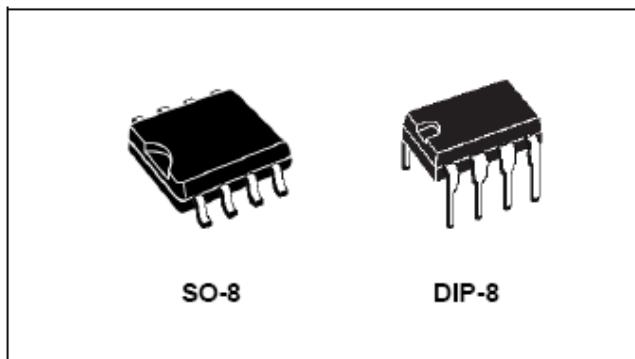
#### 4.1.1 Generalities

#### Features

- Fixed 60kHz Switching Frequency
- 9V to 38V Wide Range  $V_{DD}$  Voltage
- Current Mode Control
- Auxiliary Undervoltage Lockout with Hysteresis
- High Voltage Start-up Current Source
- Overtemperature, Overcurrent and Overvoltage Protection with Auto-Restart
- Typical power capability
  - European (195 - 265 Vac) 8W for SO-8, 13W for DIP-8
  - European (85 - 265 Vac) 5W for SO-8, 8W for DIP-8

#### Description

The VIPer12A combines a dedicated current mode PWM controller with a high voltage Power MOSFET on the same silicon chip.

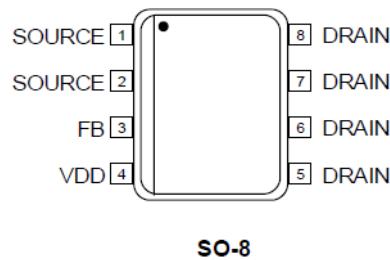


Typical applications cover off line power supplies for battery charger adapters, standby power supplies for TV or monitors, auxiliary supplies for motor control, etc.

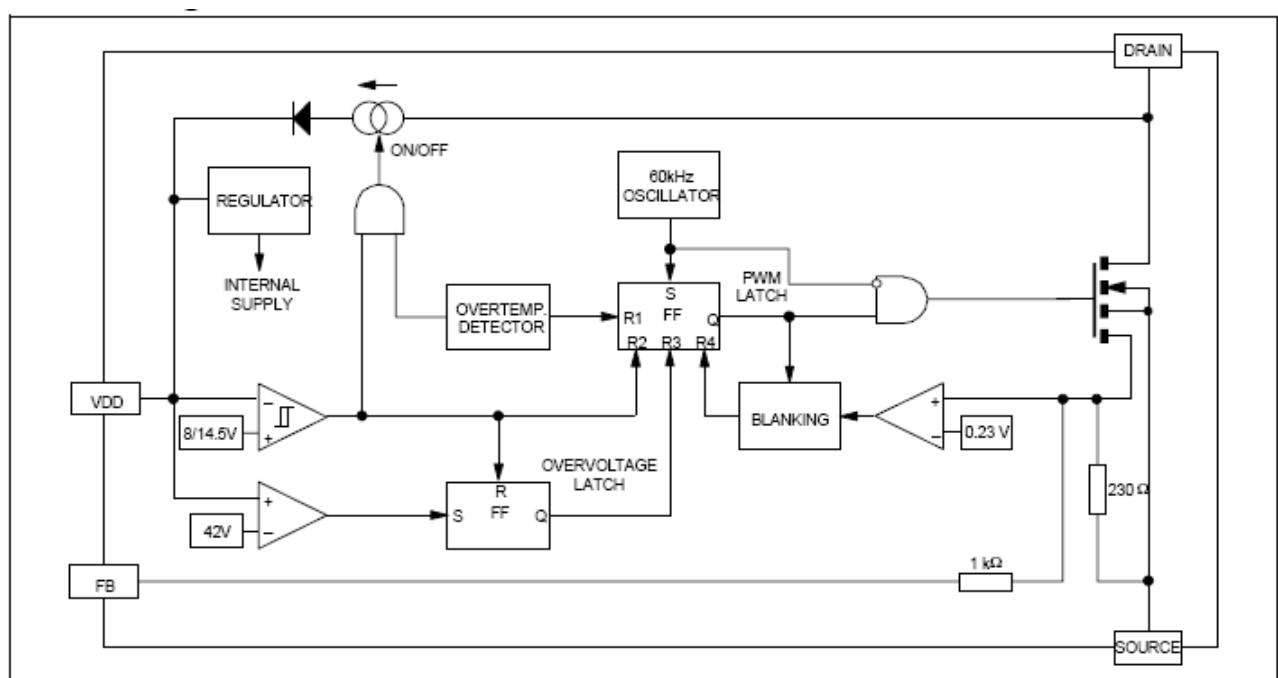
The internal control circuit offers the following benefits:

- Large input voltage range on the  $V_{DD}$  pin accommodates changes in auxiliary supply voltage. This feature is well adapted to battery charger adapter configurations.
- Automatic burst mode in low load condition.
- Overvoltage protection in HICCUP mode.

#### 4.1.2 Pin connection

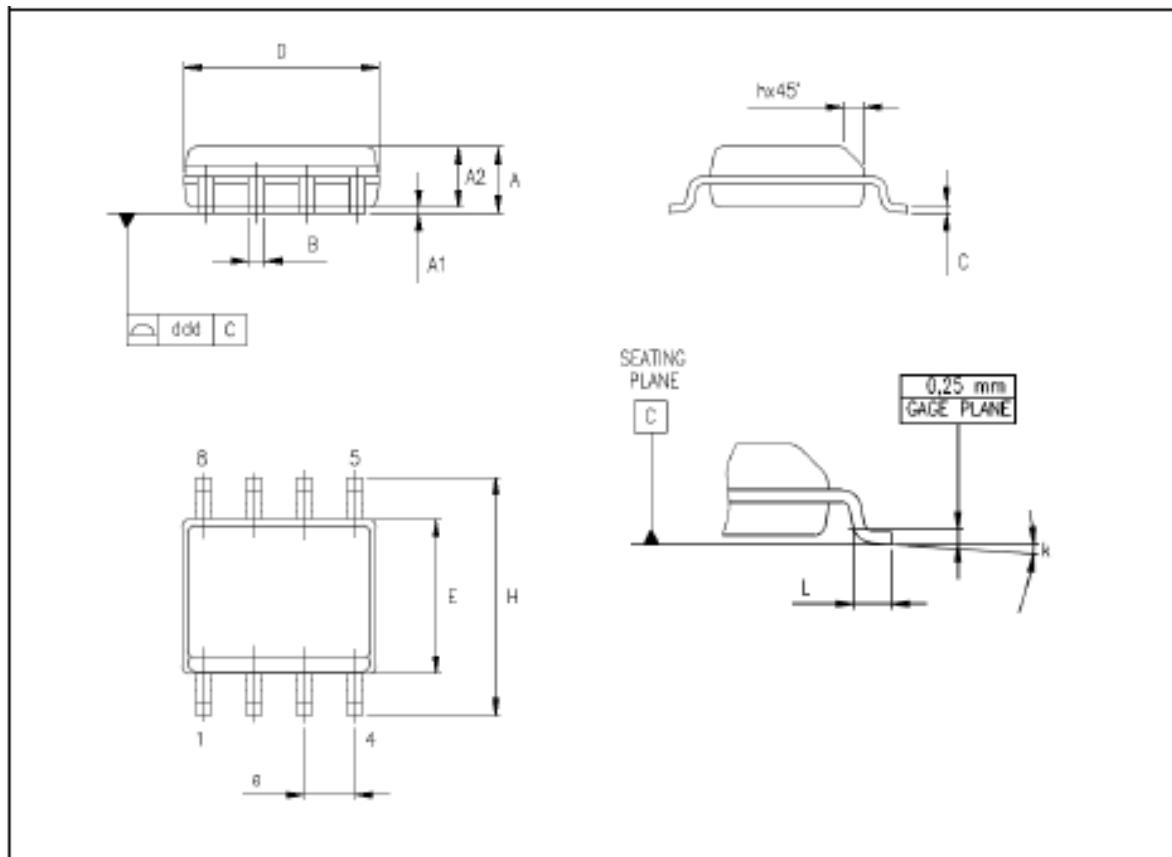


#### 4.1.3 Block diagram



## 4.1.4 Package outline/Mechanical data

| Ref. | Dimensions    |      |      |
|------|---------------|------|------|
|      | Databook (mm) |      |      |
|      | Nom.          | Min  | Max  |
| A    | 1.35          |      | 1.75 |
| A1   | 0.10          |      | 0.25 |
|      |               |      |      |
| A2   | 1.10          |      | 1.65 |
| B    | 0.33          |      | 0.51 |
| C    | 0.19          |      | 0.25 |
| D    | 4.80          |      | 5.00 |
| E    | 3.80          |      | 4.00 |
| e    |               | 1.27 |      |
| H    | 5.80          |      | 6.20 |
| h    | 0.25          |      | 0.50 |
| L    | 0.40          |      | 1.27 |
| k    | 8° (max.)     |      |      |
| ddd  |               |      | 0.1  |



## 4.2. Traceability

| Wafer fab information                   |                    |
|---|--------------------|
| <b>Wafer fab manufacturing location</b> | AMK6 6             |
| <b>Wafer diameter</b>                   | 6                  |
| <b>Silicon process technology</b>       | VIPOWER            |
| <b>Die finishing back side</b>          | Ti/Ni/Au           |
| <b>Die size</b>                         | 2800 x 2070 micron |
| <b>Passivation</b>                      | SiN                |
| <b>Metal levels</b>                     | 1                  |

| Assembly Information                     |                     |
|--|---------------------|
| <b>Assembly plant location</b>           | ST SHENZHEN -CHINA  |
| <b>Frame description</b>                 | SO 8L 98x160 SHD    |
| <b>Molding compound</b>                  | SUMITOMO G700KC     |
| <b>Wires bonding materials/diameters</b> | Au (1.3 mils)       |
| <b>Die attach material</b>               | GLUE ABLEBOND 8601S |

| Final Testing Information                        |                    |
|--|--------------------|
| <b>Electrical testing manufacturing location</b> | ST SHENZHEN -CHINA |

## 5 TESTS RESULTS SUMMARY

### 5.1 LOT Information

| Lot Nb | Diffusion Lot | Assy Lot   | Die Code |
|--------|---------------|------------|----------|
| 1      | 62307E8       | GK2451LE01 | CVNA4XCB |
| 2      | 3050231W      | GK4050RP01 | CVNA4X3B |

### 5.2 Test Plan and Results Summary

| N | Test      |      |  |        |                |                |       |
|---|-----------|------|--|--------|----------------|----------------|-------|
|   | TEST NAME | PREC | CONDITION/METHOD   | STEPS  | 1 LOT FAILS/SS | 2 LOT FAILS/SS | NOTES |
| 1 | PC (JL3)  | -    | JEDEC MSL = 3<br><br>24h bake @ 125°C<br>192hrs @ 30°C / 60% RH<br>IR reflow (3 times) 260°C<br><br>REFLOW PROFILE = Ecopack (Tmax=260°C)<br>LF<br><br>Reference specification = JEDEC J-STD-020 | FINAL  | 0/238          | 0/56           | *     |
| 2 | AC        | Y    | JEDEC MSL = 3<br><br>REFLOW PROFILE = Ecopack (Tmax=260°C)<br>LF<br><br>Ta = 121<br>Pressure (Atm) = 2<br><br>Reference specification = JESD22-A102  | 0 H    | 0/77           |                |       |
| 3 | TC        | Y    | JEDEC MSL = 3<br><br>REFLOW PROFILE = Ecopack (Tmax=260°C)<br>LF<br><br>Low Ta = -65<br>High Ta = 150<br><br>Reference specification = JESD22-A104   | 0 CY   | 0/77           |                |       |
|   |           |      |  | 100 CY | 0/77           |                |       |
|   |           |      |  | 200 CY | 0/77           |                |       |
|   |           |      |  | 500 CY | 0/77           |                |       |

\* 28 samples for each lot submitted only to 12h bake @ 125°C and IR reflow (1 times) 260°C

| N | Test      |      |   |        |                |                |       |    |
|---|-----------|------|---|--------|----------------|----------------|-------|----|
|   | TEST NAME | PREC | CONDITION/METHOD  | STEPS  | 1 LOT FAILS/SS | 2 LOT FAILS/SS | NOTES |    |
| 4 | HTSL      | N    | Ta = 150<br>Reference specification = JESD22-A103               | 0 H    | 0/77           |                |       |    |
|   |           |      |   | 168 H  | 0/77           |                |       |    |
|   |           |      |   | 500 H  | 0/77           |                |       |    |
|   |           |      |   | 1000 H | 0/77           |                |       |    |
| 5 | HTRB      | Y    | T <sub>j</sub> = 150°C<br>Reference specification = JESD22-A108 | 0 H    | 0/28           | 0/56           |       | ** |
|   |           |      |   | 168 H  | 0/28           | 0/56           |       |    |
|   |           |      |   | 500 H  | 0/28           |                |       |    |
|   |           |      |   | 1000 H | 0/28           |                |       |    |

\*\* samples of first lot and 28 samples of second lot submitted only to 12h bake @ 125°C and IR reflow (1 times)  
260°C

## 6 TESTS DESCRIPTION

### 6.1 Die and Package tests description

| TEST NAME  | DESCRIPTION  | PURPOSE  |
|--|--|--|
| <b>PC (JL3): Preconditioning (solder simulation)</b> | The device is submitted to a typical temperature profile used for surface mounting, after a controlled moisture absorption.  | As stand-alone test: to investigate the level of moisture sensitivity. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "popcorn" effect and delamination.             |
| <b>AC: Autoclave at 2atm</b>                         | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.   | To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.  |
| <b>HTSL: High Temperature Storage Life</b>           | The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.   | To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.  |
| <b>TC: Temperature Cycling</b>                       | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.  | To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die |
| <b>HTRB: High Temperature Reverse Bias Test</b>      | The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: -) low power dissipation; -) max. supply voltage compatible with diffusion process and internal circuitry limitations; | To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.   |



## Public Products List

PCN Title : VIMIT10, VIPER12AS, VIPER22AS and VN751S : Introduction of MSL3 (Moisture Sensitive Level)

PCN Reference : IPG-IPC/14/8450

PCN Created on : 28-APR-2014

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

### ST COMMERCIAL PRODUCT

VIPER12AS-E

VIPER22ASTR-E

VIPER12ASTR-E

VN751S

VIPER22AS-E

VN751STR

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