PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8430
Dated 06 May 2014

CMOS products changing wafer size from 5" to 6" in Ang Mo Kio fab (Singapore)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	29-Apr-2014
Forecasted availability date of samples for customer	29-Apr-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	29-Apr-2014
Estimated date of changed product first shipment	05-Aug-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached
Type of change	Waferfab process change
Reason for change	Capacity increase
Description of the change	We are going to change the wafer size from 5" to 6" of the product lines D310 and S131 in CMOS technology, in Ang Mo Kio fab (Singapore).
Change Product Identification	By a new Finished Goods code
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Arrigo, Domenico Massimo	Marketing Manager
Arrigo, Domenico Massimo	Product Manager
Moretti, Paolo	Q.A. Manager

ATTACHMENT TO PCN IPG-IPC/14/8430

WHAT*:*
After completing the wafer size change from 5” to 6” on the Bipolar products in Ang Mo Kio fab in Singapore (see PCN IPD-IPC/12/7320 Dated 13 Aug 2012), we are now also changing the CMOS products from 5” to 6” wafer size at the same location.

The involved products are the following:

Product line	Commercial Product
D310	TD310IN
	TD310ID (tube) TD310IDT (tape&reel)
S131	AVS1ACP08

WHY*:*
In order to optimize production and to increase capacity.

HOW*:*
As per the attached report.
A new internal part number (Finished Goods) will identify the 6” product.

WHEN*:*
Considering the positive results of the evaluations performed, the change from 5” to 6” can take effect immediately.

The samples of the D310 devices can be delivered upon request.
The AVS1ACP08 samples will be available in 4 weeks A.R.O.

Based on the material availability and the product version phase-out and phase-in, the first shipments of the new Finished Goods may happen earlier than the PCN terms stated herein.

Preliminary Reliability Report

CMOS C1PA TECHNOLOGY PRODUCTS WAFER SIZE CHANGE FROM 5” TO 6” in Ang Mo Kio fab, SINGAPORE

General Information	
Product Line	*D310*
Product division	*IPG- I&PC*
Package	*PDIP 16*
Silicon process technology	*CMOS (3µm) C1PA*

Locations	
Wafer fab location	*Ang Mo Kio*
Assembly plant location	*LONGGANG (China)*
Reliability assessment	*Pass*

General Information	
Product Line	*S131*
Product division	*IPG- I&PC*
Package	*PDIP 8*
Silicon process technology	*CMOS (3µm) C1PA*

Locations	
Wafer fab location	*Ang Mo Kio*
Assembly plant location	*LONGGANG (China)*
Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	9-April-2014		S. Regini	Original document

Issued by

Samantha Regini

Approved by

Paolo Moretti

TABLE OF CONTENTS

1. APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

2. QUALITY AND RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report describes all the evaluation activities and the results achieved in order to convert IPC division products in CMOS 3µm C1PA technology from 5" to 6" wafer size in Ang Mo Kio fab – Singapore. CMOS 3µm C1PA technology is already qualified in this fab.
The two products used for the qualification are:
- D310TAW assembled in PDIP 16 in LONGGANG (China).
- S131DAW assembled in PDIP 8 in LONGGANG (China).

The qualification activities include:

- Package-oriented reliability evaluation of D310TAW device diffused in AMK fab.
- Electrical characterization on D310TWA and S131DAW devices diffused in AMK fab.
- Electrical and parametric test result analysis of the two test vehicles.

According to Reliability Qualification Plan, below is the list of the trials performed:

Package Oriented Tests
- High Temperature Storage
- Autoclave
- Thermal Cycles

Electrical Characterization
- ESD resistance test
- LATCH-UP resistance test

2.2 Conclusion

Taking in account the results of the evaluations performed**, the wafer size of I&PC Division products in CMOS C1PA technology can be changed from 5" to 6" in AMK wafer fab - Singapore.**

3. DEVICE CHARACTERISTICS

3.1 Traceability

3.1.1 TV1 – D310TAW

Wafer fab information	
Wafer fab manufacturing location	*AMK - SINGAPORE*
Wafer diameter	*6 inches*
Wafer thickness	*375 µm ±25*
Silicon process technology	*CMOS (3um) C1PA*
Die finishing back side	*RAW SILICON*
Die size	*4400 x 1950 µm*
Bond pad metallization layers	*AlSi*
Die Finish Front	*P-VAPOX / NITRIDE*
Metal levels	*1*

Assembly Information	
Assembly plant location	*LONGGANG - CHINA*
Package description	*PDIP 16L*
Molding compound	*SAMSUNG SG-8300HXZ*
Wires bonding materials/diameters	*Au/1mils*
Die attach material	*LOCTITE ABLESTIK QMI168*
Lead solder material	*NiPdAu*

3.1.2 TV2 – S131DAW

Wafer fab information	
Wafer fab manufacturing location	*AMK - SINGAPORE*
Wafer diameter	*6 inches*
Wafer thickness	*375 µm ±25*
Silicon process technology	*CMOS (3um) C1PA*
Die finishing back side	*RAW SILICON*
Die size	*2210 x 2594 µm*
Bond pad metallization layers	*AlSi*
Die Finish Front	*P-VAPOX / NITRIDE*
Metal levels	*1*

Assembly Information	
Assembly plant location	*LONGGANG - CHINA*
Package description	*PDIP 8L*
Molding compound	*RESIN LOCTITE HYSOL GR360A-ST*
Wires bonding materials/diameters	*Au/1 mils*
Die attach material	*GLUE LOCTITE ABLESTIK 8390S25*
Lead solder material	*Sn*

4. RELIABILITY TESTS

4.1 Reliability test conditions and results

4.1.1 TV1 – D310TAW

Package Oriented Tests							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
AC	Autoclave						
	PC before	**121°C 2atm**	**0/77**			**96h**	
TC	Temperature Cycling						
	PC before	**Temp. range: -65/+150°C**	**0/77**			**500cy**	
HTSL	High Temperature Storage						
	No bias	**Tamb=150°C**	**0/77**			**500h**	
			x/77			**1000h**	**On going- Forecast w18 '14**

Electrical Characterization Tests							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
ESD	Electro Static Discharge						
	Human Body Model	**+/- 2kV**	**0/3**				
	Machine Model	**+/- 200V**	**0/3**				
	Charge Device Model	**+/- 750V**	**0/3**				
LU	Latch-Up						
	Over-voltage and Current Injection	**Tamb=85°C Jedec78**	**0/6**				

4.1.2 TV2 – S131DAW

Electrical Characterization Tests							
Test	Method	Conditions	Failure/SS			Duration	Note
			Lot 1	Lot 2	Lot 3		
ESD	Electro Static Discharge						
	Human Body Model	**+/- 2kV**	**x/3**				**Forecast w28 '14**
	Machine Model	**+/- 200V**	**x/3**				**Forecast w28 '14**
	Charge Device Model	**+/- 750V**	**x/3**				**Forecast w28 '14**
LU	Latch-Up						
	Over-voltage and Current Injection	**Tamb=85°C Jedec78**	**x/6**				**Forecast w28 '14**

5. RELIABILITY TESTS DESCRIPTION & DETAILED RESULTS

5.1 Package oriented tests

5.1.1 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 200 cycles.
- Final Testing @ 500 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -65°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.1.2 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (96hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 96 hrs

5.1.3 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2 Electrical Characterization Tests

5.2.1 Latch-up

This test is intended to verify the presence of bulk parasitic effects inducing latch-up.
The device is submitted to a direct current forced/sinked into the input/output pins. Removing the direct current no change in the supply current must be observed.

Stress applied:

condition	NEG. INJECTION	POS. INJECTION	OVERVOLTAGE
IN low: 0V	-100mA	Inom+100mA	100 mA + Inom or 1.5x Inom whichever is greather
IN high: 3V	-100mA	Inom+100mA	100 mA + Inom or 1.5x Inom whichever is greather

5.2.2 E.S.D.

This test is performed to verify adequate pin protection to electrostatic discharges.
The flow chart is the following:

- Initial testing @ Ta=25°C
- ESD discharging @ Ta=25°C
- Final Testing @ Ta=25°C

TEST CONDITIONS:

- **Human Body Model** — ANSI/ESDA/JEDEC STANDARD JES001
  CDF-AEC-Q100-002
- **Machine Model** — JEDEC STANDARD EIA/JESD-A115
  CDF-AEC-Q100-003
- **Charge Device Model** — ANSI/ESD STM 5.3.1 ESDA – JEDEC JESD22-C101
  CDF-AEC-Q100-011

6. PROCESS CHANGE CHARACTERIZATION

6.1 Parametric Test and EWS analysis

Parametric test distributions have been analyzed: no significant difference has been observed on any T84 critical parameter between CMOS C1PA products diffused on 6" and 5" wafer size in AMK fab.
EWS yield results and parametric distributions have also been analyzed comparing 6" and 5 " wafer size.
All the results are conforming to the expectations: no significant difference in EWS yield % and in the parametric distributions is highlighted.

Public Products List

PCN Title : CMOS products changing wafer size from 5" to 6" in Ang Mo Kio fab (Singapore)
PCN Reference : IPG-IPC/14/8430
PCN Created on : 30-APR-2014

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

TD310ID	TD310IDT	TD310IN

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