# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-PTS/14/8309
Dated 05 Feb 2014

## W023 Silicon Line housed in SO-8 : Transfer from AMK5 to AMK6 and Assy /Final Test from Muar to Shenzhen

## Table 1. Change Implementation Schedule

| | |
|---|---|
| Forecasted implementation date for change | 02-Jun-2014 |
| Forecasted availability date of samples for customer | 29-Jan-2014 |
| Forecasted date for **STMicroelectronics** change Qualification Plan results availability | 29-Jan-2014 |
| Estimated date of changed product first shipment | 02-Jun-2014 |

## Table 2. Change Identification

| | |
|---|---|
| Product Identification (Product Family/Commercial Product) | see list |
| Type of change | Waferfab location change |
| Reason for change | Optimization activity |
| Description of the change | W023 silicon line housed in SO8 package will be transferred from 5 inchs to 6 inchs in AngMoKio plant (AMK5 ->AMK6) and Assembly / Final Test from ST Muar (Malaysia) to ST Shenzhen (China) plant. |
| Change Product Identification | Dedicated Finished-Good Codes |
| Manufacturing Location(s) | |

# DOCUMENT APPROVAL

| Name | Function |
|---|---|
| Nicoloso, Riccardo | Marketing Manager |
| Liporace, Nicola | Product Manager |
| Minerva, Francesco | Q.A. Manager |

# W023 Silicon Line housed in SO-8 : Transfer from AMK5 to AMK6 and Assy /Final Test from Muar to Shenzhen

## WHAT:

W023 silicon line housed in SO8 package will be transferred from 5 inchs to 6 inchs in AngMoKio plant (AMK5 -> AMK6) and Assembly / Final Test from ST Muar (Malaysia) to ST Shenzhen (China) plant.

### SO8 Assembly Change Matrix from ST Muar to ST Shenzhen

| Item | SO-8 Muar | SO-8 Shenzhen |
|---|---|---|
| **Molding Compound** | NITTO MP8000CH4-2A | SUMITOMO EME-G700KC |
| **Die Attach** | GLUE ABLEBOND 8601S-25 | LOCTITE ABLESTIK 8601S-25 |
| **Wires** | Au 1 mils | Au 1 mils |
| **Lead-plating** | PPF (Ni/Pd/Au) | uPPF (Ni/Pd/Ag-Au) |
| **Lead-plating thic.** | 40/2/0.2 mils | 20/0.5/0.8 mils |

## WHY:

Optimization Strategy

## WHO:

All the Customers that are using the W023 silicon line housed in SO-8 package.

## WHEN:

Tentative date of change is June 2014.
Sample available on request
Qualification report included to this PCN (RR005213CT2235).

## WHERE:

ST AMK5, AMK6 – ST Muar (Malaysia), ST Shenzhen (China)

# L4949ED-E (W023)

# BIPOLAR technology transfer from ST AMK5 to ST AMK6

# SO8 Assembly transfer from ST Muar to ST Shenzhen

| General Information | |
|---|---|
| **Commercial Product** | L4949ED-E |
| **Product Line** | W023 |
| **Silicon process technology** | BIP |
| **Package** | SO8 |

| Revision history | | | |
|---|---|---|---|
| **Rev.** | **Date of Release** | **Author** | **Changes description** |
| 0.1 | December 9th 2013 | F. Ceraulo - APG Q&R Catania | Creation |

## Table of contents

# - 1. Reliability evaluations overview

## 1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on **L4949ED-E** (W023 as ST internal silicon line) in order to qualify both a technology and an assembly processes transfer:

1) Diffusion FAB transfer from ST AMK5 Ang Mo Kio (Singapore) 5” wafer fab to ST AMK6 Ang Mo Kio (Singapore) 6” wafer fab;
2) SO8 Assembly site transfer from ST Muar (Malaysia) to ST Shenzhen (China).

This product is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions as power-on reset and input voltage sense for Automotive Application designed in BIPOLAR technology.

The qualification was done according to **AEC_Q100 Rev.G** specification following the path described here below:

| Test group as per **AEC-Q100 Rev.G** | | Performed (Y/N) | Comment |
|---|---|---|---|
| A | Accelerated Environment Stress | Y | |
| B | Accelerated Lifetime Simulation | Y | |
| C | Package Assembly Integrity | Y | |
| D | Die Fabrication Reliability | N | Not Applicable for BIPOLAR technology |
| E | Electrical Verification | Y | |
| F | Defect Screening | N | To be implemented starting from first production lot |
| G | Cavity Package Integrity | N | N/A: not for plastic packaged devices |

See details per each test group in section 4 of this report.

NOTE: the package oriented tests were done using lots with different assembly configurations both in terms of Bonding Force and Ultra-Sonic Power. 3 lots nominal (NN), 6 lots worst cases (HH: Highest Bonding Force and Highest US Power, LL: Lower Bonding Force and Lower US Power)

## 1.2 Results

All reliability tests have been completed with positive results neither functional nor parametric rejects were detected at final electrical testing.

**Based on the overall positive results we consider the products qualified from a reliability point of view.**

# - 2. Traceability

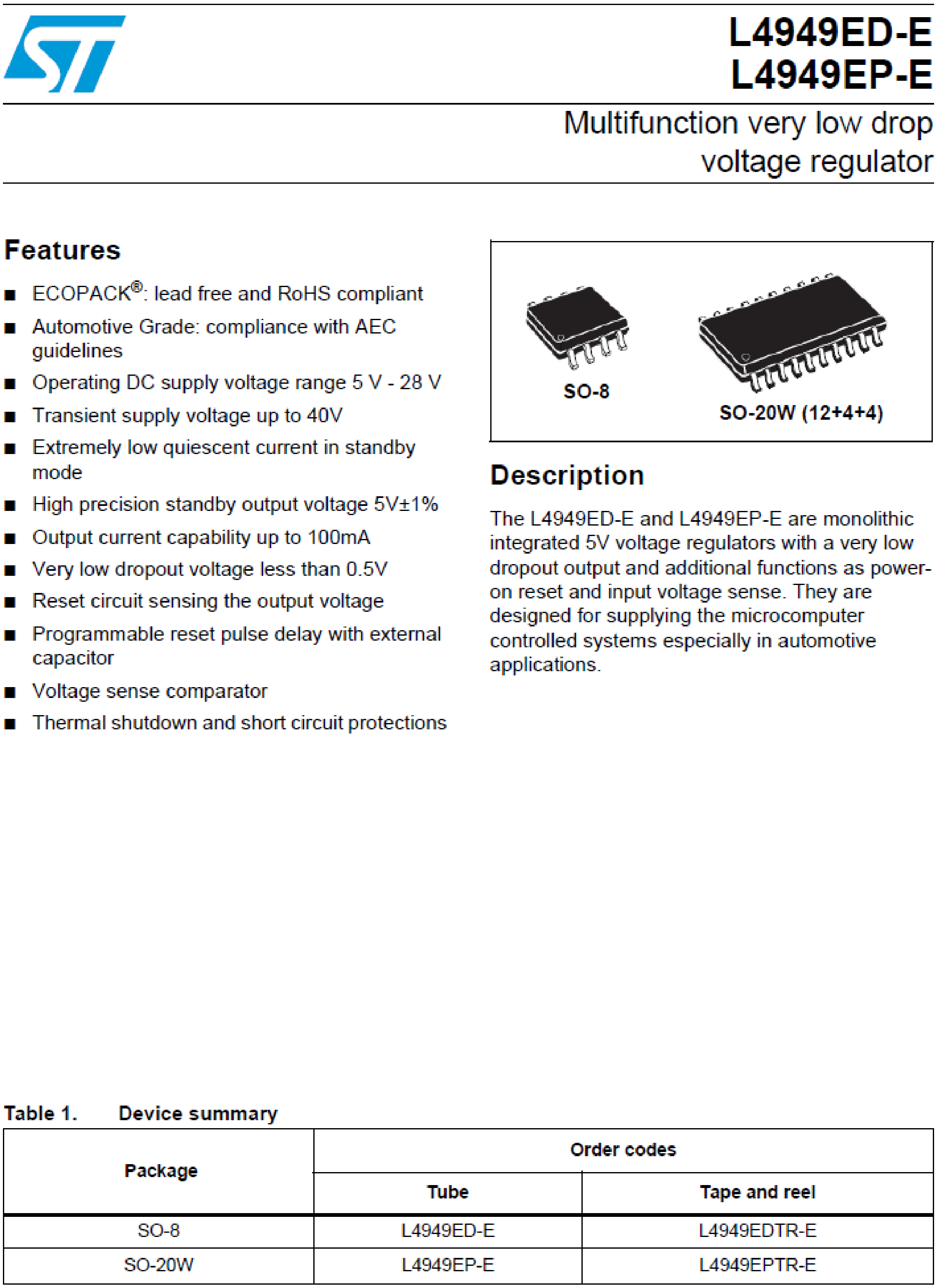
| Wafer fab information | |
|---|---|
| **Wafer fab manufacturing location** | ST AMK6 Ang Mo Kio (Singapore) |
| **Wafer diameter (inches)** | 6 |
| **Silicon process technology** | BIP |
| **Die finishing back side** | CHROMIUM/NICKEL |
| **Die size (micron)** | 2160 x 1960 |
| **Metal levels / materials** | 2 levels / AlSiCu (1.2 µm last level) |
| **Die finishing front side** | SiN / Polyimide |
| **Diffusion Lots #** | Lot 1: 6222KTF, Lot 2: 62302LE, Lot 3: 62302LF |

| Assembly Information | |
|---|---|
| **Assembly plant location** | ST Shenzhen (China) |
| **Package description** | SO8 |
| **Molding compound** | SUMITOMO EME-G700KC |
| **Wires bonding materials/diameters** | Au 1.0mils |
| **Die attach material** | GLUE ABLEBOND 8601S-25 |
| **Assembly Lots #** | Lot1: 993050PU01(NN), 993050PURR(HH), 993050PURQ(LL),<br>Lot2: 993050Q001(NN), 993050Q0RR(HH), 993050Q0RQ(LL),<br>Lot3: 993050PW01(NN), 993050PWRR(HH), 993050PWRQ(LL),<br>NOTE: the reliability evaluation was done on lots with different assembly configurations both in terms of Bonding Force and Ultra-Sonic Power. 3 lots nominal (NN), 6 lots worst cases (HH: Highest Bonding Force and Highest US Power, LL: Lower Bonding Force and Lower US Power) |

| Reliability Information | |
|---|---|
| **Reliability test execution location** | STM Catania (Italy) |

# - 3. Devices characteristics

## 3.1 Generalities



# L4949ED-E
# L4949EP-E

## Multifunction very low drop voltage regulator

### Features

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Operating DC supply voltage range 5 V - 28 V
- Transient supply voltage up to 40V
- Extremely low quiescent current in standby mode
- High precision standby output voltage 5V±1%
- Output current capability up to 100mA
- Very low dropout voltage less than 0.5V
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Voltage sense comparator
- Thermal shutdown and short circuit protections

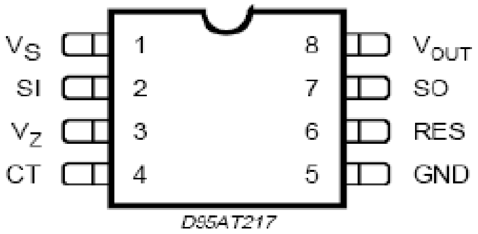
### Description

The L4949ED-E and L4949EP-E are monolithic integrated 5V voltage regulators with a very low dropout output and additional functions as power-on reset and input voltage sense. They are designed for supplying the microcomputer controlled systems especially in automotive applications.

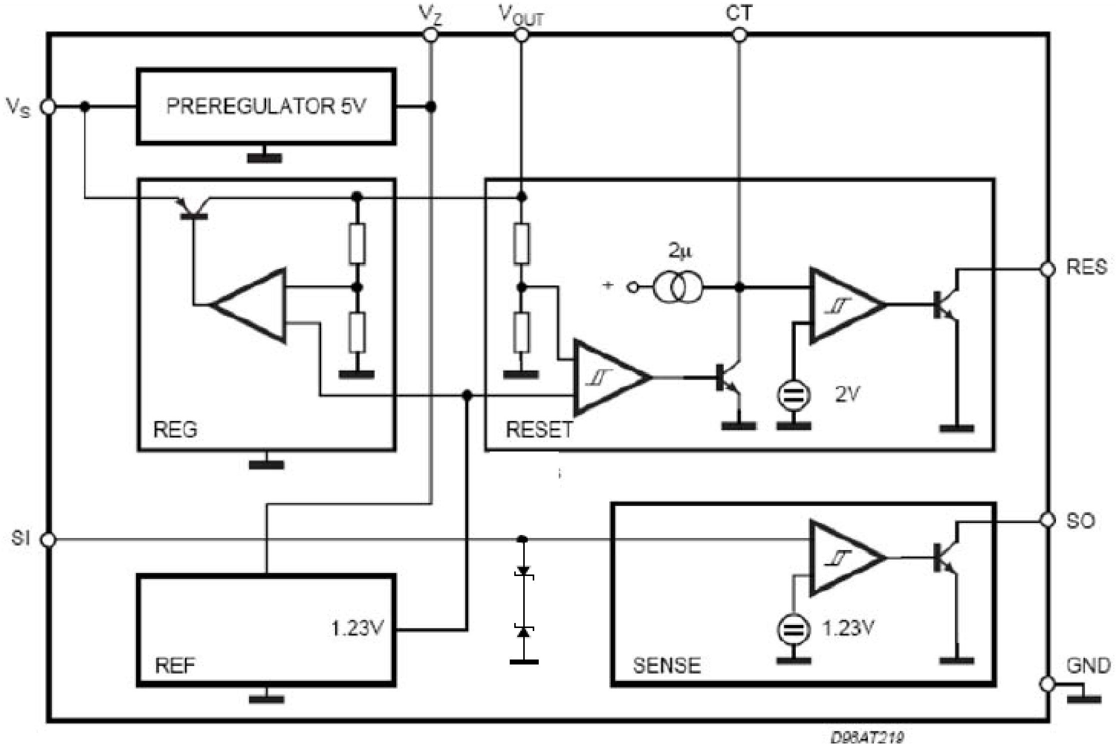
**Table 1. Device summary**

| Package | Order codes | |
|---|---|---|
| | Tube | Tape and reel |
| SO-8 | L4949ED-E | L4949EDTR-E |
| SO-20W | L4949EP-E | L4949EPTR-E |

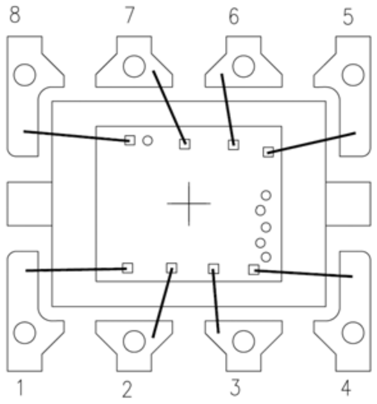
## 3.2 Pins connection



## 3.3 Blocks diagram



## 3.4 Bonding diagram



# - 4. Reliability qualification plan and results

| Test group A: Accelerated Environment Stress | | | | | |
|---|---|---|---|---|---|
| **AEC #** | **Test Name** | **STM Test Conditions** | **Sample Size/ Lots** | **Results Fails/SS/Lots** | **Comments** |
| **A1** | **PC**<br>Pre Cond | - Preconditioning according to Jedec JESD22-A113F including 5 Temperature Cycling Ta=-40ºC/+60ºC<br>- Reflow according to level 3 Jedec JSTD020D-1<br>- 100 Temperature Cycling Ta=-50ºC/+150ºC | Before THB, AC, TC, HTOL | | |
| **A2** | **THB**<br>Temp Humidity Bias | Ta=85ºC, RH=85%, Vcc=24V for 1000 hours | 77/3 | 0/77/3 | |
| **A3** | **AC**<br>Autoclave | **ENV. SEQ.** Enviromental Sequence<br>**TC** (Ta=-65ºC / +150ºC for 100 cycles) +<br>**AC** (Ta=121ºC, Pa=2atm for 96 hours) | 77/9 | 0/77/9 | |
| **A4** | **TC**<br>Temp. Cycling | Ta=-65ºC / +150ºC for 500 cycles | 77/9 | 0/77/9 | |
| **A5** | **PTC**<br>Power Temp. Cycling | Ta=-40ºC / +125ºC for 1000 cycles. | - | - | Not Applicable Pdis<1W |
| **A6** | **HTSL**<br>High Temp. Storage Life | Ta=150ºC for 1000 hours. | 45/9 | 0/45/9 | |

| Test group B: Accelerated Lifetime Simulation | | | | | |
|---|---|---|---|---|---|
| **AEC #** | **Test Name** | **STM Test Conditions** | **Sample Size/ Lots** | **Results Fails/SS/Lots** | **Comments** |
| **B1** | **HTOL**<br>High Temp. Op. Life | Bias Dynamic stress (JESD22-A108): Ta=125ºC, Vcc=28V for 1000 hours | 77/3 | 0/77/3 | |
| **B2** | **ELFR**<br>Early Life Failure Rate | Parts submitted to **HTOL** per JESD22-A108 requirements; GRADE 1: 24 hours at 150ºC | 800/3 | Passed | |
| **B3** | **EDR**<br>Endurance Data Retention | Only for memory devices | - | - | Not Applicable |

## Test group C: Package Assembly Integrity

| AEC # | Test Name | STM Test Conditions | Sample Size/ Lots | Results Fails/SS/Lots | Comments |
|---|---|---|---|---|---|
| **C1** | **WBS**<br>Wire Bond Shear | Per AEC-Q100-001 | 30 bonds /minimum 5 units/1 lot | All measurement within spec limits | |
| **C2** | **WBP**<br>Wire Bond Pull | Per MIL-STD883, M2011 Condition C or D | 30 bonds /minimum 5 units/1 lot | All measurement within spec limits | |
| **C3** | **SD**<br>Solderability | | 15/3 | All measurement within spec limits | |
| **C4** | **PD**<br>Physical Dimensions | | 10/3 | All measurement within spec limits | |
| **C5** | **SBS**<br>Solder Ball Shear | Only for BGA package | - | - | Not Applicable |
| **C6** | **LI**<br>Lead Integrity | Not required for Surface Mount Devices | - | - | Not Applicable |

## Test group D: Die Fabrication Reliability

| AEC # | Test Name | STM Test Conditions | Sample Size/ Lots | Results Fails/SS/Lots | Comments |
|---|---|---|---|---|---|
| **D1** | **EM**<br>Electromigration | | | | Not Applicable for BIPOLAR technology |
| **D2** | **TDDB**<br>Time Dependent Dielectric Breakdown | | | | Not Applicable for BIPOLAR technology |
| **D3** | **HCI**<br>Hot Carrier Injection | | | | Not Applicable for BIPOLAR technology |
| **D4** | **NBTI**<br>Negative Bias Temperature Instability | | | | Not Applicable for BIPOLAR technology |
| **D5** | **SM**<br>Stress Migration | | | | Not Applicable for BIPOLAR technology |

## Test group E: Electrical Verification

| AEC # | Test Name | STM Test Conditions | Sample Size/ Lots | Results Fails/SS/Lots | Comments |
|---|---|---|---|---|---|
| **E2** | **ESD**<br>HBM | HBM=[R=1.5kΩ, C=150pF] | 1 lot | ±2.0kV | |
| **E3** | **ESD**<br>CDM | | 1 lot | ±500V<br>±750V (*Corner pins)* | |
| **E4** | **LU**<br>Latch-Up | Injection current : ±100mA<br>Over voltage: 1.5 x Vop max | 6/1 | Inj-L/Inj-H@125°C: ±100mA all pins<br>Inj+L/Inj+H@125°C: ±100mA all pins<br>OV: passed | |
| **E5** | **ED**<br>Electrical Distributions | | 30/3 | Done | |
| **E7** | **CHAR**<br>Characterization | | | - | Not Applicable for this qualification |
| **E8** | **GL**<br>Gate Leakage | | 6/1 | PASSED | |
| **E9** | **EMC**<br>Electromagnetic Compatibility | | - | - | Not Applicable for this qualification |
| **E10** | **SC**<br>Short Circuit Characterization | According to **AEC-Q100-012** | - | - | |

## Test group F: Defects Screening Tests

| AEC # | Test Name | STM Test Conditions | Sample Size/ Lots | Results Fails/SS/Lots | Comments |
|---|---|---|---|---|---|
| **F1** | **PAT**<br>Process Average Testing | | Not performed on qualification lots listed on traceability section of this report. To be implemented starting from first production lot | | |
| **F2** | **SBA**<br>Statistical Bin/Yield Analysis | | | | |

| Test group G: Cavity Package Integrity Tests | | | | | |
|---|---|---|---|---|---|
| **AEC #** | **Test Name** | **STM Test Conditions** | **Sample Size/ Lots** | **Results Fails/SS/Lots** | **Comments** |
| **G1** | **MS**<br>Mechanical Shock | Not applicable: not for plastic packaged devices | | | |
| **G2** | **VFV**<br>Variable Frequency Vibration | | | | |
| **G3** | **CA**<br>Constant Acceleration | | | | |
| **G4** | **GFL**<br>Gross/Fine Leak | | | | |
| **G5** | **DROP**<br>Package Drop | | | | |
| **G6** | **LT**<br>Lid Torque | | | | |
| **G7** | **DS**<br>Die Shear | | | | |
| **G8** | **IWV**<br>Internal Water Vapor | | | | |

# Public Products List

PCN Title : W023 Silicon Line housed in SO-8 : Transfer from AMK5 to AMK6 and Assy /Final Test from Muar to Shenzhen
PCN Reference : APG-PTS/14/8309
PCN Created on : 04-FEB-2014

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

## ST COMMERCIAL PRODUCT

L4949ED-E

L4949EDTR-E

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