PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-MID/13/7972
Dated 11 Jul 2013

Malta as Additional Assembly Location of LQFP-100 (14x14 mm) and LQFP-64 (10x10 mm) for Bolero and Pictus Families

Table 1. Change Implementation Schedule

Forecasted implementation date for change	30-Sep-2013
Forecasted availability date of samples for customer	04-Jul-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	04-Jul-2013
Estimated date of changed product first shipment	10-Oct-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see enclosed
Type of change	Assembly additional location
Reason for change	To simplify the Supply Chain and reduce cycle time for critical reference
Description of the change	Please be informed that Malta assembly location will be introduced as additional location of LQFP-100 (14x14mm) and LQFP-64 (10x10 mm) for Bolero and Pictus Families.
Change Product Identification	Marking of Assembly plant
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Conan-clement, Bertrand	Marketing Manager
Brambilla, Daniele Alfred	Product Manager
Mervic, Alberto	Q.A. Manager

PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-MID/13/7972

MALTA ADDITIONAL ASSEMBLY LOCATION OF LQFP-100 (14x14 mm) and LQFP-64 (10x10 mm) FOR BOLERO AND PICTUS FAMILIES

Reason for the change :

To increase manufacturing capacity and to simplify the Supply Chain and reduce cycle time for critical Reference

Type of change : Additional back-end Plant

How can the change be seen : Marking of country of assembly. The Commercial Product will not change as there is no impact on device functionality.

Impacted devices :
Bolero and Pictus families in LQFP-100 and LQFP-64: see list enclosed

Timing for change : LQFP-100 (14x14 mm) package is qualified and volume deliveries can start in Q3 2013. On LQFP-64 (10x10 mm) deliveries can start in Q3 2014

Documentation:

-Qualification report of LQFP-100 (14x14 mm) included in this communication (RR002412AG6050)

-LQFP-100 (14x14 mm) Package Qualification extension by similarity

-Qualification plan of LQFP-64 (10x10 mm) included

-Dual Source Manufacturing Strategy for SPC56.

M10 QUALIFICATION

RR002412AG6050

Rev. 2.0

PRODUCT

LEOPARD 1M

(SPC56EL60)

CUT 3.1

Process	Packages
CMOS-M10	LQFP144 20x20
Rousset 8''	LQFP100 14x14

Function

PTS

Issued by: **L. Cola**

Approved: **P. Zabberoni**

APG – Quality and Reliability - Digital Products

TABLE OF CONTENTS

Reliability Report

General Information	
Product Line	*FL6003*
Product Description	*Leopard 1M*
Commercial Product	*SPC56EL60*
Product Group	*APG*
Product division	*PTS*
Package	*LQFP144, LQFP100*
Silicon process Technology	*CMOCM10 6M*

Locations	
Wafer fab location	*Rousset 8*
Assembly plant location	*ST-Malta, ST-Muar*
Reliability assessment	**Qualified in accordance to AEC-Q100 revG**

Abstract

Aim of this document is to report the qualification activity results on Leopard 3.1. Product qualification is performed in accordance with AEC-Q100 standard, temperature grade 1 (-40°C to +125°C).

DOCUMENT HISTORY

Version	Date	Author	Comment
1.0	13/06/12	L. Cola	First candidate release.
1.1	28/06/12	L. Cola	Fixed Nomenclature for ESD levels and device
1.2	24/07/12	L. Cola	Fixed wrong report “Internal” classification, now “Confidential”
1.3	25/07/12	L. Cola	Added LQFP100 qualification with G700L resin
1.4	30/07/12	L. Cola	Added packages information
1.5	21/09/12	L. Cola	Added note on WBP test after TC
2.0	28/09/12	L.Cola	Added LQFP144 qualification with ULA resin

1 RELIABILITY EVALUATION OVERVIEW

1.1 Objectives

Aim of this document is to report the reliability trials results achieved on Leopard 1M cut 3.1 qualification exercise.

Leopard 1M is processed in R8-Rousset FAB using CMOS M10 (90 nm) technology and it is assembled in Malta-ST assy in LQFP144 package and in Muar-ST assy line in LQFP100 package.

Different package materials with respect to what is already qualified in M10 family are requested to be qualified on Leopard 1M for LQFP144 and LQFP100 packages:

- LQFP144: introduction of ULA resin for Safety requirements
- LQFP100: new frame pad size from 7.2x7.2 to 9x9, with or without ULA.

Thus dedicated package qualifications have been planned on this product.
Qualification of Leopard 1M done on LQFP144 package without ULA and new packages qualification were run in different time.

Leopard 1M embeds the FSL3 Flash module.

The qualification exercise of Leopard 1M in LQFP144 no ULA package is based on three diffusion lots of Cut 2.0 plus one lot of Cut 3.1 coming from Rousset R8: assy reports required on all the qualification lots.

Cut 3.1 is diffused to correct some bugs found on Cut 2.0 and will involve only minor metal fixes.

Cut 3.1 qualification is based on a similarity approach, thus only a reduced qualification has been applied.

Package qualification on LQFP100 pin with new frame is based on 3 Assy lots coming from two diffusion lots of Cut 2.0.

Package qualification on LQFP144 pin with ULA is based on 3 Assy lots coming from one diffusion lot of Cut 3.1.

Introduction of ULA resin in LQFP100 with new frame doesn't require qualification due to similarity approach with LQFP144 ULA qualification.

Rev 1.0 and Rev 1.1 of this document are related to qualification of Leopard 1M on LQFP144 package without ULA resin.

Rev 1.2, Rev 1.3 and Rev 1.4 of this document are related to qualification of Leopard 1M with LQFP100 package with new frame (no ULA resin) and LQFP144 without ULA resin.

Qualification of Leopard 1M in LQFP144 with ULA resin and LQFP100 new frame with ULA resin (similarity approach for ULA) has been added in revision 2.0 of this document.

The M10 (90nm technology) process is qualified in R8 Fab since 2009 and new optimized "Flow 2" has been qualified in Q1/2011.

The qualification exercise for this new product is in respect of Q100 revG.

1.2 Flash qualification:

AEC Q100 – 005 Rev C document stated that device shall be tested for Program/Erase Endurance Cycling using the minimum number of cycles (100K) stated in the applicable device specification. HTDR and HTOL trials have to be started after this preconditioning.

HTOL will be performed after a Program/Erase endurance Cycling of 1000Cycles. Effects of Program/Erase Endurance Cycling using the minimum number of cycles (100K) are covered by Read Disturb trials at 1000 and 10.000 cycles. These conditions are worse than those reported in AEC Q100 – 005 Rev C.

Data retention specification after 100K Write/Erase cycles has been released to 5years.

ECC is not used during qualification trials, but only for projection of reliability data.

The qualification exercise is in respect of Q100 rev G specification and it considers also added customers' requirements.

1.3 Conclusions

All qualification trials relative to LQFP144 and LQFP100 have been completed with positive results.

Leopard 1M Cut 3.1 in LQFP144 and LQFP100 can be fully qualified in accordance to AEC-Q100 Grade 1 Rev G. New ULA molding compound can be qualified on LQFP144 and, by similarity, also on LQFP100.

2 TRACEABILITY

2.1 Wafer fab information

DIE FEATURES		
Diffusion Site	:	Rousset R8
Wafer Diameter (inches)	:	8
Process Technology	:	CMOS-M10
Passivation	:	USG – Nit UV
Die finishing back side	:	Lapped Silicon

2.2 Package outline/Mechanical data

PACKAGE FEATURES			
		LQFP 144	LQFP 100
Package Description	:	*LQFP 144 20x20x1.4*	*LQFP 100 14x14x1.4*
Assembly Site	:	*ST KIRKOP – MALTA*	*ST KIRKOP – MALTA*
Die Attach material	:	GLUE ABLEBOND 3280T	*QMI9507-1A1 10cc/41g EFD Sy*
Molding non-ULA	:	SUMITOMO EME-G700L D14mm W3.7g (non ULA)	*SUMITOMO EME-G700LS D14mm W3.7g (non ULA)*
Molding ULA	:	SUMITOMO EME-G700SLS D14mm W3.7g (ULA)	*SUMITOMO EME-G700SLS D14mm W3.7g (ULA)*
Substrate/Leadframe	:	FRAME LQFP 144L 20x20 6x6 DS.1mmOpB RgAg	*FRAME LQFP 100L 14x14 9sq C7025 SpAg+L1*
Wires bonding materials/diameters	:	WIRE Au 2N GPG2 D0.9 BL9-13 sp2x2	*WIRE Au 2N GPG2 D0.9 BL9-13 sp2x2*

2.3 Final testing information:

PACKAGE FEATURES		
Electrical Testing manufacturing location	:	ST KIRKOP – MALTA
Tester	:	Teradyne J750

2.4 Lot Information:

Product	Lot #	Diffusion
Leopard 1M Cut 2.0	L1	G115911
	L2	G115946
	L3 (package)	G122987
	L4 (package)	G119960
Leopard 1M Cut 3.1	L1 (also package)	G138973

3 AEC-Q100 QUALIFICATION PLAN

3.1 Environmental stress tests

TEST GROUP A – ACCELLERATED ENVIRONMENTAL STRESS TEST							
AEC #	**Test**	**Q100 Test Condition**	**Actual Test Conditions**	**Test Temp.**	**Q100 Sample Size/Min Lots**	**Generic Data**	**Proposed Testing**
A1	**PC** Pre-Cond	JEDEC J-STD-020	24h bake @ 125℃ 192h @ 30℃/60%RH Reflow simulation (3times)	Room	All prior to AC, THB, TC, HTOL, HTDR	M10 Products qualifications	231/3 LQFP100 (new frame) 231/3 LQFP144 (ULA molding)
A2	**THB** Temp Humidity Bias	JESD22-A101/A110	Ta=85℃, 85%RH 500h, 1000h	Room & Hot	77/3	M10 Products qualifications	77/3 LQFP100 (new frame) 77/3 LQFP144 (ULA molding)
A3	**AC** Auto-clave	JESD22-A102/A118	P=2.08atm Ta=121℃, 96h	Room	77/3	M10 Products qualifications	77/3 LQFP100 (new frame) 77/3 LQFP144 (ULA molding)
A4	**TC** Temp. Cycling	JESD22-A104	Ta = -50/+150℃ 500, 1000 cycles	Room, Hot & Cold (1) (5)	77/3	M10 Products qualifications	77/3 LQFP100 (new frame) 77/3 LQFP144 (ULA molding)
A5	**PTC** Power Temperature Cycle	JESD22-A105		Room & Hot			Not Applicable
A6	**HTSL** High Temp. Storage Life	JESD22-A103		Room & Hot	77/1		77/3 LQFP100 (new frame) For LQFP144 see Flash Test

3.2 Lifetime stress tests

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TEST							
AEC #	**Test**	**Q100 Test Condition**	**Actual Test Conditions**	**End Point Requirements**	**Q100 Sample Size/Min Lots**	**Generic Data**	**Proposed Testing**
B1	**HTOL** High Temperature Operating Life	JESD22-A108	PC before trial; V=Vd+20%, Ta=125℃ 168h, 500h, 1000h	Room, Hot & Cold	77/3		77/3 Cut 2.0 (1000hrs) 77/1 Cut 3.1 (500hrs, *1000hrs monitor*)
B2	**ELFR** Early Life Failure Rate	AEC Q100-008	TA = 125℃ 48 hrs	Room, Hot & Cold			800 x 1
B3	**EDR** Endurance Data Retention Op. Life	AEC Q100-005					See Dedicated Flash Test

3.3 Package integrity tests

TEST GROUP C –PACKAGE ASSEMBLY INTEGRITY TESTS							
AEC #	**Test**	**Q100 Test Condition**	**Actual Test Conditions**	**End Point Requirements**	**Q100 Sample Size/Min Lots**	**Proposed Testing**	**Proposed Testing**
C1	**WBS** Wire Bond Shear	AEC Q100-001		Cpk>1.5 in SPC	30 Bonds x 5 Devices	Assy report	30 bonds from minimum 5 units from 1 lot
C2	**WBP** Wire Bond Pull	MIL-STD-883 – 2011		Cpk>1.33 Ppk>1.67 or 0 fail after TC	30 Bonds x 5 Devices	Assy report	30 bonds from minimum 5 units from 1 lot
C3	**SD** Solderability	JESD22-B102		> 95% solder Coverage	15/1	Assy report	15/1
C4	**PD** Physical Dimension	JESD22-B100/B108		Cpk > 1.5	10/3	Assy report	10/1
C5	**SBS** Solder Ball Shear	AEC Q100-010					Not Applicable
C6	**LI** Lead Integrity	JESD22-B105		No lead Breakage or finish cracks	5/1		Not Applicable

3.4 Die fabrication reliability tests

TEST GROUP D – DIE FABBRICATION RELIABILITY TEST						
AEC #	**Test**	**Actual Test Conditions**	**Test Temperature**	**Generic Data**	**Generic Data**	**Proposed Testing**
D1	**EM** Electromigration	3 J: 0.5 – 3.0E6 A/cm2	3 T: 270C – 350C	M10 Process Qualification	M10 Process Qualification	No
D2	**TDDB** Time Dependent Dielectric BV			M10 Process Qualification	M10 Process Qualification	No
D3	**HCI** Hot Carrier Injection	3 VD accelerated near operative range	Room Temperature	M10 Process Qualification	M10 Process Qualification	No
D4	**NBTI** Negative Bias Temperature Instability		VD accelerated near operative range		M10 Process Qualification	No
D5	**SM**				M10 Process Qualification	No

3.5 Electrical verification tests

TEST GROUP E – ELECTRICAL VERIFICATION TESTS							
AEC #	**Test**	**Q100 Test Condition**	**Actual Test Conditions**	**Test Temperature**	**Q100 Sample Size/Min Lots**	**Generic Data**	**Proposed Testing**
E1	**TEST**				All Units		
E2	**ESD MM/HBM** Electrostatic Discharge	AEC Q100-002/3	Human Body Model 2.0KV Machine Model 200V	Room & Hot	3 per V level per pin comb/1		3 units/V level per Model 1 lot per package Cut 2.0 and Cut 3.1
E3	**ESD CDM** Electrostatic Discharge	AEC Q100-011	Charge Device Model 500V, 750V on corner PIN	Room & Hot	3 per level		3 units/V level per Model 1 lot per package Cut 2.0 and Cut 3.1
E4	**LU** Latch-up	AEC Q100-004	Current Inj. + Overvoltage on power supply At Room & Hot	Room & Hot	6		6/1 Cut 2.0 and Cut 3.1
E5	**ED** Electrical Distributions	AEC Q100-009	Ppk >= 1.66	Room & Hot & Cold	30/3		30/3
E6	**FG** Fault Grading	AEC Q100-007					Yes
E7	**CHAR** Characterization	AEC Q003					Yes
E8	**GL** Electrothermally Induced Gate Leakage	AEC Q100-006		Room	6/1		No
E9	**EMC** Electromagnetic Compatibility	SAE J1752/3			1		Yes

3.6 Defect screening tests

TEST GROUP F – DEFECT SCREENING TEST							
AEC #	**Test**	**Q100 Test Condition**	**Actual Test Conditions**	**Test Temp.**	**Q100 Sample Size/Min Lots**	**Generic Data**	**Proposed Testing**
F1	**PAT** Process Average Testing	AEC Q001					Yes
F2	**SBA** Statistical Bin Yield Analysis	AEC Q002					Yes

3.7 Flash dedicated test

FLASH DEDICATED TEST						
N	**TEST NAME**	**CONDITIONS [SPEC]**	**SAMPLE SIZE X lot**	**DEFECTS ***	**TEST**	**NOTES**
1	HTDR	PC before trial; 1k cyc before trial, Ta=150℃, 168h, 500h, 1000h, 2000h	77x3 Cut 2.0	0	Before and After @ RT	3, 4
2	FET@ RT	Ta = 25℃ 100kcy	77x3 Cut 2.0	0	Before and After @ RT	3
	HTDR After FET @ RT	Ta=150℃ 168h + Vth Drift Analysis			Before and After @ RT	3
3	FET @ HT	Ta = 125℃ 10kcy	77x1 Cut 2.0	0	Before and After @ RT	3
	HTDR After FET @ HT	Ta=150℃ 168h + Vth Drift Analysis			Before and After @ RT	3
4	FET @ LT	Ta = -40℃ 10kcy	77x1 Cut 2.0	0	Before and After @ RT	3
	HTDR After FET @ LT	Ta=150℃ 168h + Vth Drift Analysis			Before and After @ RT	3

* *Defect* is any device rejected at the readout electrical testing or failing additional acceptance criteria according to the specified procedure.

Notes

1 with Scanning Acoustic Microscopy inspection at 500Cy and 1000Cy
2 after Jedec Level 3 preconditioning
3 with drift analysis on key parameters
4 0 defects is intended over 77 parts per lots. Cell level defectivity is computed after drift analysis and must be <1ppm with ECC ON.
5 With Wire Bond Pull test performed as per Package Assembly Integrity Test table on both LQFP100 and LQFP144.

4 RELIABILITY TESTS RESULTS SUMMARY

4.1 Device qualification in LQFP144 package (No ULA)

Test			Step	RESULTS		Notes
N	TEST NAME	CONDITIONS [SPEC]		Cut 2.0	Cut 3.1	
1.a	**ESD**	HBM = H2 (2kV)	**Final result**	**PASSED**	**PASSED**	
1.b	**ESD**	MM = M3 (200V)	**Final result**	**PASSED**	**PASSED**	
1.c	**ESD**	CDM = C3B (500V / 750V corner only)	**Final result**	**PASSED**	**PASSED**	
2.a	**LU**	Current Injection = Level B +/- 100 mA	**Final result**	**PASSED**	**PASSED**	
2.b	**LU**	Supply Voltage = Level B 1.5xVmax	**Final result**	**PASSED**	**PASSED**	

Test			Step	RESULTS				Notes
				Cut 2.0			Cut 3.1	
N	TEST NAME	CONDITIONS [SPEC]		LOT 1	LOT 2	LOT 3	LOT 1	
1	**HTOL** High Temp. Operating Life	1000 W/E cyc @125℃ done before trial, JESD22-A108	**0 hrs**	0/77	0/77	0/77	0/77	
			168 hrs	0/77	0/77	0/77	0/77	
			500 hrs	0/77	0/77	0/77	0/77	**PASSED Cut 2.0 and Cut 3.1**
			1000 hrs	0/77	0/77	0/77	0/77 (monitor)	**PASSED Cut 2.0**
2	**ELFR**	Ta=125ºC, +24hrs	**48hrs (24+24hrs)**	0/800				**PASSED: 0 fails between 24hrs and 48 hrs**
3	**HTDR** High Temp. Data Retention	1000 W/E cyc @125℃ done before trial, Ta=150℃, 1000hrs	**0 hrs**	0/77	0/77	0/77		
			168 hrs	0/77	0/77	0/77		
			500 hrs	0/77	0/77	0/77		
			1000 hrs	0/77	0/77	0/77		
			2000 hrs	0/77	0/77	0/77		**PASSED**
4.a	**FET@25℃**	Ta=25℃ 100k Write/Erase cyc	**10k cyc**	0/77	0/77	0/77		
			50k cyc	0/77	0/77	0/77		
			100k cyc	0/77	0/77	0/77		**PASSED**
4.b	**HTDR After FET**	Ta=150ºC, 168hrs	**168 hrs**	0/77	0/77	0/77		**PASSED**

Test			Step	RESULTS				Notes
				Cut 2.0			Cut 3.1	
N	TEST NAME	CONDITIONS [SPEC]		LOT 1	LOT 2	LOT 3	LOT 1	
5.a	FET@125℃	Ta=125℃ 100k Write/Erase cyc	10k cyc	0/77				
			50k cyc	0/77				
			100k cyc	0/77				PASSED
5.b	HTDR After FET	Ta=150ºC, 168hrs	168 hrs	0/77				PASSED
6.a	FET@-40℃	Ta=-40℃ 100k Write/Erase cyc	10k cyc	0/77				
			50k cyc	0/77				
			100k cyc	0/77				PASSED
6.b	HTDR After FET	Ta=150ºC, 168hrs	168 hrs	0/77				PASSED

4.2 Package qualification of LQFP100 New Frame, no ULA

Test			Step	RESULTS		Notes
N	TEST NAME	CONDITIONS [SPEC]		Cut 2.0	Cut 3.1	
1.a	**ESD**	HBM = H2 (2kV)	**Final result**	**PASSED**	**PASSED**	
1.b	**ESD**	MM = M3 (200V)	**Final result**	**PASSED**	**PASSED**	
1.c	**ESD**	CDM = C3B (500V / 750V corner only)	**Final result**	**PASSED**	**PASSED**	
2.a	**LU**	Current Injection = Level B +/- 100 mA	**Final result**	**PASSED**	**PASSED**	
2.b	**LU**	Supply Voltage = Level B 1.5xVmax	**Final result**	**PASSED**	**PASSED**	

Test			Step	RESULTS			Notes
N	TEST NAME	CONDITIONS [SPEC]		LOT 1	LOT 2	LOT 3	
1	**PC MSL 3**	24h bake @ 125℃ 192h @ 30℃/60%RH Reflow simulation 3 times, J-STD-020	**Pre**	0/231	0/231	0/231	
			Post	0/231	0/231	0/231	**PASSED**
2	**THB** Temperature Humidity Bias	Ta=85℃, 85%RH, JESD22-A101/A110	**0 hrs**	0/77	0/77	0/77	
			500 hrs	0/77	0/77	0/77	
			1000 hrs	0/77	0/77	0/77	**PASSED**
3	**AC** Autoclave	P=2.08atm Ta=121℃, JESD22-A102/A118	**0 hrs**	0/77	0/77	0/77	
			96 hrs	0/77	0/77	0/77	**PASSED**
4	**TC** Temperature Cycling	Ta=-50℃ /+150 ℃, (incl. SAM and WBP) JESD22-A104	**0 cyc**	0/77	0/77	0/77	
			500 cyc	0/77	0/77	0/77	
			1000 cyc	0/77	0/77	0/77	**PASSED**
5	**HTSL** High Temperature Storage Lifetime	Ta=150℃, JESD22-A103	**0 hrs**	0/77	0/77	0/77	
			500 hrs	0/77	0/77	0/77	
			1000 hrs	0/77	0/77	0/77	**PASSED**

4.3 Package qualification of LQFP144 New ULA molding

Test			Step	RESULTS	Notes
N	TEST NAME	CONDITIONS [SPEC]		Cut 3.1	
1.a	**ESD**	HBM = H2 (2kV)	**Final result**	**PASSED**	
1.b	**ESD**	MM = M3 (200V)	**Final result**	**PASSED**	
1.c	**ESD**	CDM = C3B (500V / 750V corner only)	**Final result**	**PASSED**	
2.a	**LU**	Current Injection = Level B +/- 100 mA	**Final result**	**PASSED**	
2.b	**LU**	Supply Voltage = Level B 1.5xVmax	**Final result**	**PASSED**	

Test			Step	RESULTS			Notes
N	TEST NAME	CONDITIONS [SPEC]		LOT 1	LOT 2	LOT 3	
1	**PC MSL 3**	24h bake @ 125℃ 192h @ 30℃/60%RH Reflow simulation 3 times, J-STD-020	**Pre**	0/231	0/231	0/231	
			Post	0/231	0/231	0/231	**PASSED**
2	**THB** Temperature Humidity Bias	Ta=85℃, 85%RH, JESD22-A101/A110	**0 hrs**	0/77	0/77	0/77	
			500 hrs	0/77	0/77	0/77	
			1000 hrs	0/77	0/77	0/77	**PASSED**
3	**AC** Autoclave	P=2.08atm Ta=121℃, JESD22-A102/A118	**0 hrs**	0/77	0/77	0/77	
			96 hrs	0/77	0/77	0/77	**PASSED**
4	**TC** Temperature Cycling	Ta=-50℃ /+150 ℃, (incl. SAM and WBP) JESD22-A104	**0 cyc**	0/77	0/77	0/77	
			500 cyc	0/77	0/77	0/77	
			1000 cyc	0/77	0/77	0/77	**PASSED**
5	**HTSL** High Temperature Storage Lifetime	Ta=150℃, JESD22-A103	**0 hrs**	0/77	0/77	0/77	
			500 hrs	0/77	0/77	0/77	
			1000 hrs	0/77	0/77	0/77	**PASSED**

LQFP-100 14x14 Package
Qualification extension by similarity

APG Q&R Digital

June 2013

life.augmented

ST Confidential

Similarity for Product Family

- Similarity rules to extend qualification to products belong to the same **product family** is define by a ST specification (ADCS 7028386).

- Hereafter are reported checks done, in line with ST specification, to extend package qualification LQFP-100 14x14, using FL60 microcontroller, to FP50,FB60 and FB64 (Bolero and Pictus) microcontrollers in Malta BE Site.

Product Family

- Based on the following FL60, FP50, FB60 and FB64 microcontrollers can be considered as a Family products:

- They have:
  - the same “Design System” (flow, methodology, tools, ….)
  - the same library (process basic element library or cells library)
  - the same design rules
  - the same assembly rules
  - the same silicon process
  - the wafer technological process and the plants where the process is used are qualified
  - the package used by the product and the plants where assembly is performed are qualified
  - any other manufacturing step (EWS, Final Testing, Burn In) process and locations are qualified

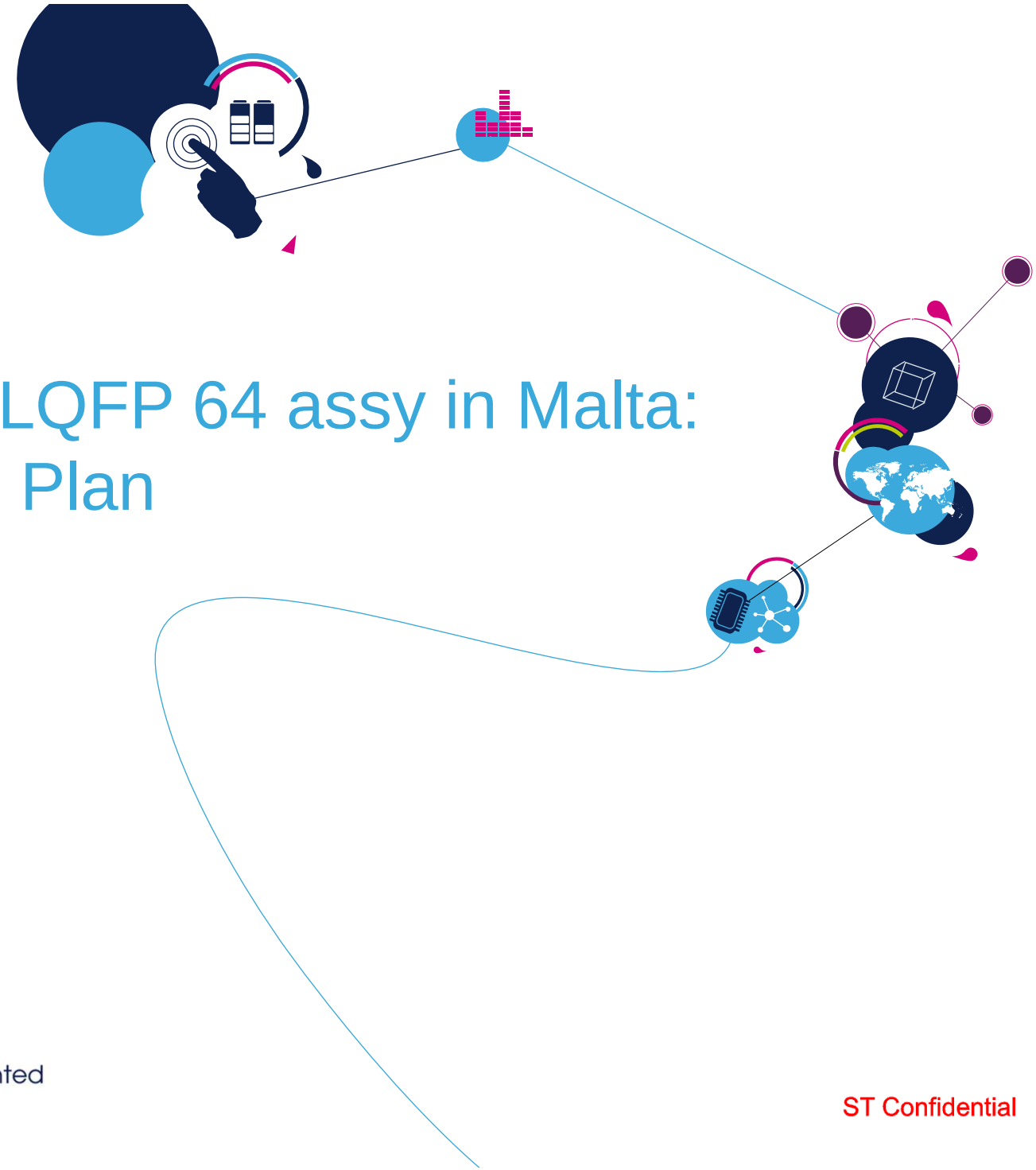
Similarity Criteria

- The device to be qualified uses the same (qualified) technological process and manufacturing plant than the test vehicle(s): **YES**
- The device to be qualified uses an already qualified package and assembly line : **YES**
- The device to be qualified uses the same design methodology than the test vehicle(s): **YES**
- The die area of the device to be qualified is equal/smaller than the die area of the test vehicle(s): **YES**
- The supply voltage of the device to be qualified is equal/lower than the supply voltage of the test vehicle(s) or equal/lower than the supply voltage of an already qualified product within the family: **YES**
- The power dissipation of the device to be qualified is equal/less than the power dissipation of the test: vehicle(s) or equal/less than the power dissipation of an already qualified product within the family: **YES**
- The load current of the device to be qualified is equal/lower than the load current of the test vehicle(s) or equal/lower than the load current of an already qualified product within the family: **YES**
- The operating temperature range of the device to be qualified is not different than the operating temperature range of the test vehicle(s) or not different from the operating temperature range of an already qualified product within the family: **YES**
- The device to be qualified uses the ESD protections qualified on test vehicle(s) or qualified on a product within the family: **YES**
- The device to be qualified uses all the guidelines for latch up prevention: **YES**
- The device to be qualified does not use critical functions or cells not previously included in test vehicle(s) or in an already qualified product within the family: **YES**
- The data sheet of the device to be qualified does not include specific customer requests as very low leakage currents, specific parameter stability in time or in temperature, immunity to specific external constraints, etc ..., not previously assessed with test vehicle(s) or with an already qualified device within the family: **YES**

- **Similarity criteria are met and package qualification by extension can be used.**

Conclusion

- FL60, FP50, FB60 and FB64 microcontrollers belong to the same Family products.
- Similarity criteria for package qualification by extension have been verified and met.
- LQFP-100 14x14 Package qualification in Malta using FL60 is extended to FP50, FB60 and FB64 microcontrollers.
- FL60 (Leopard) Package reliability report is included in PCN.



Pictus 256k LQFP 64 assy in Malta: Qualification Plan

M. De Tomasi

Wk 27 2013

life.augmented

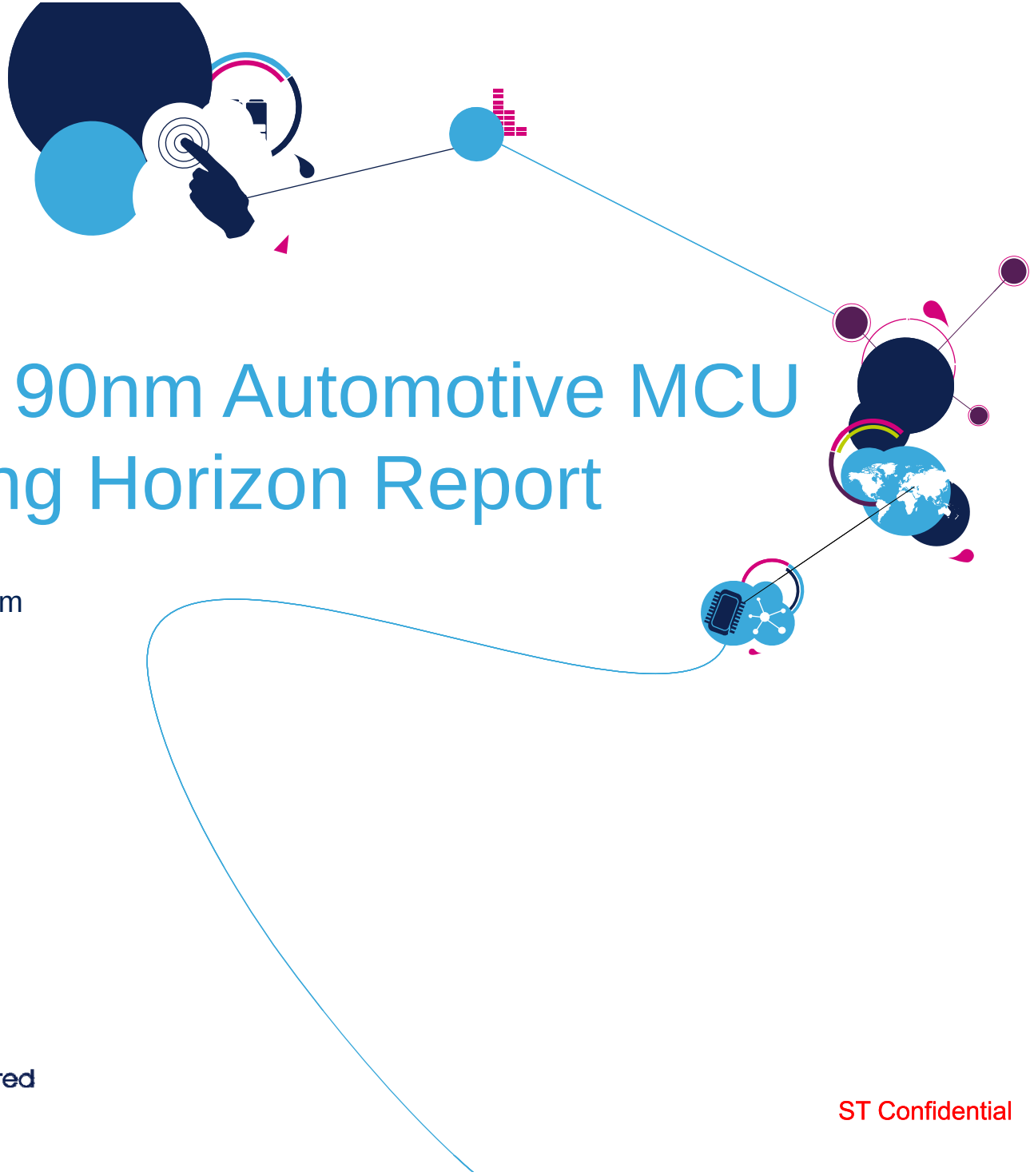
Introduction

- Pictus 256k LQFP 64 is now assembled in Muar and qualified
- Request is to qualify assy of LQFP64 also in Malta
- AEC – Q100 requires full package qualification in case of Assy plant transfer, no similarity allowed from original site
- No package similarity can be used with product already qualified in Malta

Qualification Trials

Trial	Conditions	Samples x Assy Lot
HTOL	1k cyc @ 125°C + 168hrs HTOL@125°C (1000hrs monitor)	77 x 1
ELFR	BI + 24hrs	800 x 1
TC	1000cyc -50°C/+150°C	77 x 3
AC	96h	77 x 3
THB	1000h 85°C/85%	77 x 3
HTS	1000hrs@150°C	77 x 1
CA	---	on 3 assy lots

- Assy report required on all qualification lots
- Additional trial: analysis of electrical distribution at FT



SPC56 M10 90nm Automotive MCU Manufacturing Horizon Report

Product Management Team

July 2013

Rev 1.1

life.augmented

ST 32-Bit Automotive MCU secured Supply Chain

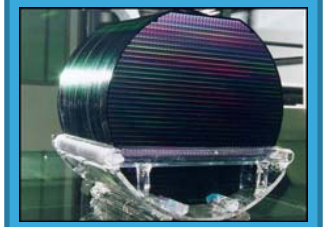
- Supply Chain model and Strategy
- Internal Front End Manufacturing sites
- Dual Sourcing strategy for M10 Process
- Internal Back End Manufacturing sites
- Dual Sourcing strategy for LQFP64 10x10mm and LQFP100 14x14mm

ST 32-Bit Automotive MCU secured Supply Chain model and Strategy

WAF

Business forecasting

WAFER MANUFACTURING



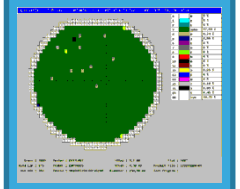
DUAL Source Strategy

90 nm:
- **Rousset 8''**
- **Crolles 12''**
- **Agrate 8'' (BEOL)**

55 nm:
- **Crolles 12''**
- **Foundry 12''**

40 nm:
- **Crolles 12''**
- **Foundry 12''**

EWS



Electrical Wafer Sort

DUAL Source:

- **Rousset 8''**
- **Agrate 8''**

Front End

DICE

Buffer Stock

ASSY

DUAL Source:

QFP Multi Sources:
- Malta
- Muar
- ASE (subcon)

BGA Dual Source:
- Muar
- ASE (subcon)

Final Test

Double Source:

- **Malta**
- **KYEC (subcon)**

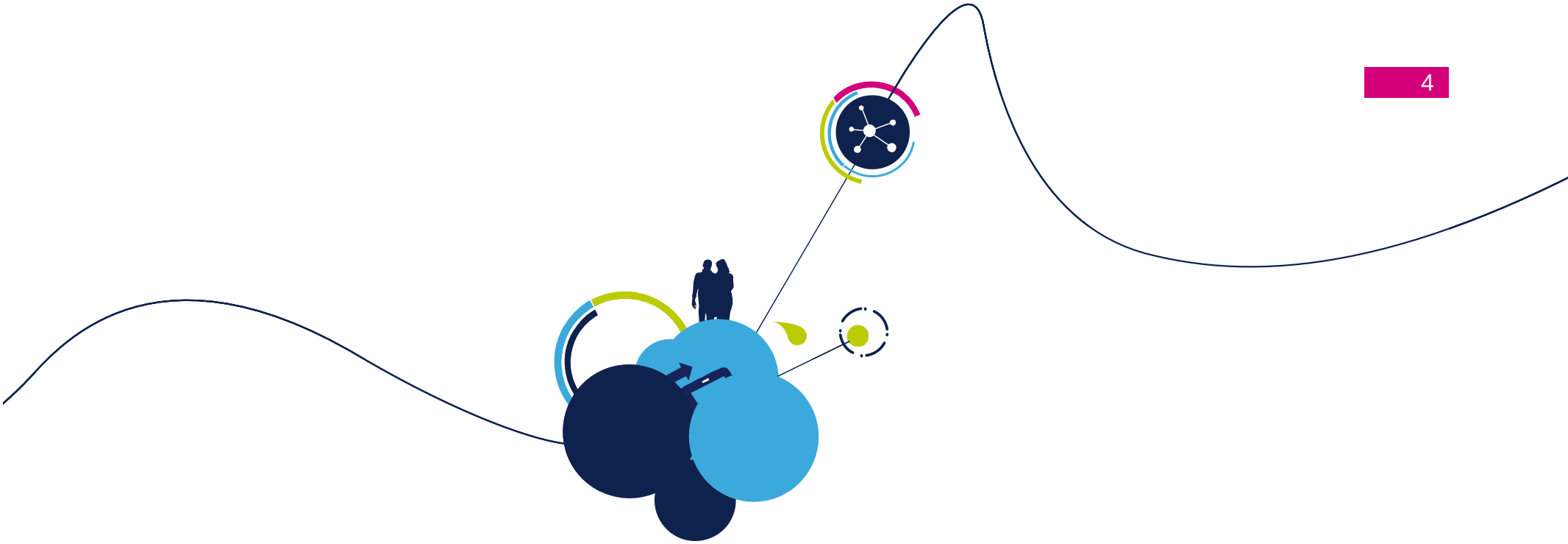
Back End

FG

Buffer stock

ST Manufacturing Strategy for 90nm SPC56 Automotive Microcontrollers is to implement dual source capabilities for Front-End and Back-End to support large volumes, improve flexibility and secure Customer business.

life.augmented



M10 Front End Dual Sourcing

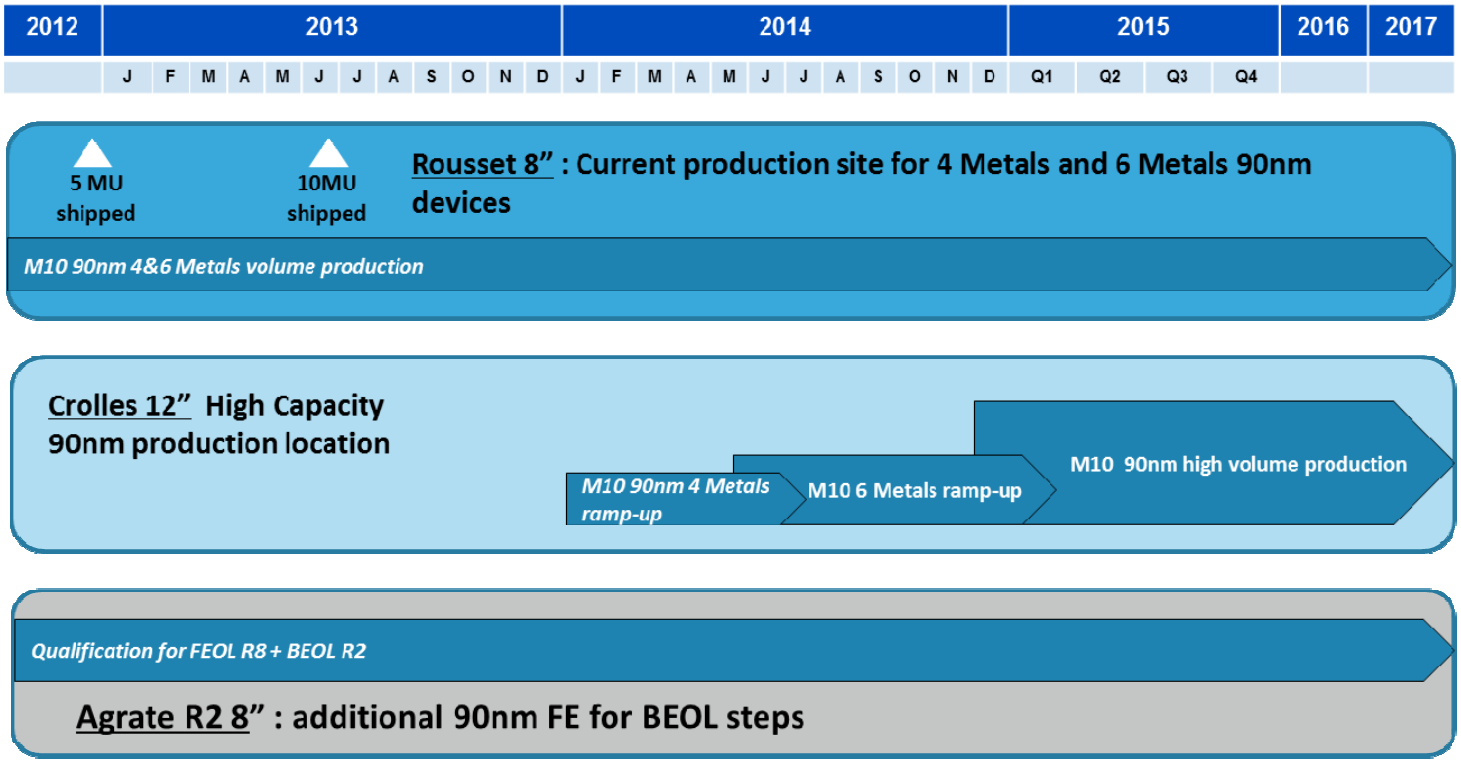
ST Automotive MCU
Internal FE Manufacturing sites

Rousset	Current	Potential
8” /200mm Capacity	7500 wafers/week Cu + Alu	6000 wafers/week full Cu
Product Start	CY2000	
Clean room	7300m²	9500m²
Investissement to date	$1.8 B	
Technologies in production	0.35µm to 90nm	65/55nm
Class	Mini environnement concept (class 1)	
Employees	2722 (total site, including EWS, Divisions and Support Functions)	

Crolles300	Current	Potential
12” /300mm Capacity	3500 wafers/week	4500 wafers/week
Product Start	CY2003	
Clean room	10000m²	
Investissement to date	$1.55 B	
Technologies in production	90nm down to 40nm	32nm down to 22nm
Class	Mini environnement concept (class 1)	
Employees	>5000 (total site, including contractors, partners, and R&D)	

life.augmented

SPC56 32-Bit M10 90 nm Front End Manufacturing Dual Source strategy

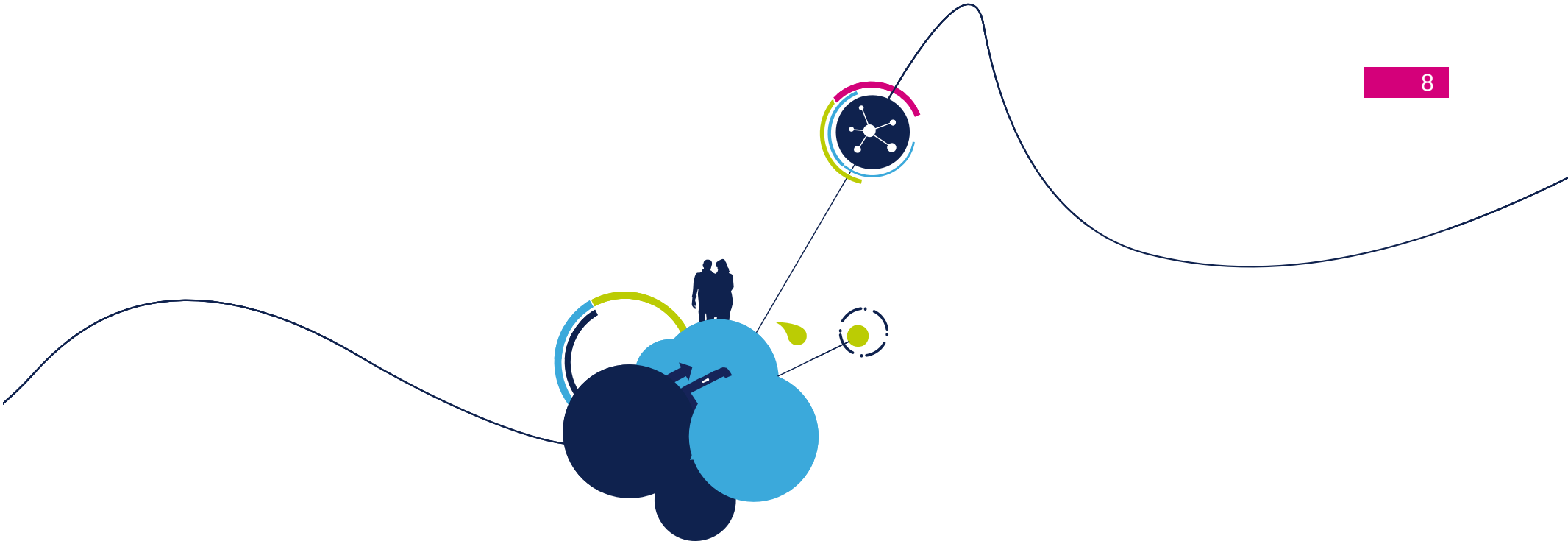


SPC56 M10 90nm Dual Source Front End strategy

- ST has successfully executed the first step of its manufacturing strategy: to industrialize and ramp-up SCP56 M10 family in ST Automotive MCU historical fab of Rousset 8” with excellent quality and service levels

- With the projected growth of 90nm production volumes over the period 2014-2017, and to secure Customer deliveries in case emergency situations, ST is now aggressively qualifying and ramping-up production in it high capacity Front End Crolles 12“ / CR300
  - Process has been enabled and qualified, First product is qualified and further products are completing AECQ100 qualification
  - PCN 7698 has been initiated
  - CR300 is one of the most advanced MCU Manufacturing plants at worldwide level, according to Customers and Car Makers, and there are clear benefits for Customers to use it as wafer source in terms of capacity and quality

- ST is now individually approaching its SPC56 Customers to define plans for qualifying Crolles as M10 90nm wafers source



M10 Back End Dual Sourcing

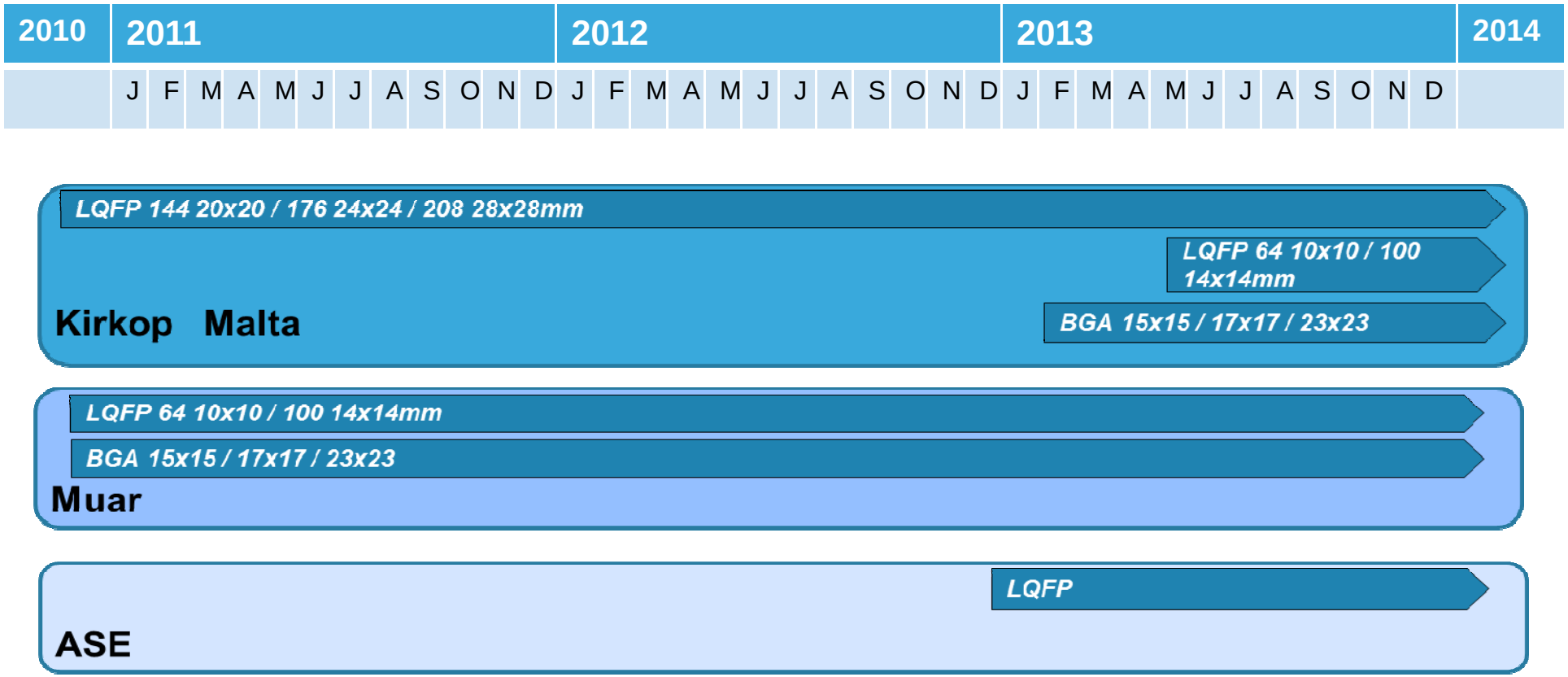
ST Automotive MCU
Internal Back End Manufacturing sites

Internal manufacturing

life.augmented

ST Confidential

SPC56 Assembly Manufacturing strategy



SPC56 LQFP
Dual Source Back End strategy

- ST has successfully executed the first step of its manufacturing strategy for assembly with the industrialization and ramp-up of SCP56 family in Malta and Muar

- With the projected growth of SPC56 production volumes over the period 2014-2017, and to secure Customer deliveries in case emergency situations, ST is now aggressively qualifying and ramping-up production of LQFP100 14x14 in Malta
  - Process has been qualified
  - ST will introduce Cupper/Palladium wires on some of its packages

- Additional requirements for LQFP64 10x10mm assembly capacity is foreseen at H2 2014 Horizon

- ST is now individually approaching its SPC56 Customers to define plans for qualifying Malta as assembly site for LQFP100 14x14mm

- ST will initiate the double sourcing of LQFP64 10x10mm in H1 2014

life.augmented

Public Products List

PCN Title : Malta as Additional Assembly Location of LQFP-100 (14x14 mm) and LQFP-64 (10x10 mm) for Bolero and Pictus Families
PCN Reference : APG-MID/13/7972
PCN Created on : 10-JUL-2013

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

SPC560B40L3B4E0X	SPC560B40L3B6E0X	SPC560B40L3B6E0Y
SPC560B40L3C4E0X	SPC560B40L3C6E0X	SPC560B50L1B4E0X
SPC560B50L3B4E0X	SPC560B50L3B6E0X	SPC560B50L3C4E0X
SPC560B50L3C6E0X	SPC560B50L3C6E0Y	SPC560B54L3B6E0X
SPC560B54L3C6E0X	SPC560B60L3C6E0X	SPC560B60L3C6E0Y
SPC560C40L3C6E0X	SPC560C50L3B4E0X	SPC560C50L3C6E0X
SPC560C50L3C6E0Y	SPC560D40L1C4E0Y	SPC560D40L3C4E0X
SPC560D40L3C4E0Y	SPC560P34L1BEAAR	SPC560P34L1BEAAY
SPC560P34L1BEABR	SPC560P34L1BEABY	SPC560P34L1CEFAR
SPC560P34L1CEFAY	SPC560P34L1CEFBR	SPC560P34L1CEFBY
SPC560P34L3BEAAR	SPC560P34L3BEAAY	SPC560P34L3BEABR
SPC560P34L3BEABY	SPC560P34L3CEFAR	SPC560P34L3CEFAY
SPC560P34L3CEFBR	SPC560P34L3CEFBY	SPC560P40L1BEAAR
SPC560P40L1BEAAY	SPC560P40L1BEABR	SPC560P40L1BEABY
SPC560P40L1BEFBR	SPC560P40L1BEFBY	SPC560P40L1CEFAR
SPC560P40L1CEFAY	SPC560P40L1CEFBR	SPC560P40L1CEFBY
SPC560P40L3BEAAR	SPC560P40L3BEAAY	SPC560P40L3BEABR
SPC560P40L3BEABY	SPC560P40L3BEFBR	SPC560P40L3BEFBY
SPC560P40L3CEFAR	SPC560P40L3CEFAY	SPC560P40L3CEFBR
SPC560P40L3CEFBY	SPC560P44L3BEAAR	SPC560P44L3BEAAY
SPC560P44L3CEABR	SPC560P44L3CEABY	SPC560P44L3CEFAR
SPC560P44L3CEFAY	SPC560P50L3B1ABR	SPC560P50L3B1ABY
SPC560P50L3BEABR	SPC560P50L3BEABY	SPC560P50L3BEFAR
SPC560P50L3BEFAY	SPC560P50L3CEFAR	SPC560P50L3CEFAY
SPC560P50L3CEFBR	SPC560P50L3CEFBY	

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries(‘‘ST’’) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND / OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS ‘‘AUTOMOTIVE GRADE’’ MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com