PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-AAS/13/7954
Dated 21 Jun 2013

TDA2003AV; TDA2030AH TRANSFER FROM AMK5 (5" wafers) TO AMK6 (6" wafers)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	14-Jun-2013
Forecasted availability date of samples for customer	15-Jul-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-Jul-2013
Estimated date of changed product first shipment	20-Sep-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	TDA2003A family
Type of change	Waferfab process change
Reason for change	To rationalize the production capacity.
Description of the change	the products TDA2003AV and TDA2003AH , diffused on bipolar LABT process, will be transferred from the AMK5 (5" wafers) production line to AMK6 (6" wafers) production line, both inside the Ang Mo Kyo (Singapore) site. Note: with the agreement of the customer, parts from 6" wafers can be delivered even in advance in respect of the scheduled date.
Change Product Identification	Finished Good code
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Ferri, Simone	Marketing Manager
Onetti, Andrea Mario	Product Manager
Speroni, Ernesto Fabrizio	Q.A. Manager

TDA2003AV; TDA2030AH TRANSFER FROM AMK5 (5” wafers) TO AMK6 (6” wafers)

WHAT

As part of the running program to convert to 6” wafers the silicon lines diffused on the bipolar processes in the Ang Mo Kio plant, the products TDA2003AV and TDA2003AH , diffused on bipolar LABT process, will be transferred from the AMK5 (5” wafers) production line to AMK6 (6” wafers) production line, both inside the Ang Mo Kyo (Singapore) site.

WHY

To rationalize the production capacity.

HOW

The bipolar diffusion process family is qualified and running in volumes on 6” wafers since 2003
The qualification has been done through test vehicles representative to the same bipolar process family (namely L203 and LX05) and actually trough a device belonging to the same silicon line (namely L540) .

Attached the qualification test plan with the updated results.

The alignment of electrical parameters of the impacted devices will be monitored as well.

Note: with the agreement of the customer, parts from 6” wafers can be delivered even in advance in respect of the scheduled date.

Reliability Evaluation Plan on
L540: wafer diameter change from 5' to 6"

LABT Technology – AMJ9 6"

LINE: L540
PACKAGE: PENTAWATT

			LOT 1 (FAIL/S.S.)	LOT 2 (FAIL/S.S.)	LOT 3 (FAIL/S.S.)		
Test	**Conditions**	**Extra**			**Leg LL**	**Leg NN**	**Leg HH**
HTOL	Tj=150°C, Vs=16V, 1000h	2000h	0/77 @ 2000h completed	-	-	-	-
HTB	Tj=150°C, Vs=18V, 1000h	-	0/77 @ 1000h completed	-	-	-	-
ESD HBM	±1kV, ±2kV	-	PASSED	-	-	-	-
ESD CDM	±500V, ±750V	-	PASSED	-	-	-	-
ELFR	Tj=150°C, Vs=16V, 24h	-	0/800 completed	0/800 completed	-	0/800 completed	-
TC	Ta=-50/+150°C, 1000c	2000c	-	-	0/77 @ 500Cy 0/77 @ 1000cy completed 2000Cy ongoing	0/77 @ 500Cy 0/77 @ 1000cy completed 2000Cy ongoing	0/77 @ 500Cy 0/77 @ 1000cy completed 2000Cy ongoing
HTSL	150°C, 1000h	2000h	-	-	0/77 @ 500h 0/77 @ 1000h completed 1500h ongoing	0/77 @ 500h 0/77 @ 1000h completed 1500h ongoing	

AC	96h, 2atm, 121°C	192h	-	-		0/77@ 96h 192h completed,	
			LOT 1 (FAIL/S.S.)	LOT 2 (FAIL/S.S.)	LOT 3 (FAIL/S.S.)		
Test	Conditions	Extra			Leg LL	Leg NN	Leg HH
THB	85°C, 85% V=16V, 1000h	2000h	-	-	1500H PASSED	1500H PASSED	
WBP	THB	-	-	-	@ 1000c		
CA	-	-	-	-		planned	

NOTE:
Updated on 2013 week22.

LAAT Technology – AMK 6”

LINE: L203
PACKAGE: PDIP 16L

Test	Conditions	-	RESULT (FAIL/S.S.)		NOTE
HTB	Tj=150°C, Vs=50V, 1000h	-	0/50 @ 1000h	-	Reliability report : REL-6333-173/077.03W

LAAT Technology – AMK 6”

LINE: LX05 (EW2)
PACKAGE: TO220

Test	Conditions	-	RESULT (FAIL/S.S.)	GENERIC DATA	NOTE
HTB	Tj=125°C, Vs=35V, 1000h	-	0/77 @ 1000h	0/385 (*)	Reliability report : T.R. 7.03/1150

(*) Generic data for all year 2003

TEST DESCRIPTION

TEST NAME	DESCRIPTION	PURPOSE
HTOL: High Temperature Operating Life	The device is stressed in dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature, load current, internal power dissipation.	To simulate the worst-case application stress conditions. The test is oriented to investigate typical IC failure modes like oxide faults and metal degradation and to check overall IC the parametric stability.
HTS: High Temperature Storage	The device is stored in unbiased condition at the maximum temperature allowed by the package materials, sometimes higher than the maximum operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
HTB: High Temperature Bias	The device is stressed in static biased configuration, approaching the operative max. absolute ratings in terms of junction temperature and supply voltage.	To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, and layout sensitivity to surface effects.
TC: Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding wire-bonds failure.
ESD (HBM): Electrostatic Discharge (Human Body Model)	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models.	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
ESD (CDM): Electrostatic Discharge (Charged Device Model)		
THB: Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions for ambient temperature and relative humidity.	To investigate failure mechanisms activated in the die-package environment by electrical field and wet conditions. It is mainly oriented to highlight typical failure mechanisms of IC in these conditions like electro-chemical corrosion.
LTS: Low Temperature Storage	The device is stored in unbiased condition at the min. temperature allowed by the package materials, sometimes lower than the min. op. temp.	To investigate the failure mechanisms activated by extremely cold conditions for prolonged time.

AC: Autoclave	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity. To point out critical water entry paths with consequent electrochemical and galvanic corrosion.

Public Products List

PCN Title : TDA2003AV; TDA2030AH TRANSFER FROM AMK5 (5" wafers) TO AMK6 (6" wafers)
PCN Reference : AMS-AAS/13/7954
PCN Created on : 26-JUN-2013

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

TDA2003AH	TDA2003AV

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