PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-PWR/13/7845
Dated 09 May 2013

Front-End Capacity Extension for Power Bipolar Transistors (Planar Technology) - Tours (France)

Table 1. Change Implementation Schedule

Forecasted implementation date for change	02-May-2013
Forecasted availability date of samples for customer	02-May-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	02-May-2013
Estimated date of changed product first shipment	08-Aug-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab additional location
Reason for change	optimize Power Bipolar Transistors productivity and Wafer FAB utilization
Description of the change	Following the continuous improvement of our service and in order to rationalize and optimize Power Bipolar Transistors productivity, this document is announcing that Power Bipolar Transistors (Planar Technology), currently manufactured in Ang Mo Kio (Singapore) Wafer FAB, will be produced again in the Tours (France) plant as in the past. Power Bipolar Transistors (Planar Technology) produced in Tours (France), guarantees the same quality and electrical characteristics as reported in the relevant data sheet. Devices used for qualification are available as Samples
Change Product Identification	"VU" as Wafer FAB production area code
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Please be informed that Power Bipolar Transistors (Planar Technology), currently manufactured in Ang Mo Kio (Singapore) Wafer FAB, will be also produced in Tours (France) plant.

The involved product series and affected Technologies are listed in the table below:

Product Family	Technology	Commercial Product / Series
Power Bipolar Transistors	Planar	See attached list

Any other product related to the above table, even if not expressly included or partially mentioned in the attached list, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 18-2013.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle
Power Bipolar Transistors	I²PAK DPAK SOT-32 TO-92	BULB128-1 STD13003T4 ST13003 STL73

Pilot Run Samples available upon request, starting from Week 23-2013:

BUL128, BUL128D-B, BUL38D, BUL49D, BULB49DT4, BULD118D-1, ST13003-K, ST13003-S, ST13005, STBV32, STBV32-AP, STBV32E-AP, STI13005-H, STK13003M, STL128D, STL128DFP, STL128DN, STL128DNFP, STLD128DNT4, STT13005D-K, STX13003, STX13003-AP, STX13003G, STX13003G-AP, STX13003M, TR236, T RD136DT4.

Change implementation schedule:

The first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power Bipolar Transistors	From Week 31-2013

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of Power Bipolar Transistors (Planar Technology), manufactured in Tours (France) plant, will be ensured by “VU" as Wafer FAB production area code printed on the box label.

Sincerely Yours.

TOURS vs. AMK

Contents

1. Parametric Verification on:

- **BVCEO;**
- **hfe;**
- **VCEsat;**

2. CPKs data.

LEGEND:

- Tours distribution on the left,
- AMK distribution on the right.

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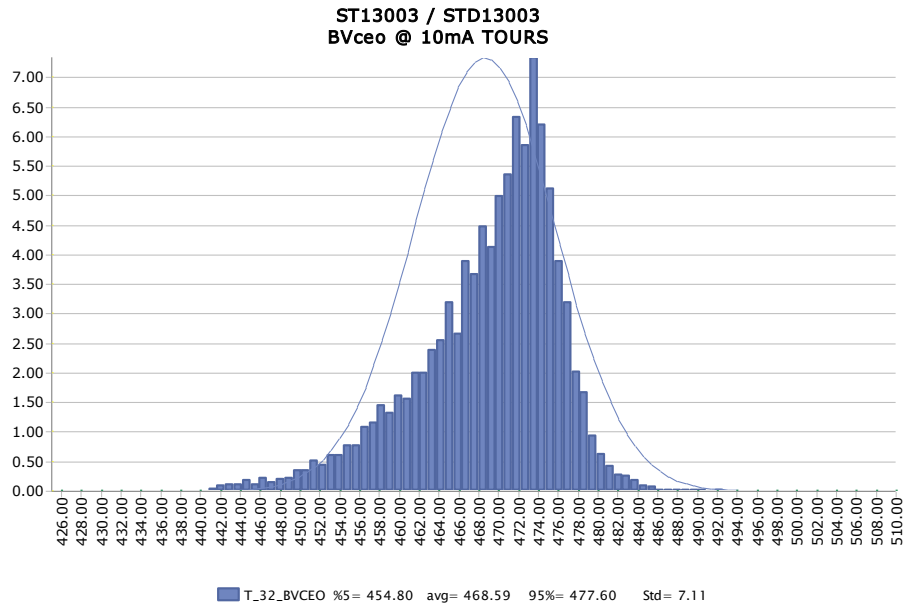
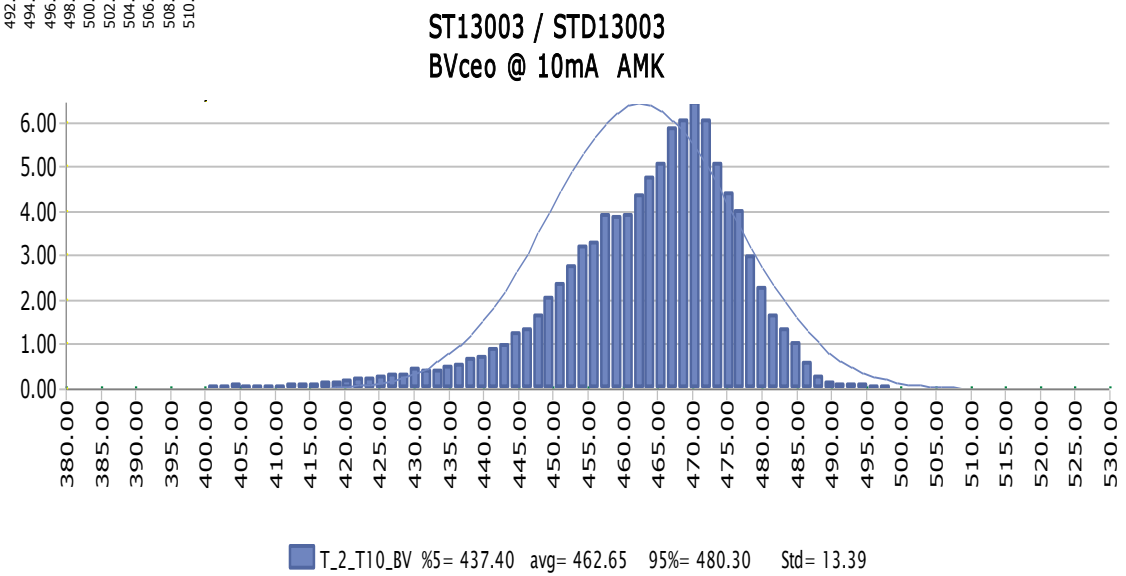
TOURS vs. AMK

PARAMETRIC VERIFICATION BVceo @ 10mA





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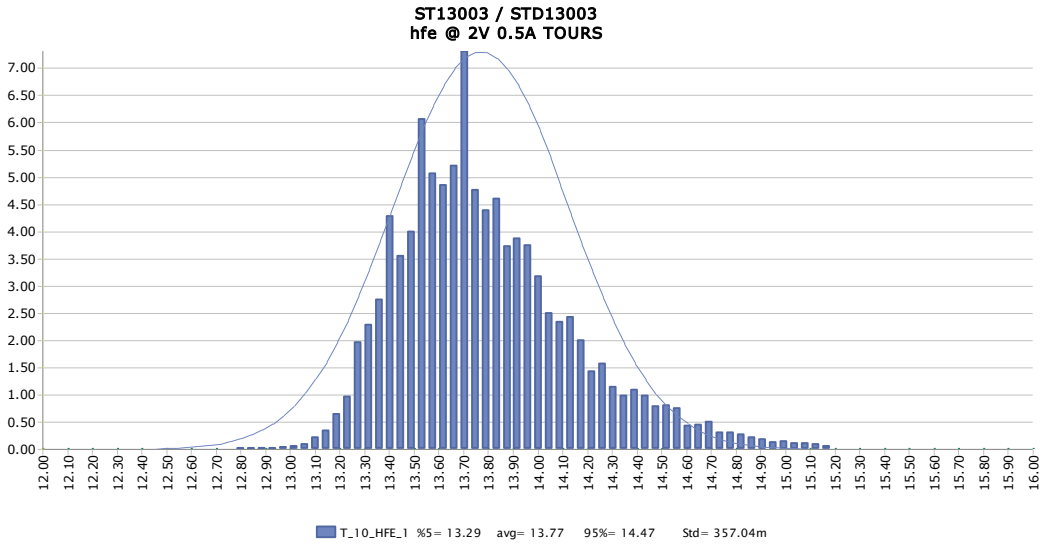
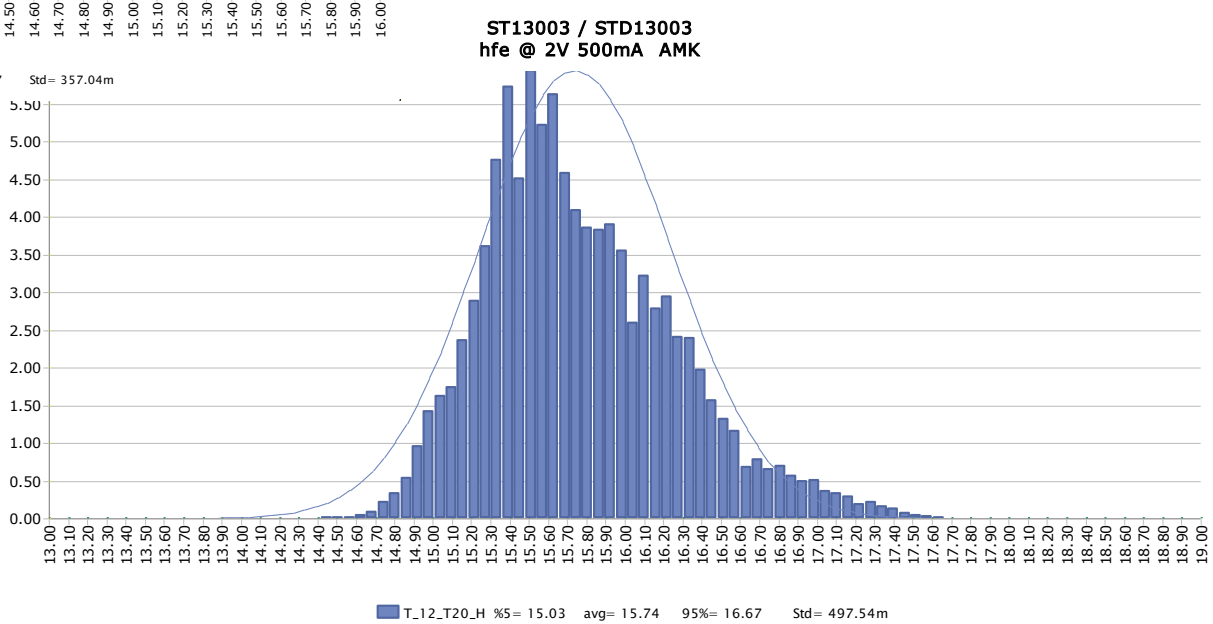
TOURS vs. AMK

PARAMETRIC VERIFICATION hfe @ 2V 500mA





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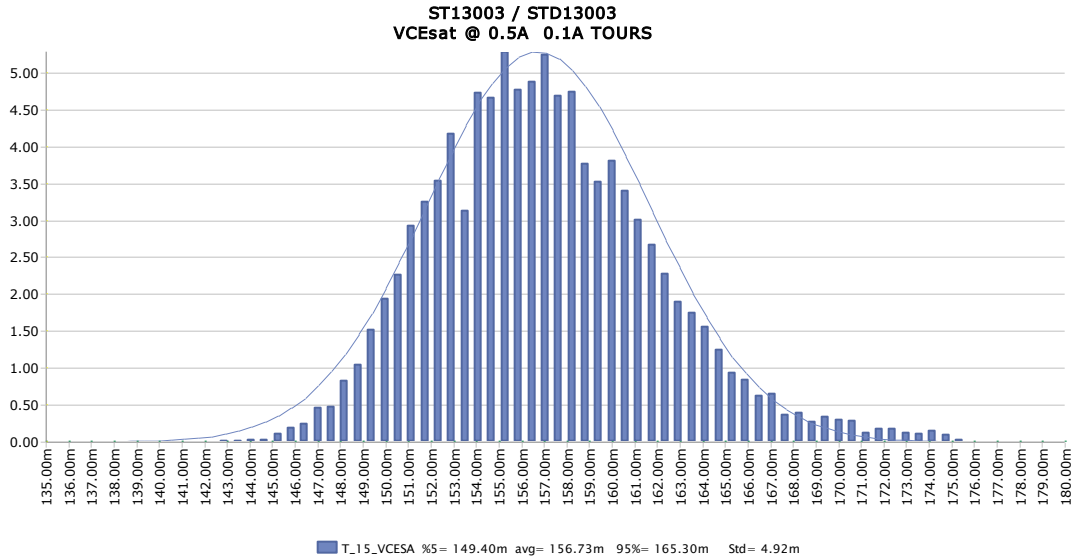
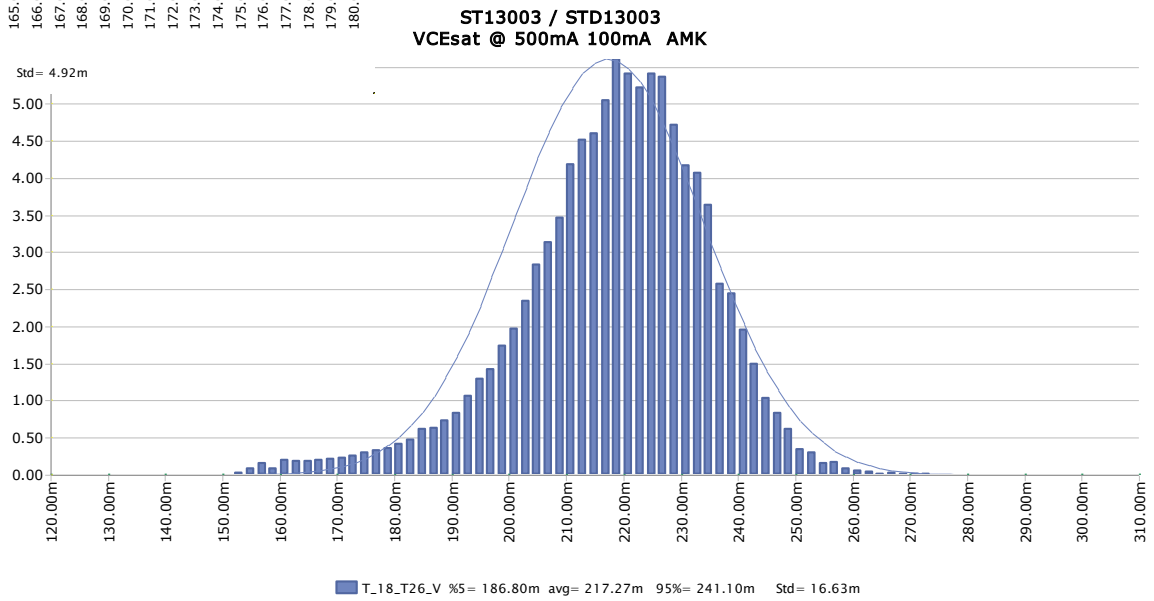
TOURS vs. AMK

PARAMETRIC VERIFICATION VCEsat @ 500mA 100mA





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TOURS vs. AMK

Limits (min & max) and CPK

Limits (min & max) and CPK

Commercial Product:	**ST13003 / STD13003**			
Wafer Fab site:	**Tours**		Wafer Fab site:	**AMK**
Test name	Bvceo @ 10mA			
	min:	400V	min:	400V
	max:		max:	
	CPK	3.21	CPK	1.55
Test name	hfe @ 2V 0.5A			
	min:	8	min:	8
	max:	20	max:	20
	CPK	5.38	CPK	5.18
Test name	VCEsat @ 0.5A 0.1A			
	min:		min:	
	max:	0.5V	max:	0.5V
	CPK	10.61	CPK	4.35

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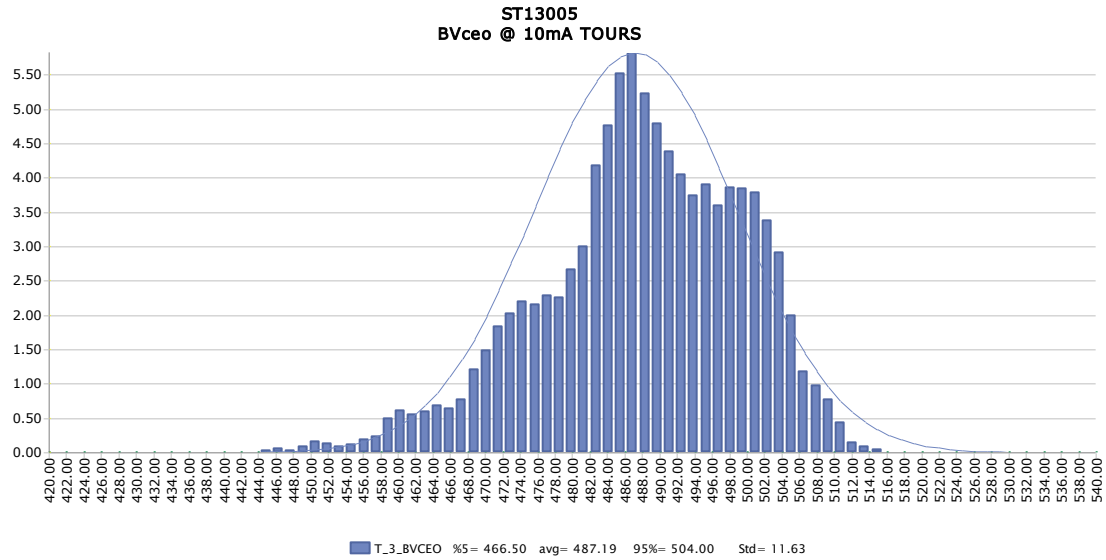
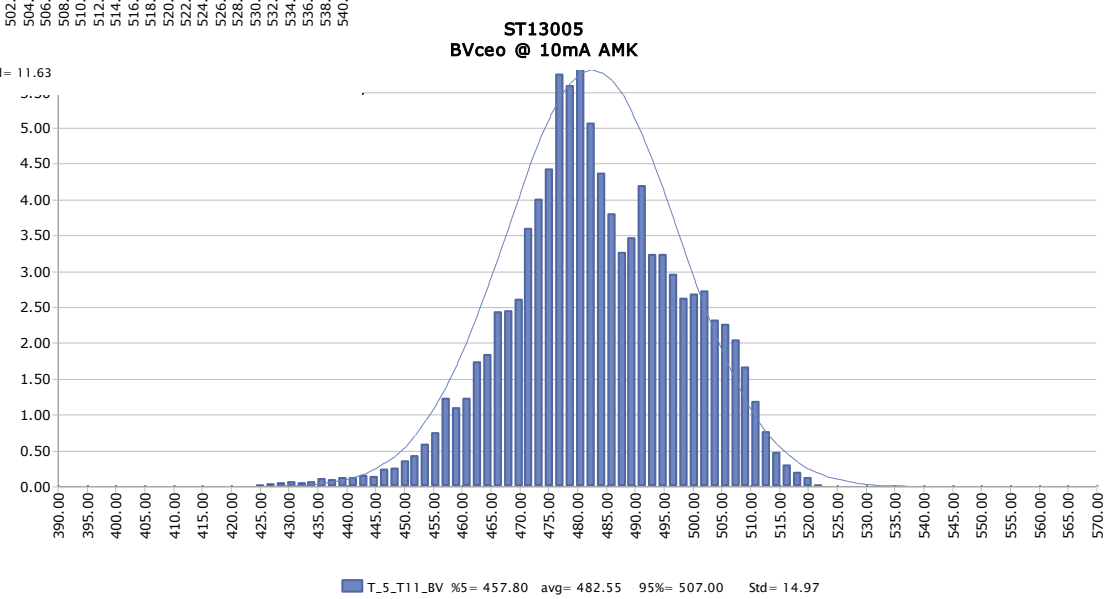
TOURS vs. AMK

PARAMETRIC VERIFICATION BVceo @ 10mA





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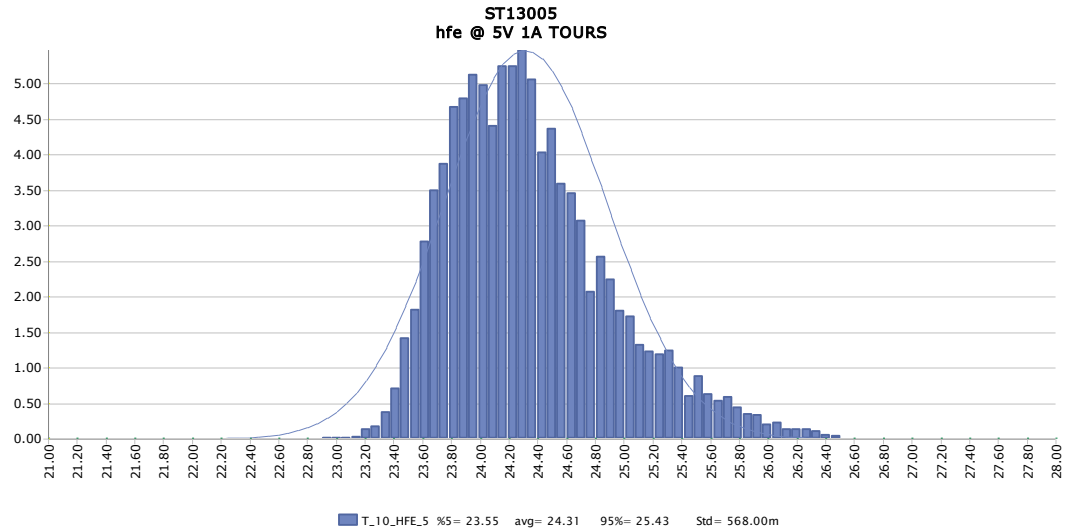
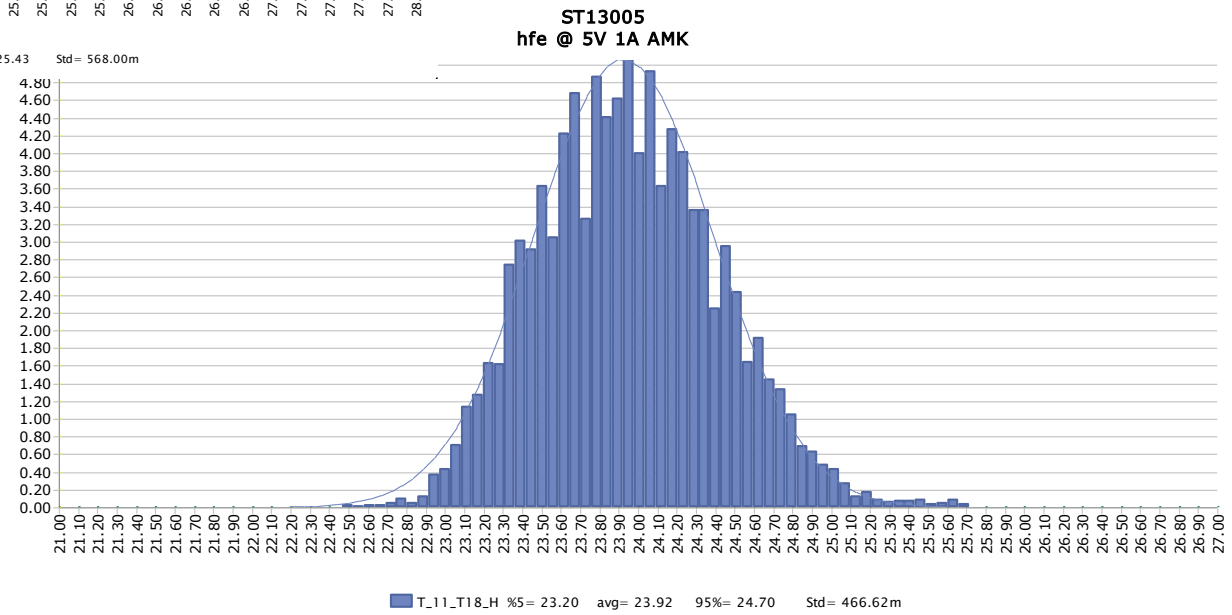
TOURS vs. AMK

PARAMETRIC VERIFICATION hfe @ 5V 1A





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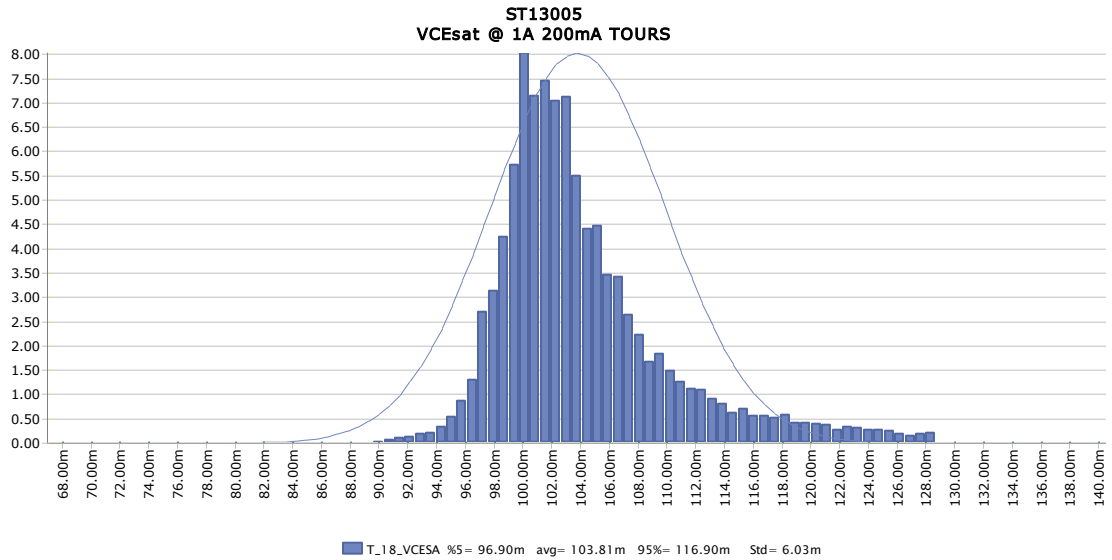
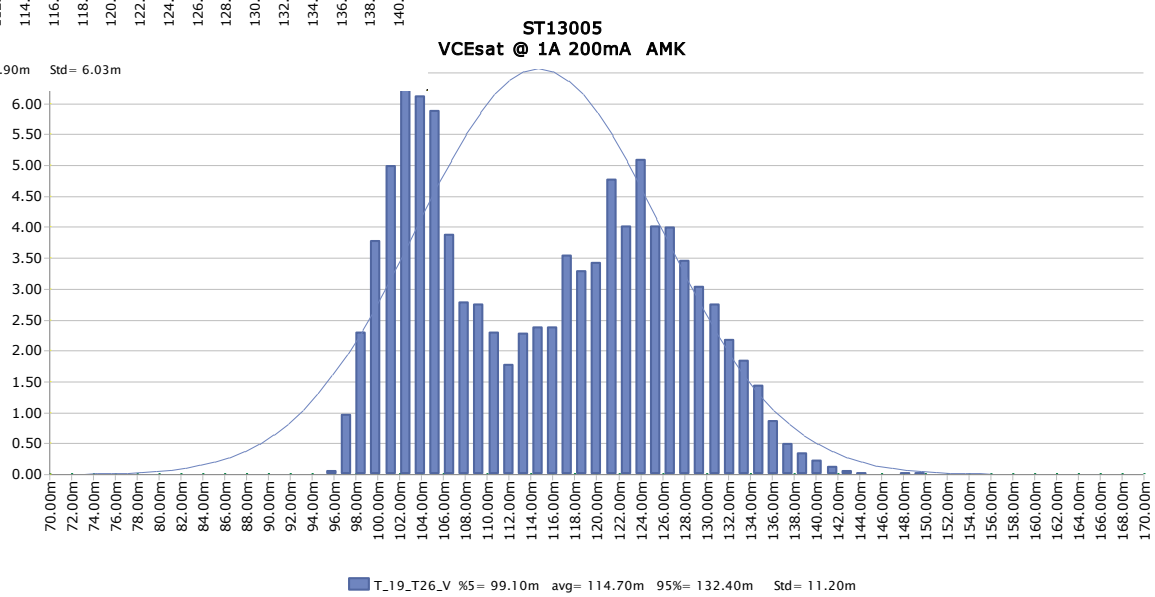
TOURS vs. AMK

PARAMETRIC VERIFICATION VCEsat @ 1A 200mA





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TOURS vs. AMK

Limits (min & max) and CPK

Limits (min & max) and CPK

Commercial Product:	**ST13005**			
Wafer Fab site:	**Tours**		Wafer Fab site:	**AMK**
Test name	Bvceo @ 10mA			
	min:	400V	min:	400V
	max:		max:	
	CPK	2.49	CPK	1.83
Test name	hfe @ 5V 1A			
	min:	15	min:	15
	max:	31	max:	31
	CPK	4.51	CPK	4.75
Test name	VCEsat @ 5A 1A			
	min:		min:	
	max:	0.9V	max:	0.9V
	CPK	5.73	CPK	3.41

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Reliability Report

Front-End Capacity Extension for Power Bipolar Transistors (Planar Technology) - Tours (France)

General Information	
Product Lines:	BV73, BV77
Product Families:	Power Bipolar Transistor
P/Ns:	BULB128-1 (BV73) STD13003T4 (BV77) ST13003 (BV77) STL73 (BV77)
Product Group:	IMS - IPD
Product division:	Power Transistor Division
Package:	I^2PAK, DPAK, SOT-32,TO-92
Silicon Process tech.:	High Voltage Planar Power Transistor

Locations	
Wafer Diffusion Plants:	*Tours (France)*
EWS Plants:	*Tours (France)*
Assembly plant:	*(BV73): I^2PAK SHENZHEN* *(BV77): DPAK LONG-GANG* *SOT-32 CHANGJIANG* *TO-92 ASE WEI-HAI*
Reliability Lab:	*IMS-IPD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	April 2013	9	C. Cappello	G.Falcone	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of Power Bipolar Transistors (Planar Technology) manufactured in the Tours (France) plant.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

High Voltage Planar Power Transistor

4.2 Construction note

D.U.T.: BULB128-1 LINE: BV73 PACKAGE: I^2PAK

Wafer/Die fab. information	
Wafer fab manufacturing location	Tours (France)
Technology	High Voltage Planar Power Transistor
Die finishing back side	Ti/Ni/Au
Die size	2310 x 2340 μm^2
Metal	Al/Si
Passivation type	P-Vapox (PSG)

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Tours (France)
Test program	WPIS

Assembly information	
Assembly site	ST-Shenzhen (China)
Package description	I^2PAK
Molding compound	Epoxy Resin
Frame material	Full Nichel
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg 5 mils Base Al/Mg 5 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST-Shenzhen (China)
Tester	IP-TESTER

D.U.T.: STD13003T4 LINE: BV77 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	Tours (France)
Technology	High Voltage Planar Power Transistor
Die finishing back side	Ti/Ni/Au
Die size	1320 x 1390 µm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Tours (France)
Test program	WPIS

Assembly information	
Assembly site	ST-LongGang (China)
Package description	DPAK
Molding compound	Resin
Frame material	Full Nichel
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Termosonic
Wires bonding materials	Cu 2 mils Base Cu 2 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST-LongGang (China)
Tester	IP-TESTER

D.U.T.: ST13003 LINE: BV77 PACKAGE: SOT-32

Wafer/Die fab. information	
Wafer fab manufacturing location	Tours (France)
Technology	High Voltage Planar Power Transistor
Die finishing back side	Ti/Ni/Au
Die size	1320 x 1390 μm^2
Metal	Al/Si
Passivation type	Yellow Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Tours (France)
Test program	WPIS

Assembly information	
Assembly site	Changjiang (China)
Package description	SOT-32
Molding compound	Epoxy Resin
Frame material	Full Nichel
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Termosonic
Wires bonding materials	Cu 1.7 mils Base Cu 1.7 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Changjiang (China)
Tester	TESEC

D.U.T.: STL73 LINE: BV77 PACKAGE: TO-92

Wafer/Die fab. information	
Wafer fab manufacturing location	Tours (France)
Technology	High Voltage Planar Power Transistor
Die finishing back side	Ti/Ni/Au
Die size	1320 x 1390 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Tours (France)
Test program	WPIS

Assembly information	
Assembly site	Ase Wei-Hai (China)
Package description	TO-92
Molding compound	Epoxy Resin
Frame material	Full Nichel
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Termosonic
Wires bonding materials	Cu 1.5 mils Base Cu 1.5 mils Emitter
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Ase Wei-Hai (China)
Tester	TESEC

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	P/N - Package	Product Line	Comments
1	BULB128-1 - I^2PAK	BV73	High Voltage Planar Power Transistor
2	STD13003T4 - DPAK	BV77	
3	ST13003 - SOT-32	BV77	
4	STL73 - TO-92	BV77	

5.2 Reliability test plan summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						LOT 1	LOT 2	LOT 3	LOT 4	
Die Oriented Tests										
HTRB	N	JESD22 A-108	TA = 150°C, BIAS=560V	77 x 4 lots	168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	
HTSL	N	JESD22 A-103	TA = 150°C	77 x 4 lots	168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	
Package Oriented Tests										
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ TA=85°C Rh=85% Over Reflow @ Tpeak=260°C/245°C 3 times	200 x 1 lot	FINAL		PASS			
AC	Y	JESD22 A-102	Pa=2Atm / TA=121°C	50 x 2 lots	96 H	0/50	0/50			
TC	Y	JESD22 A-104	TA = -65°C to 150°C	50 x 2 lots	100 cy	0/50	0/50			
					200 cy	0/50	0/50			
					500 cy	0/50	0/50			
TF/IOL	Y	Mil-Std 750D Method 1037	ΔTC=105°C	50 x 2 lots	5Kcy	0/50	0/50			
					10Kcy	0/50	0/50			
H3TRB	Y	JESD22 A-101	TA=85°C , RH=85% , BIAS= 100V	50 x 2 lots	168 H	0/50	0/50			
					500 H	0/50	0/50			
					1000 H	0/50	0/50			

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
AC Auto Clave	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB / THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Public Products List

PCN Title : Front-End Capacity Extension for Power Bipolar Transistors (Planar Technology) - Tours (France)
PCN Reference : IPD-PWR/13/7845
PCN Created on : 06-MAY-2013

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

2STL2580
2STL2580-AP
BUF420AW
BUF460AV
BUL128
BUL128D-B
BUL129D
BUL138
BUL312FP
BUL38D
BUL39D
BUL49D
BUL58D
BULB128-1
BULB49DT4
BULD118D-1
BULD39D-1
BUT11A
BUV298V
BUX348
BUX87
BUXD87T4
ESM6045DV
ST13003-K
ST13003D-K
ST13005
ST13005N
ST13007D
ST8812FX
ST901T
STB13007DT4
STBV32
STBV32-AP
STBV42
STBV42-AP
STBV42G-AP
STD13003T4
STD616A-1
STD901T
STI13005-H
STL128D
STL128DFP
STL128DN
STL128DNFP
STL73
STL73-AP
STL73D
STL73D-AP
STLD128DNT4
STN2580
STT13005-K
STT13005D-K
STU13005N
STW3040
STX0560
STX13003
STX13003-AP
STX13003G
STX13003G-AP
STX13005
STX616-AP
STX93003-AP
TR136
TR236
TRD136DT4

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