PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-APD/13/7769
Dated 27 Mar 2013

TDA2822M Wafer Diameter change

Table 1. Change Implementation Schedule

Forecasted implementation date for change	20-Mar-2013
Forecasted availability date of samples for customer	20-Mar-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	09-Apr-2013
Estimated date of changed product first shipment	26-Jun-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	TDA2822M
Type of change	Waferfab material change
Reason for change	To rationalize the production capacity
Description of the change	the wafer diameter for the products TDA2822M , (diffused on bipolar LABT process in AMJ9 fab) will be changed from 5" to 6". Note: with the agreement of the customer, parts from 6" wafers can be delivered even in advance in respect of the scheduled date.
Change Product Identification	Finished good code.
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
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TDA2822M Wafer Diameter change

WHAT

As part of the running program to convert to 6” wafers the silicon lines diffused on the bipolar processes in the Ang Mo Kio plant, the wafer diameter for the products TDA2822M , (diffused on LABT process) will be changed from 5” to 6”

WHY

To rationalize the production capacity.

HOW

The bipolar LABT diffusion process family is qualified and running in volumes on 6” wafers.
The qualification has been done through test vehicles belonging to the same LABT process family (namely KSAD-Reliability Report attached).
The alignment of electrical parameters of the TDA2822M will be monitored as well.

Note: with the agreement of the customer, parts from 6” wafers can be delivered even in advance in respect of the scheduled date.

Internal Reliability Evaluation Report

Qualify AMK5 versus **AMJ9 6"**
[LABT100 Technology]
T.V: KSADAAW - LD1117SC-R *SOT223*

General Information	
Product Line	KSADAAW
Product Description	Adj semi ld postive 800mA
P/N	LD1117SC-R
Product Group	APM
Product division	IPC
Package	SOT223
Silicon Process technology	BIPOLAR >6 um
Production mask set rev.	NKSADA6

Locations	
Wafer fab	*AMJ9 6"*
Assembly plant	*NANTONG FUJITSU CHINA*
Reliability Lab	*Catania*
Reliability assessment	*Pass*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	08-July-2011	9	Alfio Rao	Giuseppe Giacopello	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

LABT100 Bipolar Technology diffused in AMJ9 6" (Transferring project).

TV: KSADAAW – LD1117SC assembled in SOT223.

Shared qualification

3.2 Conclusion

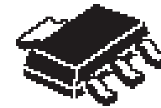
Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Features

Low dropout voltage:
– 1.15 V typ. @ I_{OUT} = 1 A, 25 ℃
Very low quiescent current:
– 5 mA typ. @ 25 ℃
Output current up to 1 A
Fixed output voltage of:
– 1.2 V, 1.8 V, 2.5 V, 3.3 V
Adjustable version availability (V_{REL} = 1.25 V)
Internal current and thermal limit
Only 10 µF for stability
Available in ± 2 % (at 25 ℃) and 4 % in full temperature range
High supply voltage rejection:
– 80 dB typ. (at 25 ℃)
Temperature range: 0 ℃ to 125 ℃



SOT-223

Description

The LD1117Axx is a low drop voltage regulator able to provide up to 1 A of output current, available even in adjustable version (V_{REF} = 1.25V). Concerning fixed versions, are offered the following output voltages: 1.2 V, 1.8 V, 2.5 V and 3.3 V. The device is supplied in: SOT-223, DPAK and TO-220. Surface mount packages optimize the thermal characteristics even offering a relevant space saving effect. High efficiency is assured by NPN pass transistor. Only a very common 10 µF minimum capacitor is needed for stability. Only chip trimming allows the regulator to reach a very tight output voltage tolerance, within ± 2 % at 25 ℃.

4.2 Construction note

	P/N: LD1117SC-R
Wafer/Die fab. information	
Wafer fab manufacturing location	AMJ9 6"
Technology	LABT
Process family	BT/B
Die finishing back side	Cr/Ni/Au
Die size	1.990X1.860mm2
Bond pad metallization layers	AlSi
Passivation type	SiN (nitride)
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APPE (Singapore)
Assembly information	
Assembly site	NANTONG FUJITSU CHINA
Package description	SOT223
Molding compound	SUMITOMO EMEG600F
Frame material	Copper 118x93
Die attach process	Glue
Die attach material	ABLESTICK 8352L
Die pad size	146X200, 146X410, 146X360, 167X167
Wires bonding materials/diameters	Au 1.5 mils
Lead finishing process	Matte Tin Plating
Final testing information	
Testing location	NANTONG FUJITSU CHINA
Tester	QT200
Test program	KSX2FAAD.CTS

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

P/N: LD1117SC-R

Lot #	Diffusion Lot	Assy Lot	Technical Code	Package	Product Line	Data Code
1	W047K34	GF113030	FMLL*KSADAAW	*SOT223*	KSADAAW	'113

5.2 Test plan and results summary

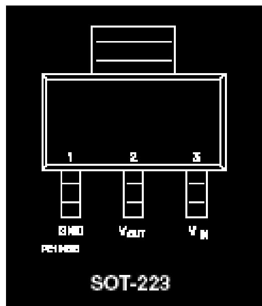
P/N: LD1117SC-R

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS	Note
						Lot 1	
Die Oriented Tests							
HTOL	N	JESD22 A-108	Tj = 125°C, BIAS= 15V	77	168 h	0/77	
					500 h	0/77	
					1000 h	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C	45	168 h	0/45	
					500 h	0/45	
					1000 h	0/45	
Package Oriented Tests							
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168h @ Ta= 85°C Rh= 85 % Over Reflow @ Tpeak= 260°C 3 times	250	Final	Pass	
AC	Y	JESD22 A-102	Pa= 2Atm / Ta= 121°C	77	168 h	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	77	100 cy	0/77	
					200 cy	0/77	
					500 cy	0/77	
THB	Y	JESD22 A-101	Ta= 85°C, RH = 85%, BIAS= 12V	77	168 h	0/77	
					500 h	0/77	
					1000 h	0/77	

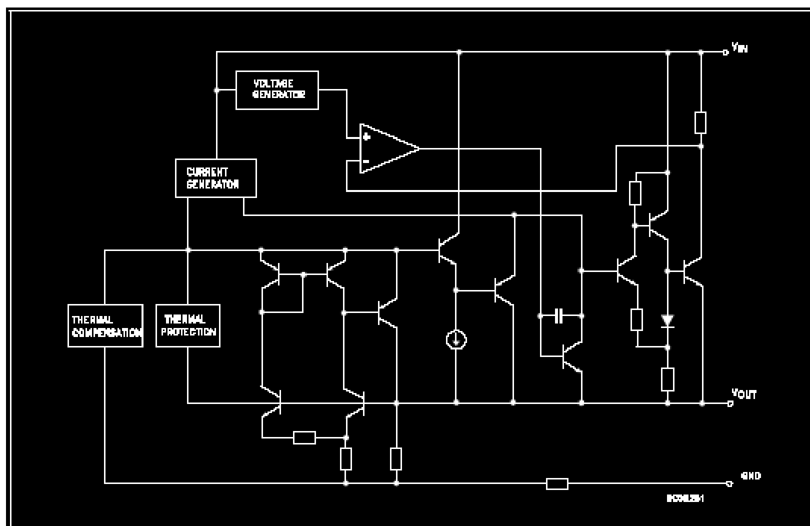
6 ANNEXES

6.1 Device details

6.1.1 Pin connection



6.1.2 Block diagram



6.1.3 Bonding diagram

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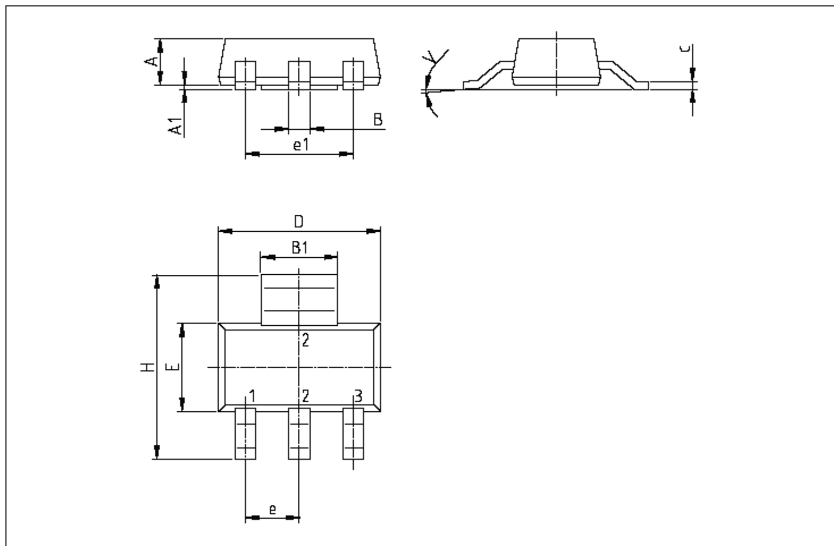
6.1.4 Package outline/Mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.8			70.9
A1	0.02		0.1	0.8		3.9
B	0.6	0.7	0.85	23.6	27.6	33.5
B1	2.9	3	3.15	114.2	118.1	124.0
c	0.24	0.26	0.35	9.4	10.2	13.8
D	6.3	6.5	6.7	248.0	255.9	263.8
e		2.3			90.6	
e1		4.6			181.1	
E	3.3	3.5	3.7	129.9	137.8	145.7
H	6.7	7	7.3	263.8	275.7	287.5
V			10°			10°

Table title: SOT-223 mechanical data



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

Public Products List

PCN Title : TDA2822M Wafer Diameter change
PCN Reference : AMS-APD/13/7769
PCN Created on : 26-MAR-2013

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

TDA2822M

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