PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS-APD/13/7743
Dated 21 Mar 2013

High side current sense amplifier SOT23-5 package robustness improvement

Table 1. Change Implementation Schedule

Forecasted implementation date for change	01-Jul-2013
Forecasted availability date of samples for customer	29-Mar-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	14-Mar-2013
Estimated date of changed product first shipment	05-Jul-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached
Type of change	Package assembly material change
Reason for change	Package robustness improvement
Description of the change	The purpose of this qualification is to improve the existing SOT23-5 package robustness. As part of our improvement action to resolve the issue of die shear mode failure and the cratering issue encoun-tered on some specific application, we would like to convert the wafer bumps from Lead-free back to "High-Lead". The molding compound has been changed to halogen free with high lead bumps. Our devices remain Ecopack2 compliant. Samples availability: TSC101AIYLT & TSC888BILT ==> week13 2013. TSC888CILT & TSC101AILT ==> week17 2013. Others part upon specific customer’s request. Please enter a non-standard samples order in the system with PCN#7743 in comment.
Change Product Identification	xx$Yx instead of xx$YxH
Manufacturing Location(s)	

DOCUMENT APPROVAL

Name	Function
Camiolo, Jean	Marketing Manager
De marco, Alberto	Product Manager
Bugnard, Jean-Marc	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS-APD/13/7743

Analog, MEMS and Sensor Group

0101 Product line Qualification / High lead bumps

WHAT:

The aim of this qualification is to improve the existing SOT23-5 package robustness.
As part of our improvement action to resolve the issue of die shear mode failure and the cratering issue encountered on some specific application, we would like to convert the wafer bumps from Lead-free back to "High-Lead".

The molding compound has been switched to halogen free with high lead bumps.

	1st process	**Current process**	**Modified process**
Assembly location	CARSEM Malaysia		
Bumps	**SnPb High Lead**	**Lead free**	**SnPb High Lead**
Leadframe	Copper		
Molding compound	**Nitto MP8000**	**Hitachi CEL 8240 HF**	**Hitachi CEL 8240 HF**
Lead finishing	Matte Sn		
Wafer thickness	275µm		
Backgrinding location	CARSEM Malaysia		

For the complete list of part numbers affected by the change, please refer to the attached Product list.
Samples availability: TSC101AIYLT & TSC888BILT ➔ week13 2013 upon request.
TSC888CILT & TSC101AILT ➔ week17 2013 upon request.
Other part numbers upon specific customers request.

WHY:
To improve package robustness during reflow process at Customer manufacturing lines.

HOW:
The change that covers AMS (Analog, Mems & Sensors) products is qualified based on qualification plan here attached.
Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of performing comparative package characterization and reliability tests. Please refer to Reliability evaluation plan for all details.

WHEN:
Production in ST Bumping Subcontractor ChipBond in High Lead bumps for AMS products is forecasted in July 2013.

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by a dedicated finished good ending with xx$Yx instead of xx$YxH for leadfree bumps.

The changes here reported will not affect the electrical, dimensional, thermal parameters and reflow process keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Reliability Evaluation Report

0101 Product line Qualification / High lead bumps for AMS products (Analog MEMS & Sensor Group)

General Information	
Product Line	101A01, 101B01, 101C01
Product Description	High side current sense amplifier
P/N	TSC101xIYLT, TSC101xILT, TSC888xILT
Product Group	AMS
Product division	Analog
Package	SOT23-5
Silicon Process technology	BCD3 SHRINK
Production mask set rev.	1.0
Maturity level step	30

Locations	
Wafer fab	AMK6 6" / CHIPBOND bumping
Assembly plant	CARSEM Malaysia
Reliability Lab	Grenoble

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Reviewed by	Approved by	Comment
1.0	26 feb 2013	13	S. Fassetta	X Rochette	JM Bugnard	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The aim of this qualification consists in improving the existing SOT23-5 package robustness.
As part of our improvement action to resolve some issue of die shear mode failure and some cratering issue encountered on some specific application, we would like to convert the wafer bumps from Lead-free back to “High-Lead”.

The molding compound has been switched to halogen free with high lead bumps.

	1st process	Current process	Modified process
Assembly location	CARSEM Malaysia		
Die attach	N/A		
Bumps	**SnPb High Lead**	**Lead free**	**SnPb High Lead**
Leadframe	Copper		
Molding compound	**Nitto MP8000**	**Hitachi CEL 8240 HF**	**Hitachi CEL 8240 HF**
Lead finishing	Matte Sn		
Wafer thickness	275µm		
Backgrinding location	CARSEM Malaysia		

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

TSC101

High side current sense amplifier

Features

- Independent supply and input common-mode voltages
- Wide common-mode operating range: 2.8 to 30 V
- Wide common-mode surviving range: -0.3 to 60 V (load-dump)
- Wide supply voltage range: 4 to 24 V
- Low current consumption: I_{CC} max = 300 µA
- Internally fixed gain: 20 V/V, 50 V/V or 100 V/V
- Buffered output

Applications

- Automotive current monitoring
- Notebook computers
- DC motor controls
- Photovoltaic systems
- Battery chargers
- Precision current sources

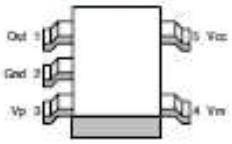
Description

The TSC101 measures a small differential voltage on a high-side shunt resistor and translates it into a ground-referenced output voltage. The gain is internally fixed.

Wide input common-mode voltage range, low quiescent current, and tiny SOT23 packaging enable use in a wide variety of applications.

L
SOT23-5
(Plastic package)

Pin connections
(top view)



The input common-mode and power supply voltages are independent. The common-mode voltage can range from 2.8 to 30 V in operating conditions and up to 60 V in absolute maximum rating conditions.

The current consumption below 300 µA and the wide supply voltage range enable the power supply to be connected to either side of the current measurement shunt with minimal error.

March 2011 Doc ID 13313 Rev 3 1/18
www.st.com

See referenced Product Baseline for detailed information.

	P/N TSC101xIYLT, TSC101xILT, TSC888xILT
Wafer/Die fab. information	
Wafer fab manufacturing location	AMK6 6"
Technology	BCD
Process family	BCD3SW HVSHRUNK
Die finishing back side	RAW SILICON
Die size	83 x 44 mils
Bond pad metallization layers	Ti/Cu/SnAg
Passivation type	PSG + NITRIDE + BCB
Poly silicon layers	
Wafer Testing (EWS) information	
Electrical testing manufacturing location	APEE Asia Pac Singapore EWS
Tester	ASL1000
Test program (Consumer part)	T101AAW 1
Test program (Automotive part “Y”)	T101AYW 2
Assembly information	
Assembly site	CARSEM M - MALAYSIA
Package description	SOT 23-5
Molding compound	Hitachi CEL8240HF10LXC
Frame material	HD L/F SOT23.5L 0.95mm pitch FCOL option 1
Die attach process	N/A
Die attach material	Flip chip (high lead solder)
Die pad size	N/A
Wire bonding process	N/A
Wires bonding materials/diameters	N/A
Lead finishing process	Matte Sn
Lead finishing/bump solder material	SnPb High lead
Substrate supplier for BGA	N/A
Final testing information	
Testing location	CARSEM
Tester	ASL1000
Test program +25°C (Consumer part)	T101ABF 1
Test program +125°C (Automotive part “Y”)	T101AYF 2

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Test vehicle	Lot #	Product	Resin / bump material
TV1	H650539 (1st diffusion lot)	TSC101C	Nitto / leaded bump
	H706288 (2nd diffusion lot)	TSC101B	
	H712473 (3rd diffusion lot)	TSC101A	
	6814HVY (4th diffusion lot)	TSC101B	
TV2	6909FFT (5th diffusion lot)	TSC101C	Hitachi / leadfree bump
TV3	ENG24002.0222 TC: 9Y240ACG V6 9Y	TSC101A	Hitachi / leaded bump

Detailed results in below chapter will refer to P/N and Lot #.

5.2 Test plan and results summary

Tests	Conditions	Step	TV1	TV2	TV3	Comments
Line			101B01	101C01	101A01	
ESD	HBM		2.5kV			
ESD	CDM		1.5kV			
ESD	MM		150V			
HTB	Tj=150C Vs=absolute max rating	1000h	0/312	0/78		
HTSL	Tj=150C Vs=Max operating	1000h	0/156	0/78		
THB	Ta=85C RH=85% Vs=nominal	1000h	0/312	0/78		
AC	Ta=121C P=2atm	96h	0/312	0/78	0/80	
TMC	Ta=-65/+150C Ambiant & Hot Test	100cy			0/320	
		500cy			0/320	
		1000cy	0/312	0/78	0/320	
MSL	Baking (150°C) Moisture soak 3 IR reflow soldering	24h			0/400	
		Jedec			0/400	
		260°C			0/400	
ELFR	T° AMB = 150°C Duration = 24H		0/800	0/200		
SD	Solderability		0/30			No fail
PD	Physical dimension		0/60			In spec

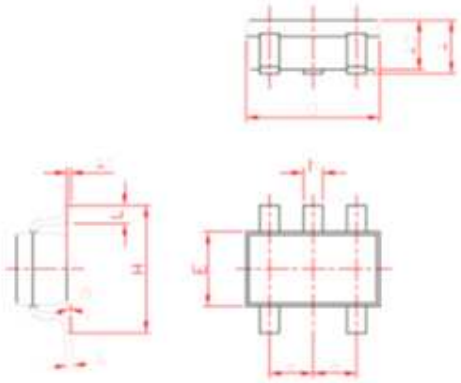
Physical dimensions for SOT23-5 package assembled in CARSEM Malaysia

PURPOSE: To check the physical dimensions of SOT23-5 package produced in CARSEM Malaysia.

REFERENCE: Automobile Electronics Council - Q100 – RevG (May 14th, 2007)
("Stress test qualification for packaged integrated circuits")

REF.	DATABOOK			DRAWING						NOTES
		MILLIMETERS					INCHES			
	TYP	MIN	MAX	TYP	MIN	MAX	TYP	MIN	MAX	
A		0.90	1.45		0.90	1.45		0.035	0.057	
A1		0.00	0.15		0.00	0.15		0.000	0.006	
A2		0.90	1.30		0.90	1.30		0.035	0.051	
b		0.30	0.50		0.30	0.50		0.012	0.020	
c		0.09	0.20		0.09	0.20		0.004	0.008	
D		2.80	3.05	2.90			0.110			
E		1.50	1.75	1.60			0.063			
e	0.95			0.95			0.037			
H		2.60	3.00	2.80			0.110			
L		0.30	0.60		0.30	0.60		0.012	0.024	
α		0	10		0	8		0	8	DEGREES

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
A	1.263	1.242	1.267	1.268	1.238	1.274	1.272	1.294	1.277	1.256
A1	0.06	0.05	0.054	0.078	0.035	0.056	0.074	0.073	0.062	0.063
A2	1.2	1.186	1.205	1.208	1.207	1.217	1.198	1.203	1.206	1.203
b	0.347	0.354	0.351	0.347	0.336	0.336	0.339	0.344	0.342	0.358
c	0.136	0.139	0.136	0.134	0.133	0.138	0.136	0.131	0.138	0.13
D	2.906	2.876	2.9	2.904	2.903	2.878	2.881	2.904	2.887	2.895
E	1.627	1.61	1.603	1.622	1.608	1.603	1.536	1.622	1.7	1.624
e	0.95	0.95	0.95	0.95	0.95	0.95	0.95	0.95	0.95	0.95
H	2.806	2.797	2.807	2.806	2.817	2.804	2.807	2.804	2.811	2.807
L	0.45	0.435	0.436	0.452	0.444	0.456	0.443	0.461	0.443	0.446



Solderability results SOT23 package assembled in CARSEM Malaysia

PURPOSE: To verify the solderability for Sot23-5 package produced in Carsem Malaysia.

REFERENCE: Automobile Electronics Council - Q100 - Rev. G (May 14th, 2007)
("Stress test qualification for packaged integrated circuits")
Jedec JESD22b102d solderability standard
IEC 60749-21 solderability standard
ST 0018688 SOLDERABILITY TEST METHOD (postplated component)
ST 0128685 SOLDERABILITY TESTING METHOD FOR PREPLATED PACKAGE

METHOD:

- Half part of the specimens is subjected to aging by exposure of the surfaces to be tested to steam (time of aging 8 hrs +/-0.5hrs). The other specimens are subjected to aging by exposure of the surfaces to be tested to dry air (16 hours).
- The parts are, then, dried.
- To flux the leads
- Solder bath immersion
- Flux removal
- Examination of terminations
  Description of possible defects: Non wetting, Dewetting, porosity/pinholes, foreign material.
- Acceptance criteria:
  Total surface inspected shall be at least 95% covered by a continuous coating of new solder.
  No defects (as described previously)

Specification Number	0018688 (solderability test method)
Equipment	Solder baths SnAgCu and SnPb
Sampling	10/ageing/bath

PACKAGE	SOLDER BATH	SOLDER BATH TEMP.	SOLDER DIPPING TIME	AGING	SAMPLING	REJECT
SMD with Pre plated NiPdAu	SnPb	220°C	10s on lead	8h steam	10	0
			10s on lead	8hrs dry air	10	0
	SnAgCu	245°C	10s on lead	8h steam	10	0
			10s on lead	8hrs dry air	10	0

Sample	Die Shear (kg/f) s/s = 50 units ENG24001				Die Shear (kg/f) s/s = 50 units ENG24002			
	Data	Mode	Data	Mode	Data	Mode	Data	Mode
1	0.47	5A	0.43	5A	0.43	5A	0.49	5A
2	0.51	5A	0.44	5A	0.44	5A	0.39	5A
3	0.47	5A	0.44	5A	0.45	5A	0.41	5A
4	0.43	5A	0.45	5A	0.46	5A	0.45	5A
5	0.45	5A	0.49	5A	0.46	5A	0.46	5A
6	0.43	5A	0.51	5A	0.48	5A	0.44	5A
7	0.44	5A	0.43	5A	0.42	5A	0.38	5A
8	0.44	5A	0.48	5A	0.42	5A	0.43	5A
9	0.45	5A	0.44	5A	0.40	5A	0.41	5A
10	0.44	5A	0.52	5A	0.45	5A	0.42	5A
11	0.43	5A	0.45	5A	0.46	5A	0.49	5A
12	0.43	5A	0.46	5A	0.39	5A	0.47	5A
13	0.45	5A	0.43	5A	0.45	5A	0.43	5A
14	0.48	5A	0.43	5A	0.54	5A	0.50	5A
15	0.47	5A	0.46	5A	0.46	5A	0.40	5A
16	0.36	5A	0.42	5A	0.45	5A	0.43	5A
17	0.41	5A	0.44	5A	0.42	5A	0.41	5A
18	0.46	5A	0.39	5A	0.43	5A	0.42	5A
19	0.47	5A	0.46	5A	0.44	5A	0.44	5A
20	0.46	5A	0.34	5A	0.45	5A	0.39	5A
21	0.44	5A	0.46	5A	0.44	5A	0.39	5A
22	0.35	5A	0.51	5A	0.42	5A	0.45	5A
23	0.36	5A	0.44	5A	0.52	5A	0.45	5A
24	0.43	5A	0.43	5A	0.53	5A	0.42	5A
25	0.44	5A	0.40	5A	0.52	5A	0.44	5A
Maximum	**0.52**				**0.54**			
Minimum	**0.34**				**0.38**			
Spec Limit (L)	**0.20**				**0.20**			
Spec Limit (U)	**N/A**				**N/A**			
Mean	**0.44**				**0.44**			
Std. Dev.	**0.04**				**0.04**			
PpK	**2.09**				**2.12**			

Note

Die shear failure mode definition.
A : Bump shear at centre
B : Bump sheared at leadframe/substrate
C : Bump sheared at die (with solder remained on pad)
D : Bump sheared at die (without solder remained on pad)
E : Bump separated from solder paste

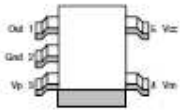
6 ANNEXES

6.1 Device details

6.1.1 Pin connection

L
SOT23-5
(Plastic package)

Pin connections
(top view)



Application schematics and pin description

The TSC101 high-side current sense amplifier features a 2.8 to 30 V input common-mode range that is independent of the supply voltage. The main advantage of this feature is that it allows high-side current sensing at voltages much greater than the supply voltage (V_{CC}).

Figure 1. Application schematics

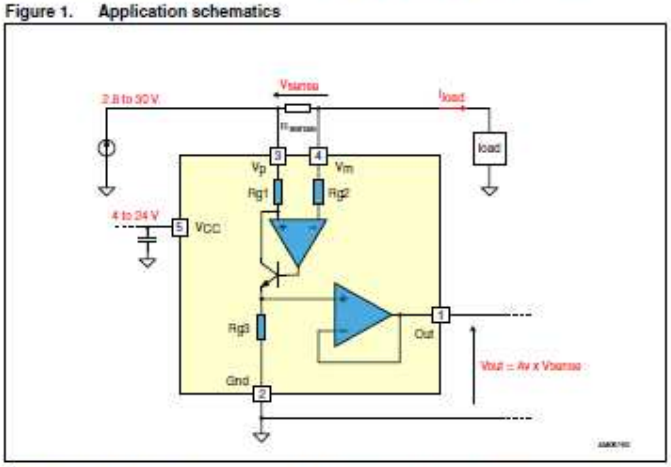


Table 1 describes the function of each pin. The pin positions are shown in the illustration on the cover page and in *Figure 1* above.

Table 1. Pin descriptions

Symbol	Type	Function
Out	Analog output	Output voltage, proportional to the magnitude of the sense voltage V_p-V_m.
Gnd	Power supply	Ground line
V_{CC}	Power supply	Positive power supply line
V_p	Analog input	Connection for the external sense resistor. The measured current enters the shunt on the V_p side.
V_m	Analog input	Connection for the external sense resistor. The measured current exits the shunt on the V_m side.

6.1.2 Package outline/Mechanical data

Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 24. SOT23-5L package mechanical drawing

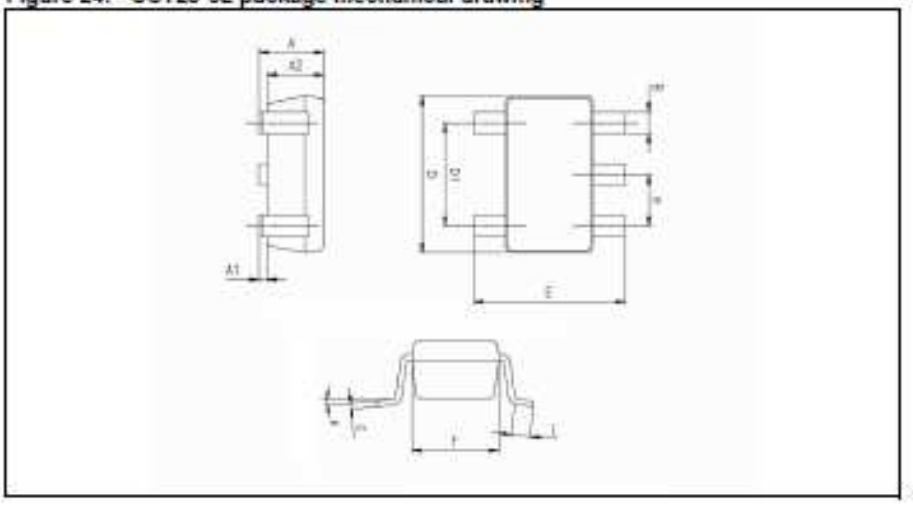


Table 9. SOT23-5L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0 degrees		10 degrees			

6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL Higt Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

6.3 ESD certificates

CERTIFICATE OF ELECTROSTATIC DISCHARGE SENSITIVITY
ACCORDING TO THE PROCEDURE N°0060102

Operator's name: Chenevas-Paule Hervé
Date: September, 13th 2007
Commercial product: TSC101AIL
Die code: P101AAAX
Package: sot23.5
Traceability code: Y724

☒ HBM (Human Body Model)
Equipment reference: 3000065565 / 3000003031
Number of units: 3
This product meets the electrostatic discharge resistance specification of 2.5KV and is compliant with the following standards :
- MIL883C
- JEDEC JESD22
- ANSI ESD STM 5.1

☒ MM (Machine Model)
Equipment reference: 3000065565 / 3000003031
Number of units: 3
This product meets the electrostatic discharge resistance specification of 150V and is compliant with the following standards :
- MIL883C
- JEDEC JESD22
- ANSI ESD STM 5.1

☒ CDM (Charged Device Model)
Equipment reference: 3000034218
Number of units: 3
This product meets the electrostatic discharge resistance specification of 1500V and is compliant with the following standards :
- MIL883C
- JEDEC JESD22
- ANSI ESD STM 5.1

6.4 LU certificates

CERTIFICATE OF LATCH-UP

ACCORDING TO THE PROCEDURE N°0018695

Operator's name: ESCH Helene
Date: January, 1st 2007
Commercial product: TSC101CIL
Die code: P101CABX
Package: Sot 23-5
Traceability code: Y713
LATCH-UP tester reference: Tektronix 370A

CURRENT INJECTION			Injection +		Class	Injection -		Class
	Pin n°	Type	I (mA)	V (V)		-I (mA)	-V (V)	
INPUTS	2	Invert	200mA	90V*	A	-200mA	-1.2V	A
	3	Non Invert	200mA	90V*	A	-200mA	-1.2V	A
OUTPUTS	1	Low output	200mA	28.7V	A	-200mA	-1.2V	A
		High output	200mA	28.7V	A	-200mA	-1.2V	A

* At around 40mA, the diode comes into snap-back mode => 200mA 40V

SUPPLY	Latch-up	No Latch-up
Overvoltage		X
Supply cut		X

Test type	Trigger polarity	Quality Level	Trigger stress
Supply voltage		A	2xVmax or 500mA
		B	1.5xVmax or 1.5xInom or Inom+100mA
Current injection	Positive	A	2xVmax or 200mA
		B	1.5xVmax or 1.5xInom or Inom+100mA
	Negative	A	-2xVmax or -200mA
		B	-1.5xVmax or -0.5xInom or -100mA
		C	If limit of level B is not achieved

Public Products List

PCN Title : High side current sense amplifier SOT23-5 package robustness improvement
PCN Reference : AMS-APD/13/7743
PCN Created on : 18-MAR-2013

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

TSC101AILT	TSC101AIYLT	TSC101BILT
TSC101BIYLT	TSC101CILT	TSC101CIYLT
TSC888AILT	TSC888BILT	TSC888CILT

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