# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/13/7720
Dated 28 Feb 2013

**M34E02 2-Kbit I2C Bus EEPROM Redesign and upgrade to the CMOSF8H+ process technology**

**Table 1. Change Implementation Schedule**

| | |
|---|---|
| Forecasted implementation date for change | 21-Feb-2013 |
| Forecasted availability date of samples for customer | 21-Feb-2013 |
| Forecasted date for **STMicroelectronics** change Qualification Plan results availability | 21-Feb-2013 |
| Estimated date of changed product first shipment | 30-May-2013 |

**Table 2. Change Identification**

| | |
|---|---|
| Product Identification (Product Family/Commercial Product) | M34E02 products family |
| Type of change | Waferfab technology change |
| Reason for change | Line up to state-of-the-art of process |
| Description of the change | Redesign and upgrade to the new CMOSF8H+ Process technology. |
| Change Product Identification | Process Technology identifier "T" |
| Manufacturing Location(s) | |

# DOCUMENT APPROVAL

| Name | Function |
|---|---|
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# PRODUCT / PROCESS CHANGE NOTIFICATION

## M34E02 2-Kbit I2C Bus EEPROM
## Redesign and upgrade to the CMOSF8H+ process technology

**What is the change?**

The **M34E02**, *2-Kbit serial presence detect (SPD) EEPROM for double data rate (DDR1, DDR2 and DDR3) DRAM modules* product family, assembled in **UFDFPN8** and **TSSOP8** packages, currently produced using the CMOSF6SP 36% process technology at ST Ang Mo Kio (Singapore) 6" wafer diffusion plant or at GLOBALFOUNDRIES (Singapore) 8" wafer diffusion plant, has been **redesigned** and will be **upgraded** to the **CMOSF8H+** process technology at **ST Rousset** (France) 8" wafer diffusion plant.

The CMOSF8H+ is closely derived from CMOSF8H (already used for production of densities ranging from 32 Kb to 2 Mb), with a more compact layout in order to achieve competitive die size.

The new M34E02 in CMOSF8H+ version is functionally compatible with the current CMOSF6SP 36% version as per datasheet rev. 11 – May 2011, attached.

The upgraded M34E02 is described in new datasheet rev. 13:

- DC characteristic: $I_{CC1}$ standby supply current:
  - Max 3 µA at $V_{CC}$ = 5.5 V
  - Max 2 µA at $V_{CC}$ = 2.5 V
  - Max 1 µA at $V_{CC}$ = 1.8 V

- Absolute maximum rating: $V_{ESD}$ electrostatic pulse Human Body model:
  - Max 3000 V

Concurrent to this change, the UFDFPN8 and TSSOP8 packages will be assembled with 0.8 mil Copper wire (Copper wire assembly process already qualified for M24C01, M24C02, M24C04 and M24C16 in CMOSF8H+, when assembled in SO8N at ST Shenzhen (China)).

**Why?**

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M34E02 in the new CMOSF8H+ process technology will increase the production capacity throughput and consequently improve the service to our customers.

**When?**

The production of the upgraded M34E02 with the new CMOSF8H+ and assembled in UFDFPN8 and TSSOP8 packages will ramp up from April 2013 and shipments can start from May 2013 onward (or earlier upon customer approval).

**How will the change be qualified?**

The new version of the M34E02 in CMOSF8H+ and assembled in UFDFPN8 and TSSOP8 packages will be qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

The **Qualification Report QRMMY1209** is available and included inside this document.

**What is the impact of the change?**

**- Form:** Marking change (see **Device marking** paragraph)

**- Fit:** No change

**- Function:**

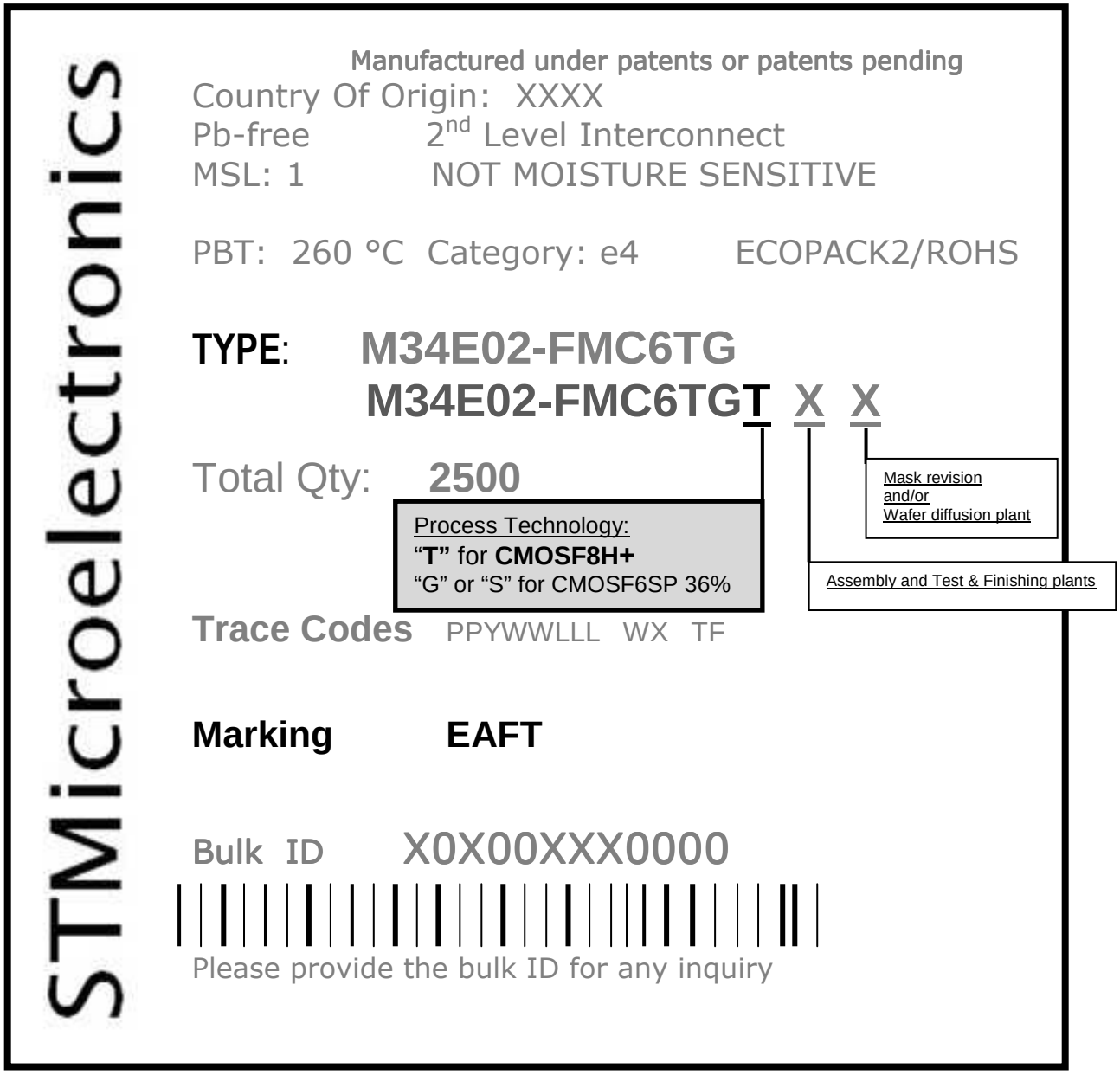
- Change on DC characteristic **$I_{CC1}$ standby supply current**
- Change on Absolute maximum rating **$V_{ESD}$ HBM**

## How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is "**T**" for the **upgraded version** in **CMOSF8H+**, this identifier being "G" or "S" for the current version in CMOSF6SP 36%.

➔ *Example for M34E02-FMC6TG*



## How can the change be seen?

### *- DEVICE MARKING*

For the **UFDFPN8** package, the difference is visible inside the product name,
M34E02-FMC6TG: **upgraded version** in **CMOSF8H+** is **EAFT**, current version is E026.

| | **Upgraded CMOSF8H+ (ST Rousset)** | Current CMOSF6SP 36% **(ST Ang Mo Kio) or GLOBALFOUNDRIES** |
|---|---|---|
| **UFDFPN8**<br>M34E02-FMC6TG | O **EAFT**<br>PYWW | O E026<br>PYWW |

For the **TSSOP8** package, the difference is visible inside the product name:
M34E02-FDW6TP: **upgraded version** in **CMOSF8H+** is **EAF6T**, current version is E02FP.

| | **Upgraded CMOSF8H+ (ST Rousset)** | Current CMOSF6SP 36% **(ST Ang Mo Kio) or GLOBALFOUNDRIES** |
|---|---|---|
| **TSSOP8**<br>M34E02-FDW6TP | O **EAF6T**<br>PYWW | O E02FP<br>PYWW |

## Appendix A- Product Change Information

| | |
|---|---|
| **Product family / Commercial products:** | M34E02 products family |
| **Customer(s):** | All |
| **Type of change:** | Wafer fab process technology change |
| **Reason for the change:** | Line up to state-of-the-art of process |
| **Description of the change:** | Redesign and upgrade to the new CMOSF8H+ Process technology. |
| **Forecast date of the change: (Notification to customer)** | Week 08 / 2013 |
| **Forecast date of Qualification samples availability for customer(s):** | - Available for UFDFPN8 package<br>- On request for TSSOP8 package |
| **Forecast date for the internal STMicroelectronics change, Qualification Report availability:** | The **Qualification Report QRMMY1209** is available and included inside this document. |
| **Marking to identify the changed product:** | Process Technology identifier "**T"** for CMOSF8H+ |
| **Description of the qualification program**: | Standard ST Microelectronics Corporate Procedures for Quality and Reliability |
| **Product Line(s) and/or Part Number(s):** | M34E02-FMC6TG<br>M34E02-FMC6TGM<br>M34E02-FDW6TP<br>M34E02-FDW1TP |
| **Manufacturing location:** | Rousset 8 inch wafer fab |
| **Estimated date of first shipment:** | Week 21 / 2013 |

## Appendix B: Qualification Report:

**See following pages**

# QRMMY1209
# Qualification report

## New design / M34E02-F
## using the CMOSF8H+ technology at the Rousset 8” Fab

**Table 1. Product information**

| General information | |
|---|---|
| **Commercial product** | M34E02-FMC6TG |
| **Product description** | 2-Kbit serial presence detect (SPD) EEPROM for double data rate (DDR1 and DDR2) DRAM modules |
| **Product group** | MMS |
| **Product division** | MMY - Memory |
| **Silicon process technology** | CMOSF8H+ |
| **Wafer fabrication location** | RS8F - ST Rousset 8”, France |
| **Electrical Wafer Sort test plant location** | ST Rousset, France<br>ST Toa Payoh, Singapore |

**Table 2. Package description**

| Package description | Assembly plant location | Final test plant location |
|---|---|---|
| UFDFPN8 (MLP8)<br>2 x 3 mm | ST Calamba, Philippines | ST Calamba, Philippines |
| | Subcon Amkor, Philippines | Subcon Amkor, Philippines |

**Reliability assessment: PASS.**

# 1 Reliability evaluation overview

## 1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M34E02-F using the CMOSF8H+ silicon process technology at the ST Rousset 8” diffusion fab.

The CMOSF8H+ is closely derived from CMOSF8H silicon process technology (already used for production of EEPROM densities ranging from 32 Kb to 2 Mb), with a more compact layout, in order to achieve a competitive die size.

The CMOSF8H+ technology is already qualified in the ST Rousset 8” fab using M24C16 as driver product.

The voltage and temperature ranges covered by this document are:

- 1.7 to 5.5 V at –40 to 85 °C

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion plant.

## 1.2 Conclusion

The new design M34E02-F using the CMOSF8H+ silicon process technology at the ST Rousset 8” diffusion fab has passed all the reliability requirements.

Refer to *Section 3: Reliability test results* for details on the test results.

# 2 Device characteristics

The M34E02-F is a 2-Kbit $I^2C$-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 256 × 8 bits.

The M34E02-F can be accessed with a supply voltage from 1.7 V to 5.5 V and operates with a clock frequency of 400 kHz (or less), over an ambient temperature range of -40 °C/+85 °C.

The M34E02-F is able to lock permanently the data in its first half (from locations 00h to 7Fh). This facility has been designed specifically for use in DRAM DIMMs (dual interline memory modules) with serial presence detect (SPD). All the information concerning the DDR1 or DDR2 configuration of the DRAM module (such as its access speed, size and organization) can be kept write-protected in the first half of the memory.

The first half of the memory area can be write-protected using two different software write-protection mechanisms. By sending the device a specific sequence, the first 128 bytes of the memory become write-protected: permanently or resettable. In addition, the devices allow the entire memory area to be write-protected, using the WC input (for example by tieing this input to $V_{CC}$).

These $I^2C$-compatible electrically erasable programmable memory (EEPROM) devices are organized as 256 × 8 bits.

$I^2C$ uses a two-wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the $I^2C$ bus definition to access the memory area and a second device type identifier code (0110) to define the protection. These codes are used together with the voltage level applied on the three chip enable inputs (E2, E1, E0).

The devices behave as slave devices in the $I^2C$ protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and RW bit (as described in the Device select code table), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the $9^{th}$ bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for WRITE, and after a NoAck for READ.

Refer to the product datasheet for more details.

# 3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The CMOSF8H+ process technology has been qualified on 3 lots using the driver product M24C16 (refer to qualification report QRMMY1126).

The M34E02-F is designed with the same architecture and technology as the driver product M24C16. Qualification of M34E02-F benefits of the family approach (1 lot).

The product vehicles used for the die qualification are presented in *Table 3*.

**Table 3. Product vehicles used for die qualification**

| Product | Silicon process technology | Wafer fabrication location | Package description | Assembly plant location |
|---|---|---|---|---|
| M24C16 | CMOSF8H+ | ST Rousset 8” | CDIP8 | Engineering assy (1) |
| M34E02-F / M24C04 (2)(3) | CMOSF8H+ | ST Rousset 8” | CDIP8 | Engineering assy (1) |

1. CDIP8 is a engineering ceramic package used only for die-oriented reliability trials.
2. Qualification on 3 lots using the driver product M24C16 - Qualification of M34E02-F benefits of the family approach (1 lot).
3. The M34E02-F product is derived from M24C04 product during test flow (same design maskset, same process technology). Consequently, M24C04 reliability results are used to qualify the named product.

The package qualifications were mainly obtained by similarity. The product vehicles used for the package qualification are presented in *Table 4*.

**Table 4. Product vehicles used for package qualification**

| Product | Silicon process technology | Wafer fabrication location | Package description | Assembly plant location |
|---|---|---|---|---|
| M24C16 (1) | CMOSF8H+ | ST Rousset 8” | UFDFPN8 (MLP8) 2 x 3 mm | ST Calamba / Subcon Amkor |

1. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24C16 are applicable to M34E02-F.

## 3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests.
- in *Table 6* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba / subcontractor Amkor package-oriented tests.

**Table 5. Die-oriented reliability test plan / result summary (CDIP8 / Engineering package)**

| Test | Test short description [1] | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Method | Conditions | Sample size / lots | Nb. of lots | Duration | Results fail / sample size | | | |
| | | | | | | M24C16 | | | M34E02/ M24C04 [2][3] |
| | | | | | | Lot 1 | Lot 2 | Lot 3 | Lot 1 |
| EDR | High temperature operating life after endurance | | | | | | | | |
| | AEC-Q100-005 | 1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V | 80 | 1 | 168 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| | | | | | 504 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| | | | | | 1008 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| | Data retention after endurance | | | | | | | | |
| | AEC-Q100-005 | 1 million E/W cycles at 25 °C then: HTSL at 150 °C | 80 | 1 | 168 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| | | | | | 504 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| | | | | | 1008 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| LTOL | Low temperature operating life | | | | | | | | |
| | JESD22-A108 | –40 °C, 6 V | 80 | 1 | 168 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| | | | | | 504 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| | | | | | 1008 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| HTSL | High temperature storage life | | | | | | | | |
| | JESD22-A103 | Retention bake at 200 °C | 80 | 1 | 168 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| | | | | | 504 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| | | | | | 1008 hrs | 0/80 | 0/80 | 0/80 | 0/80 |
| WEB | Program/erase endurance cycling + bake | | | | | | | | |
| | Internal spec. | 1 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours | 80 | 1 | 1 million cycles / 48 hrs | 0/80 [4] | 0/80 [4] | 0/80 [4] | 0/80 [4] |
| ESD HBM | Electrostatic discharge (human body model) | | | | | | | | |
| | AEC-Q100-002 JESD22-A114 | C = 100 pF, R= 1500 Ω | 27 | 1 | N/A | Pass 3000 V | Pass 3000 V | Pass 3000 V | Pass 3000 V |
| ESD MM | Electrostatic discharge (machine model) | | | | | | | | |
| | AEC-Q100-003 JESD22-A115 | C = 200 pF, R = 0 Ω | 12 | 1 | N/A | Pass 400 V | Pass 400 V | Pass 400 V | Pass 400 V |
| LU | Latch-up (current injection and overvoltage stress) | | | | | | | | |
| | AEC-Q100-004 JESD78A | At maximum operating temperature (150 °C) | 6 | 1 | N/A | Class II - Level A | Class II - Level A | Class II - Level A | Class II - Level A |

1. See *Table 7: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the driver product M24C16 - Qualification of M34E02-F benefits of the family approach (1 lot).
3. The M34E02-F products is derived from M24C04 product during test flow (same design maskset, same process technology). Consequently, M24C04 reliability results are used to qualify the named product.
4. First rejects after 10 million cycles.

**Table 6. Package-oriented reliability test plan / result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba & subcontractor Amkor)**

| Test | Test short description[1] | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Method | Conditions | Sample size / lots | Nb. of lots | Duration | Results fail / sample size | | | |
| | | | | | | M24C16 | | | M34E02 (2) |
| | | | | | | Lot 1 | Lot 2 | Lot 3 | Lot 1 |
| PC | Preconditioning: moisture sensitivity level 1 | | | | | | | | |
| | JESD22-A113 J-STD-020D | MSL1, peak temperature at 260 °C, 3 IReflow | 345 | 1 | N/A | 0/345 | 0/345 | 0/345 | - |
| THB (3) | Temperature humidity bias | | | | | | | | |
| | AEC-Q100-JESD22-A101 | 85 °C, 85% RH, bias 5.5 V | 80 | 1 | 1008 hrs | 0/80 | 0/80 | 0/80 | - |
| TC (3) | Temperature cycling | | | | | | | | |
| | AEC-Q100-JESD22-A104 | –65 °C / +150 °C | 80 | 1 | 1000 cycles | 0/80 | 0/80 | 0/80 | - |
| TMSK (3) | Thermal shocks | | | | | | | | |
| | JESD22-A106 | –55 °C / +125 °C | 25 | 1 | 200 shocks | 0/25 | 0/25 | 0/25 | - |
| AC (3) | Autoclave (pressure pot) | | | | | | | | |
| | AEC-Q100-JESD22-A102 | 121 °C, 100% RH at 2 ATM | 80 | 1 | 168 hrs | 0/80 | 0/80 | 0/80 | - |
| HTSL (3) | High temperature storage life | | | | | | | | |
| | AEC-Q100-JESD22-A103 | Retention bake at 150 °C | 80 | 1 | 1008 hrs | 0/80 | 0/80 | 0/80 | - |
| ESD CDM | Electrostatic discharge (charge device model) | | | | | | | | |
| | AEC-Q100-011 JESD22-C101 | Field induced charging method | 18 | 1 | N/A | PASS > 1500V | - | - | Results FC W07 |

1. See *Table 7: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab - Package qualification results of M24C16 are applicable to M34E02-F.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

# 4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

# 5 Glossary

**Table 7. List of terms**

| Terms | Description |
|---|---|
| **EDR** | NVM endurance, data retention and operational life |
| **HTOL** | High temperature operating life |
| **LTOL** | Low temperature operating life |
| **HTB** | High temperature bake |
| **WEB** | Program/Erase endurance cycling + bake |
| **ESD HBM** | Electrostatic discharge (human body model) |
| **ESD MM** | Electrostatic discharge (machine model) |
| **LU** | Latch-up |
| **PC** | Preconditioning (solder simulation) |
| **THB** | Temperature humidity bias |
| **TC** | Temperature cycling |
| **TMSK** | Thermal shocks |
| **AC** | Autoclave (pressure pot) |
| **HTSL** | High temperature storage life |
| **ELFR** | Early life failure rate |
| **ESD CDM** | Electrostatic discharge (charge device model) |

# 6 Revision history

**Table 8. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 31-Jan-2013 | 1 | Initial release. |

## Document Revision History

| Date | Rev. | Description of the Revision |
|---|---|---|
| February 08, 2013 | 1.00 | First draft creation |
| | | |
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## Source Documents & Reference Documents

| **Source document Title** | **Rev.:** | **Date:** |
|---|---|---|
| | | |
| | | |
| | | |

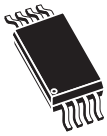
# M34E02
# M34E02-F

## 2 Kbit serial presence detect (SPD) EEPROM for double data rate (DDR1 and DDR2) DRAM modules

## Features

- 2 Kbit EEPROM for DDR1 and DDR2 serial presence detect
- Backward compatible with the M34C02
- Permanent and reversible software data protection for lower 128 bytes
- 100 kHz and 400 kHz $I^2C$ bus serial interface
- Single supply voltage:
  - 1.7 V to 5.5 V
- Byte and Page Write (up to 16 bytes)
- Self-timed write cycle
- Noise filtering
  - Schmitt trigger on bus inputs
  - Noise filter on bus inputs
- Enhanced ESD/latch-up protection
- More than 1 million erase/write cycles
- More than 40 years' data retention
- ECOPACK® (RoHS compliant) packages
- Packages:
  - ECOPACK2® (RoHS-compliant and Halogen-free)

UFDFPN8 (MB or MC)
2 x 3 mm



TSSOP8 (DW)
4.4 × 3 mm

# Contents

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# 1 Description

The M34E02 and M34E02-F are 2 Kbit serial EEPROM memories able to lock permanently the data in its first half (from location 00h to 7Fh). This facility has been designed specifically for use in DRAM DIMMs (dual interline memory modules) with serial presence detect (SPD). All the information concerning the DDR1 or DDR2 configuration of the DRAM module (such as its access speed, size and organization) can be kept write-protected in the first half of the memory.

The first half of the memory area can be write-protected using two different software write protection mechanisms. By sending the device a specific sequence, the first 128 bytes of the memory become write protected: permanently or resettable. In addition, the devices allow the entire memory area to be write protected, using the $\overline{WC}$ input (for example by tieing this input to $V_{CC}$).

These $I^2C$-compatible electrically erasable programmable memory (EEPROM) devices are organized as 256 × 8 bits.

$I^2C$ uses a two wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the $I^2C$ bus definition to access the memory area and a second device type identifier code (0110) to define the protection. These codes are used together with the voltage level applied on the three chip enable inputs (E2, E1, E0).

The devices behave as a slave device in the $I^2C$ protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and $R\overline{W}$ bit (as described in the Device select code table), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the $9^{th}$ bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for WRITE, and after a NoAck for READ.

**Figure 1. Logic diagram**

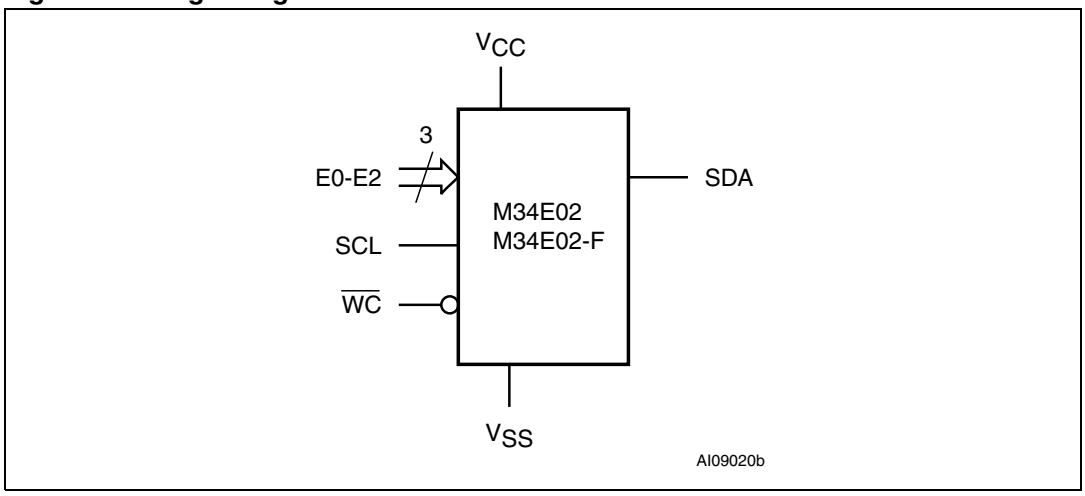
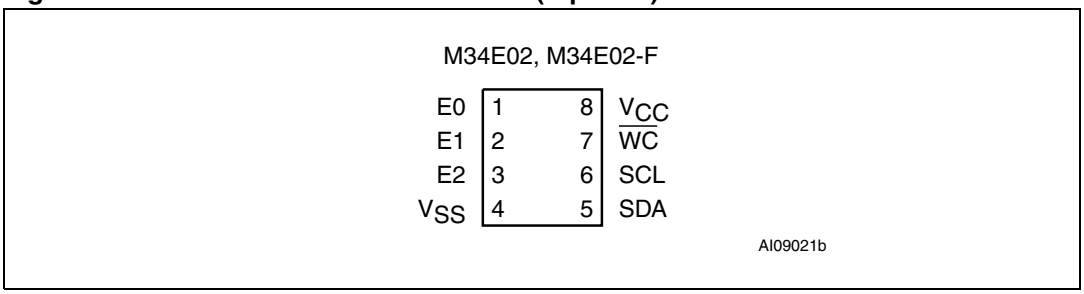


**Figure 2. TSSOP and MLP connections (top view)**




1. See the *Package mechanical data* section for package dimensions, and how to identify pin-1.

**Table 1. Signal names**

| Signal names | Description |
|---|---|
| E0, E1, E2 | Chip Enable |
| SDA | Serial Data |
| SCL | Serial Clock |
| $\overline{WC}$ | Write Control |
| $V_{CC}$ | Supply voltage |
| $V_{SS}$ | Ground |

# 2 Signal description

## 2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to $V_{CC}$. (*Figure 4* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

## 2.2 Serial Data (SDA)

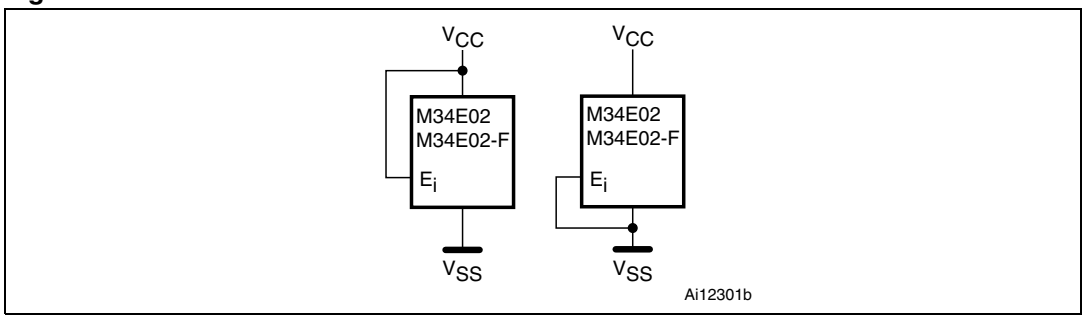
This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to $V_{CC}$. (*Figure 4* indicates how the value of the pull-up resistor can be calculated).

## 2.3 Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. In the end application, E0, E1 and E2 must be directly (not through a pull-up or pull-down resistor) connected to $V_{CC}$ or $V_{SS}$ to establish the device select code. When these inputs are not connected, an internal pull-down circuitry makes (E0,E1,E2) = (0,0,0).

The E0 input is used to detect the $V_{HV}$ voltage, when decoding an SWP or CWP instruction.

**Figure 3. Device select code**




## 2.4 Write Control ($\overline{WC}$)

This input signal is provided for protecting the contents of the whole memory from inadvertent write operations. Write Control ($\overline{WC}$) is used to enable (when driven low) or disable (when driven high) write instructions to the entire memory area or to the Protection Register.

When Write Control ($\overline{WC}$) is tied low or left unconnected, the write protection of the first half of the memory is determined by the status of the Protection Register.

## 2.5 Supply voltage ($V_{CC}$)

### 2.5.1 Operating supply voltage $V_{CC}$

Prior to selecting the memory and issuing instructions to it, a valid and stable $V_{CC}$ voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range must be applied (see *Table 8*). In order to secure a stable DC supply voltage, it is recommended to decouple the $V_{CC}$ line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the $V_{CC}$/$V_{SS}$ package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle ($t_W$).

### 2.5.2 Power-up conditions

The $V_{CC}$ voltage has to rise continuously from 0 V up to the minimum $V_{CC}$ operating voltage defined in *Table 8* and the rise time must not vary faster than 1 V/µs.

### 2.5.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on reset (POR) circuit is included. At power-up, the device does not respond to any instruction until $V_{CC}$ reaches the internal reset threshold voltage (this threshold is lower than the minimum $V_{CC}$ operating voltage defined in *Table 8*).

When $V_{CC}$ passes over the POR threshold, the device is reset and enters the Standby Power mode. However, the device must not be accessed until $V_{CC}$ reaches a valid and stable $V_{CC}$ voltage within the specified [$V_{CC}$(min), $V_{CC}$(max)] range.

In a similar way, during power-down (continuous decrease in $V_{CC}$), as soon as $V_{CC}$ drops below the power-on reset threshold voltage, the device stops responding to any instruction sent to it.

### 2.5.4 Power-down conditions

During power-down (continuous decrease in $V_{CC}$), the device must be in Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

**Figure 4. Maximum $R_P$ value versus bus parasitic capacitance (C) for an $I^2C$ bus**

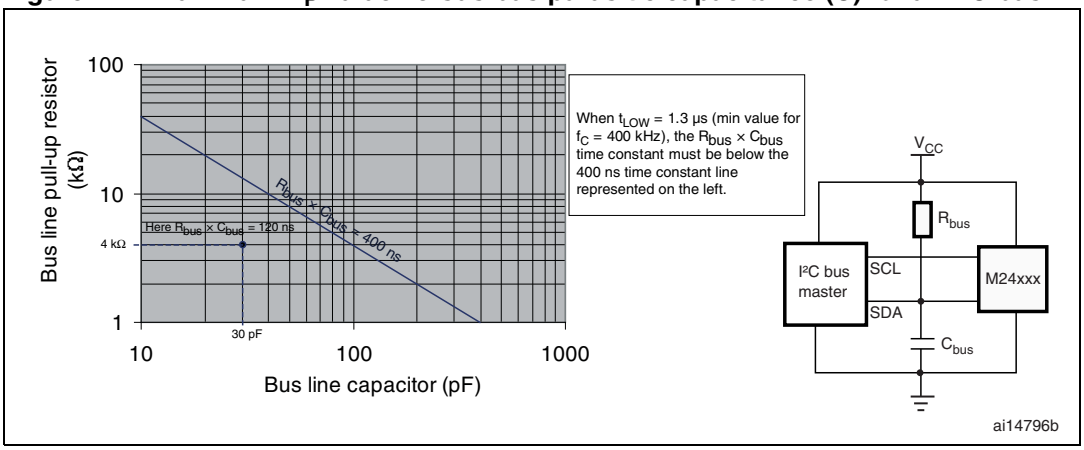


**Figure 5. $I^2C$ bus protocol**

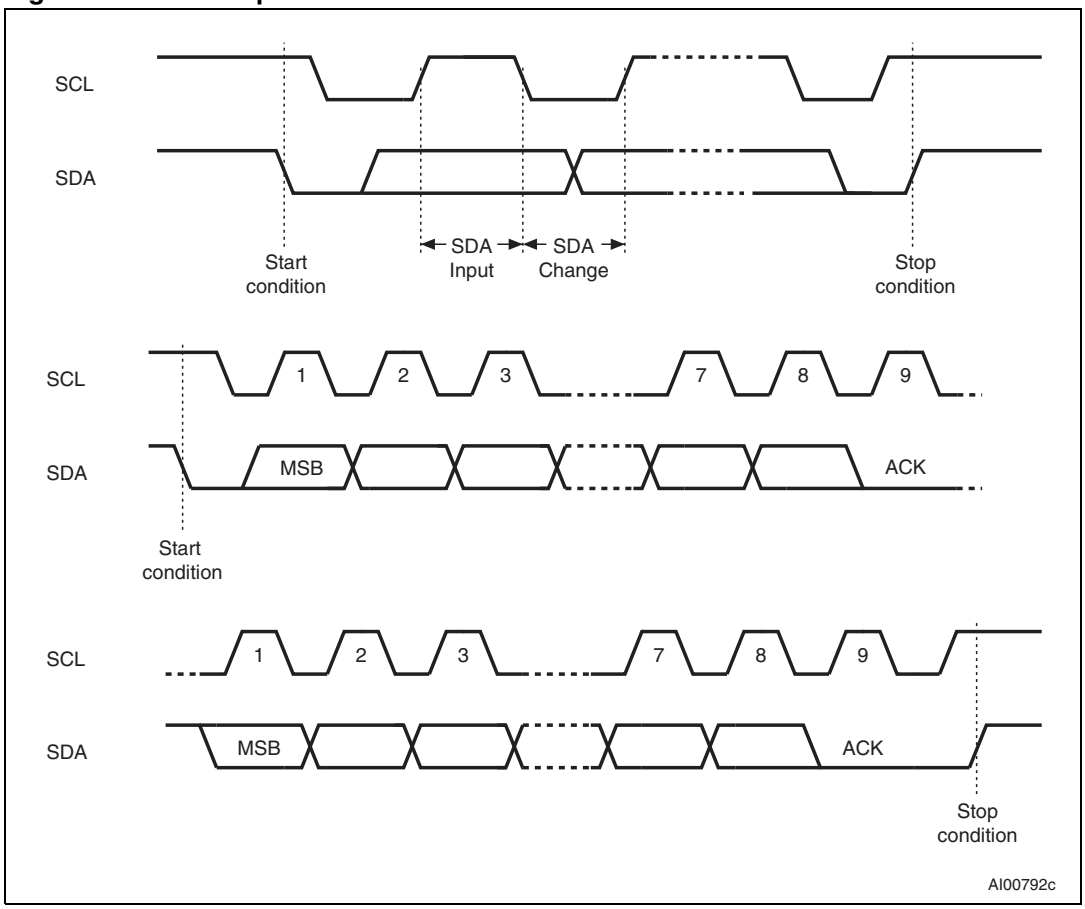



**Table 2. Device select code**

| | Chip Enable signals | | | Device type identifier | | | | Chip Enable bits | | | RW |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | b7(1) | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| Memory area select code (two arrays)(2) | E2 | E1 | E0 | 1 | 0 | 1 | 0 | E2 | E1 | E0 | RW |
| Set write protection (SWP) | $V_{SS}$ | $V_{SS}$ | $V_{HV}$(3) | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| Clear write protection (CWP) | $V_{SS}$ | $V_{CC}$ | $V_{HV}$(3) | | | | | 0 | 1 | 1 | 0 |
| Permanently set write protection (PSWP)(2) | E2 | E1 | E0 | | | | | E2 | E1 | E0 | 0 |
| Read SWP | $V_{SS}$ | $V_{SS}$ | $V_{HV}$(3) | | | | | 0 | 0 | 1 | 1 |
| Read CWP | $V_{SS}$ | $V_{CC}$ | $V_{HV}$(3) | | | | | 0 | 1 | 1 | 1 |
| Read PSWP(2) | E2 | E1 | E0 | | | | | E2 | E1 | E0 | 1 |

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.
3. $V_{HV}$ is defined in *Table 13*.

# 3 Device operation

The device supports the $I^2C$ protocol. This is summarized in *Figure 5* Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The memory device is always a slave in all communication.

## 3.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

## 3.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

## 3.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the $9^{th}$ clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

## 3.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

## 3.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

The device select code consists of a 4-bit device type identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit device type identifier is 1010b; to access the write-protection settings, it is 0110b.

Up to eight memory devices can be connected on a single $I^2C$ bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the device select code is received, the device only responds if the Chip Enable address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8$^{th}$ bit is the Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$). This bit is set to 1 for Read and 0 for Write operations.

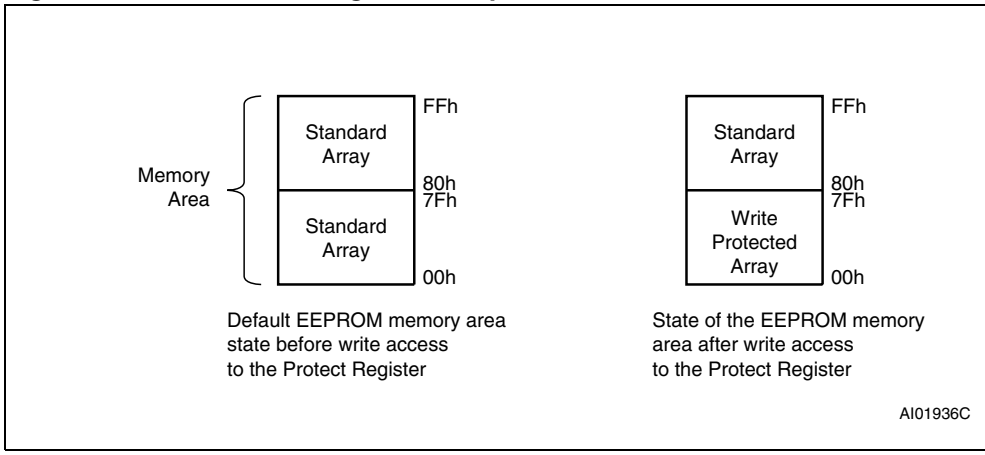
If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9$^{th}$ bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

**Table 3. Operating modes**

| Mode | $\overline{\text{RW}}$ bit | $\overline{\text{WC}}$(1) | Bytes | Initial Sequence |
|---|---|---|---|---|
| Current Address Read | 1 | X | 1 | Start, Device Select, $\overline{\text{RW}}$ = 1 |
| Random Address Read | 0 | X | 1 | Start, Device Select, $\overline{\text{RW}}$ = 0, Address |
| | 1 | X | | reStart, Device Select, $\overline{\text{RW}}$ = 1 |
| Sequential Read | 1 | X | ≥ 1 | Similar to Current or Random Address Read |
| Byte Write | 0 | $V_{IL}$ | 1 | Start, Device Select, $\overline{\text{RW}}$ = 0 |
| Page Write | 0 | $V_{IL}$ | ≤16 | Start, Device Select, $\overline{\text{RW}}$ = 0 |

1. X = $V_{IH}$ or $V_{IL}$.

**Figure 6. Result of setting the write protection**



## 3.6 Setting the write-protection

The M34E02 and M34E02-F have a hardware write-protection feature, using the Write Control ($\overline{WC}$) signal. This signal can be driven high or low, and must be held constant for the whole instruction sequence. When Write Control ($\overline{WC}$) is held high, the whole memory array (addresses 00h to FFh) is write protected. When Write Control ($\overline{WC}$) is held low, the write protection of the memory array is dependent on whether software write-protection has been set.

Software write-protection allows the bottom half of the memory area (addresses 00h to 7Fh) to be write protected irrespective of subsequent states of the Write Control ($\overline{WC}$) signal.

Software write-protection is handled by three instructions:

- SWP: Set Write Protection
- CWP: Clear Write Protection
- PSWP: Permanently Set Write Protection

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

### 3.6.1 SWP and CWP

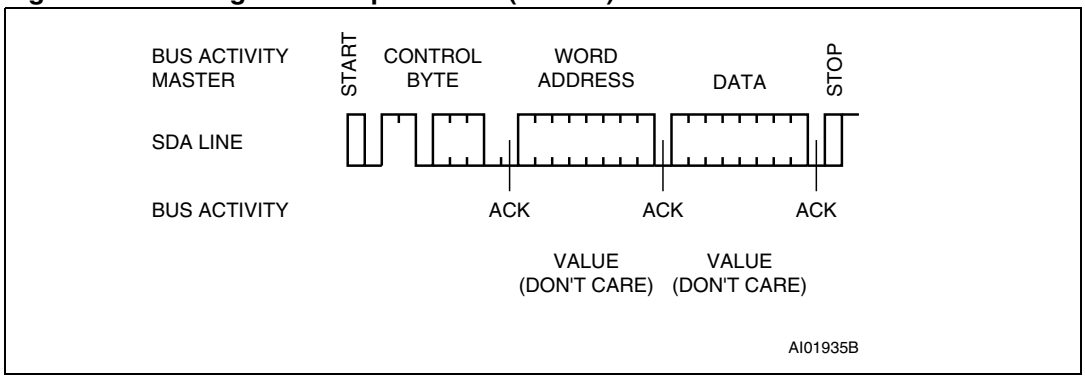
If the software write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction.

The two instructions (SWP and CWP) have the same format as a Byte Write instruction, but with a different device type identifier (as shown in *Table 2*). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all “Don’t Care” (*Figure 7*). Another difference is that the voltage, $V_{HV}$, must be applied on the E0 pin, and specific logical levels must be applied on the other two (E1 and E2, as shown in *Table 2*).

### 3.6.2 PSWP

If the software write-protection has been set with the PSWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device, and regardless the state of Write Control ($\overline{WC}$). Also, once the PSWP instruction has been successfully executed, the M34E02 and M34E02-F no longer acknowledge any instruction (with a device type identifier of 0110) to access the write-protection settings.

**Figure 7. Setting the write protection ($\overline{WC}$ = 0)**



## 3.7 Write operations

Following a Start condition the bus master sends a device select code with the R$\overline{W}$ bit reset to 0. The device acknowledges this, as shown in *Figure 8*, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "$10^{th}$ bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

### 3.7.1 Byte Write

After the device select code and the address byte, the bus master sends one data byte. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 8*

### 3.7.2 Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is low. If the addressed location is hardware write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

**Figure 8. Write mode sequences in a non write-protected area**

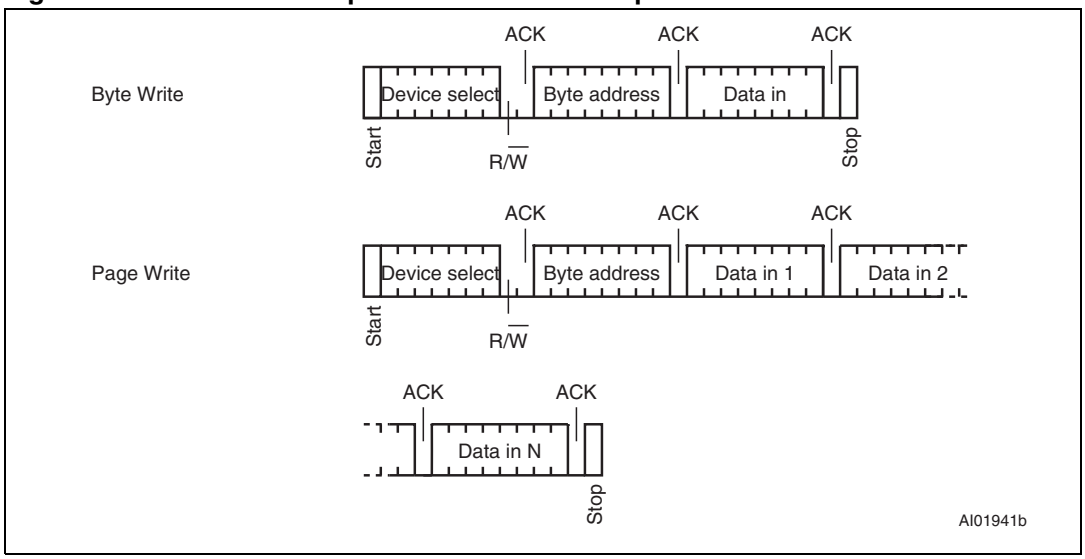
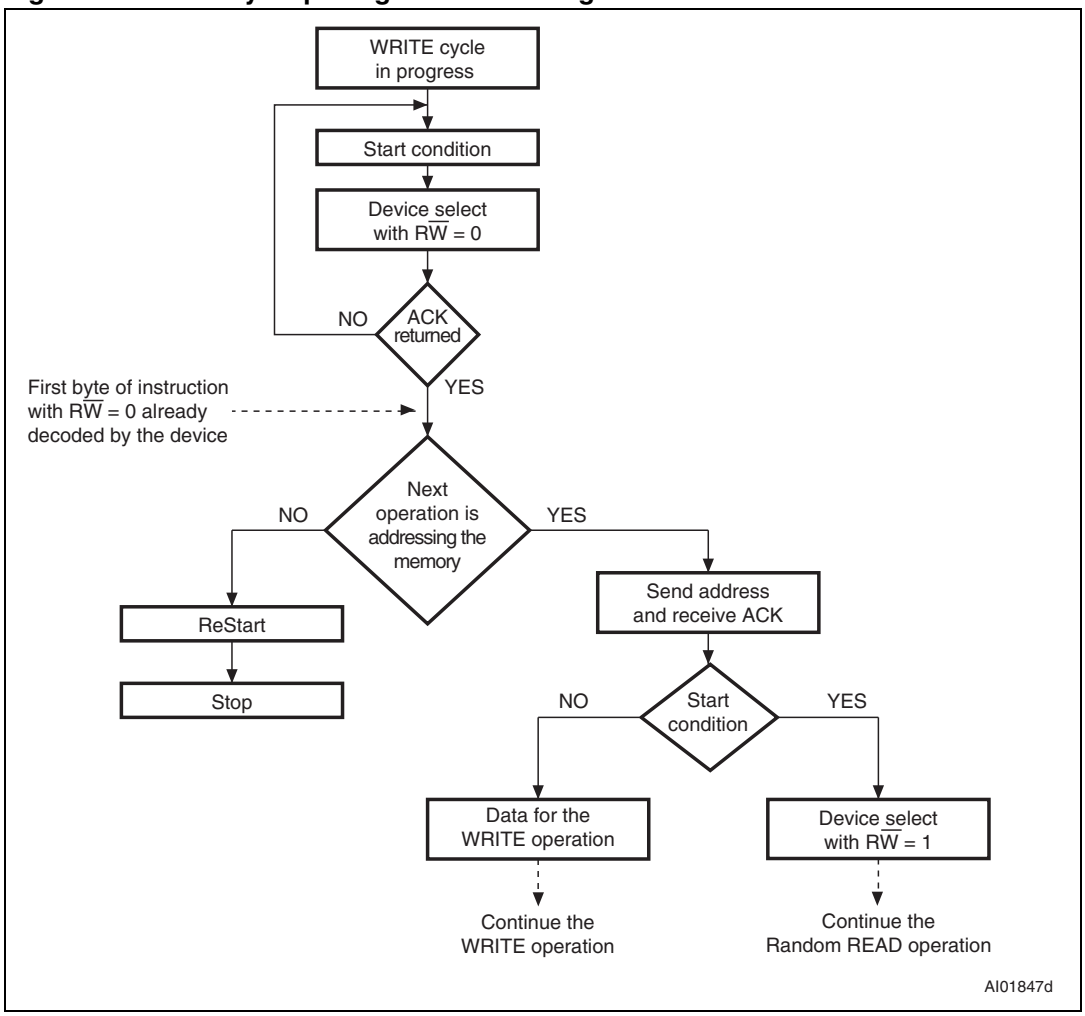



**Figure 9. Write cycle polling flowchart using ACK**



### 3.7.3 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time ($t_w$) is shown in *Table 14*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 9*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

## 3.8 Read operations

Read operations are performed independently of whether hardware or software protection has been set.

The device has an internal address counter which is incremented each time a byte is read.

### 3.8.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 10*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

### 3.8.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 10*, *without* acknowledging the byte.

### 3.8.3 Sequential Read

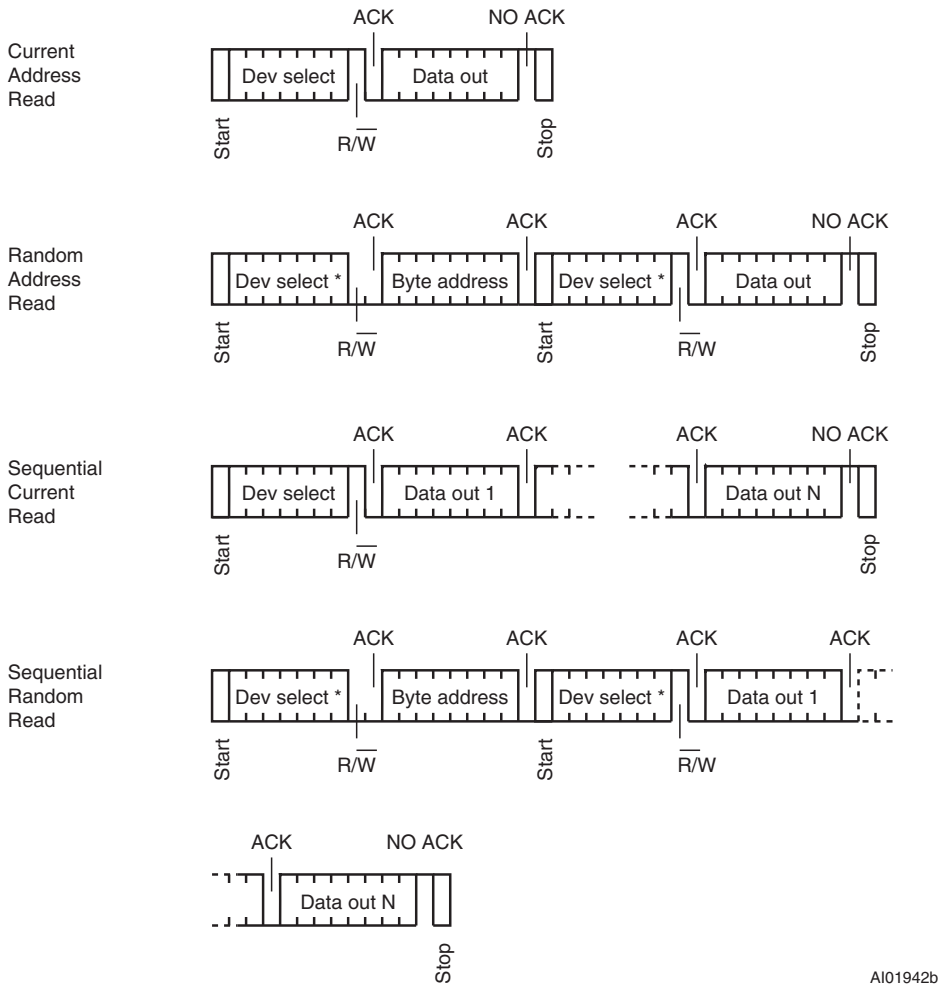
This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 10*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

### 3.8.4 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

**Figure 10. Read mode sequences**




1. The seven most significant bits of the device select code of a Random Read (in the 1st and 3rd bytes) must be identical.

# 4 Initial delivery state

The device is delivered with all bits in the memory array set to '1' (each Byte contains FFh).

# 5 Use within a DDR1/DDR2 DRAM module

In the application, the M34E02/M34E02-F is soldered directly in the printed circuit module. The three Chip Enable inputs (E0, E1, E2) must be connected to $V_{SS}$ or $V_{CC}$ directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (see *Table 4*). The pull-up resistors needed for normal behavior of the $I^2C$ bus are connected on the $I^2C$ bus of the mother-board (as shown in *Figure 11*).

The Write Control ($\overline{WC}$) of the M34E02/M34E02-F can be left unconnected. However, connecting it to $V_{SS}$ is recommended, to maintain full read and write access.

**Table 4. DRAM DIMM connections**

| DIMM position | E2 | E1 | E0 |
|---|---|---|---|
| 0 | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ |
| 1 | $V_{SS}$ | $V_{SS}$ | $V_{CC}$ |
| 2 | $V_{SS}$ | $V_{CC}$ | $V_{SS}$ |
| 3 | $V_{SS}$ | $V_{CC}$ | $V_{CC}$ |
| 4 | $V_{CC}$ | $V_{SS}$ | $V_{SS}$ |
| 5 | $V_{CC}$ | $V_{SS}$ | $V_{CC}$ |
| 6 | $V_{CC}$ | $V_{CC}$ | $V_{SS}$ |
| 7 | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |

## 5.1 Programming the M34E02 and M34E02-F

The situations in which the M34E02 and M34E02-F are programmed can be considered under two headings:

- when the DDR2 DRAM is isolated (not inserted on the PCB motherboard)
- when the DDR2 DRAM is inserted on the PCB motherboard

### 5.1.1 Isolated DRAM module

With specific programming equipment, it is possible to define the M34E02/M34E02-F content, using Byte and Page Write instructions, and its write-protection using the SWP and CWP instructions. To issue the SWP and CWP instructions, the DRAM module must be inserted in a specific slot where the E0 signal can be driven to $V_{HV}$ during the whole instruction. This programming step is mainly intended for use by DRAM module makers, whose end application manufacturers will want to clear this write-protection with the CWP on their own specific programming equipment, to modify the lower 128 Bytes, and finally to set permanently the write-protection with the PSWP instruction.

### 5.1.2 DRAM module inserted in the application motherboard

As the final application cannot drive the E0 pin to $V_{HV}$, the only possible action is to freeze the write-protection with the PSWP instruction.

*Table 5* and *Table 6* show how the Ack bits can be used to identify the write-protection status.

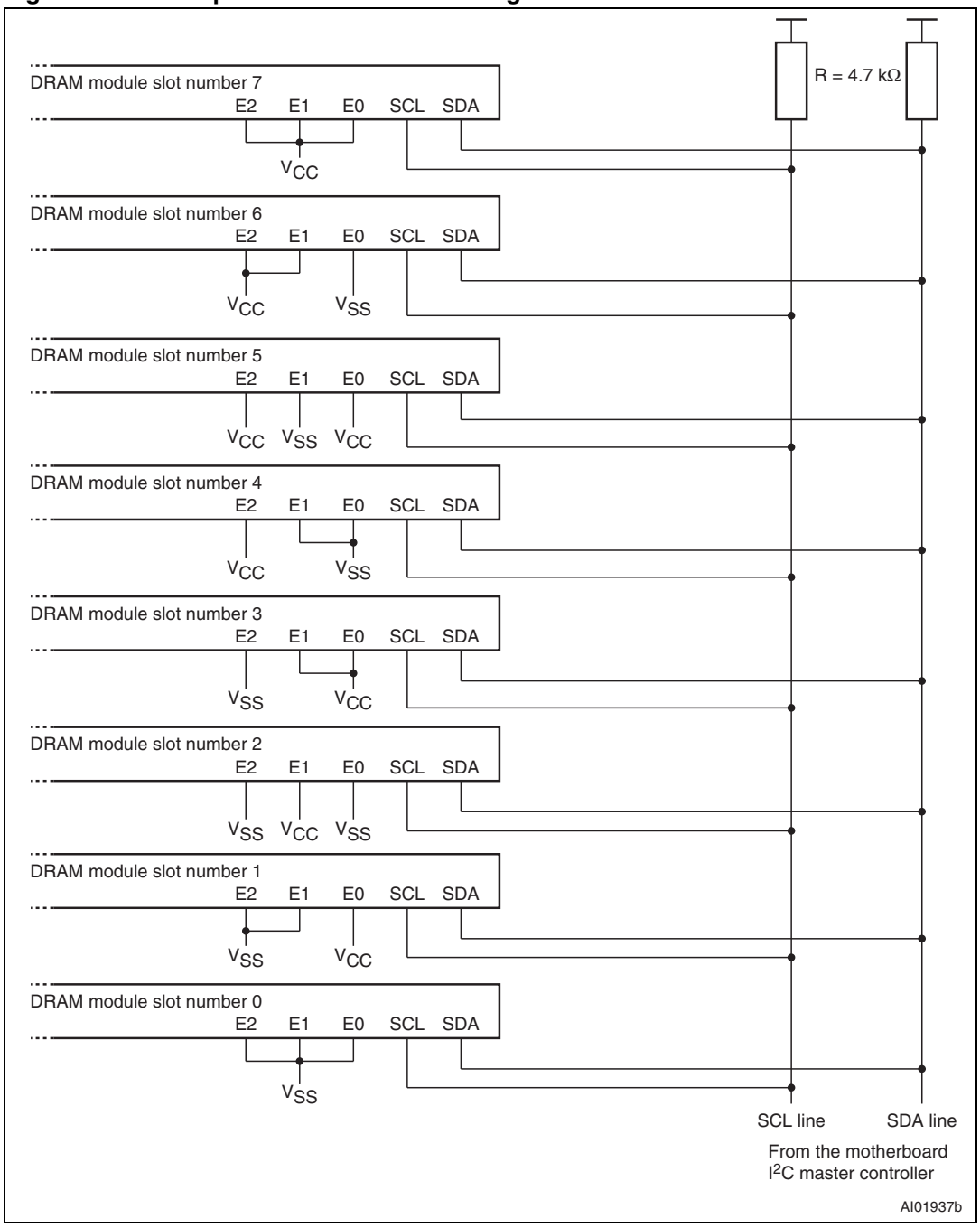
**Table 5. Acknowledge when writing data or defining the write-protection (instructions with R/W bit = 0)**

| Status | $\overline{WC}$ input level | Instruction | Ack | Address | Ack | Data byte | Ack | Write cycle ($t_W$) |
|---|---|---|---|---|---|---|---|---|
| Permanently protected | X | PSWP, SWP or CWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | | Page or Byte Write in lower 128 bytes | Ack | Address | Ack | Data | NoAck | No |
| Protected with SWP | 0 | SWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | | CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | | PSWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | | Page or Byte Write in lower 128 bytes | Ack | Address | Ack | Data | NoAck | No |
| | 1 | SWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | | CWP | Ack | Not significant | Ack | Not significant | NoAck | No |
| | | PSWP | Ack | Not significant | Ack | Not significant | NoAck | No |
| | | Page or Byte Write | Ack | Address | Ack | Data | NoAck | No |
| Not Protected | 0 | PSWP, SWP or CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | | Page or Byte Write | Ack | Address | Ack | Data | Ack | Yes |
| | 1 | PSWP, SWP or CWP | Ack | Not significant | Ack | Not significant | NoAck | No |
| | | Page or Byte Write | Ack | Address | Ack | Data | NoAck | No |

**Table 6. Acknowledge when reading the write protection (instructions with R/W bit = 1)**

| Status | Instruction | Ack | Address | Ack | Data byte | Ack |
|---|---|---|---|---|---|---|
| Permanently protected | PSWP, SWP or CWP | NoAck | Not significant | NoAck | Not significant | NoAck |
| Protected with SWP | SWP | NoAck | Not significant | NoAck | Not significant | NoAck |
| | CWP | Ack | Not significant | NoAck | Not significant | NoAck |
| | PSWP | Ack | Not significant | NoAck | Not significant | NoAck |
| Not protected | PSWP, SWP or CWP | Ack | Not significant | NoAck | Not significant | NoAck |

**Figure 11. Serial presence detect block diagram**




1. E0, E1 and E2 are wired at each DRAM module slot in a binary sequence for a maximum of 8 devices.
2. Common clock and common data are shared across all the devices.

# 6 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 7. Absolute maximum ratings**

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| | Ambient temperature with power applied | | –55 | 130 | °C |
| $T_{STG}$ | Storage temperature | | –65 | 150 | °C |
| $V_{IO}$ | Input or output range | E0<br>Others | –0.50<br>–0.50 | 10.0<br>6.5 | V |
| $I_{OL}$ | DC output current (SDA = 0) | | - | 5 | mA |
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_{ESD}$ | Electrostatic discharge voltage (human body model)(1) | | –4000 | 4000 | V |

1. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

# 7 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

**Table 8. Operating conditions (for temperature range 1 devices)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 1.7 | 3.6 | V |
| $T_A$ | Ambient operating temperature | 0 | 70 | °C |

**Table 9. Operating conditions (for temperature range 6 devices)**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 1.7 | 5.5 | V |
| $T_A$ | Ambient operating temperature | –40 | +85 | °C |

**Table 10. AC measurement conditions**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_L$ | Load capacitance | 100 | | pF |
| | SCL input rise and fall time, SDA input fall time | | 50 | ns |
| | Input levels | $0.2V_{CC}$ to $0.8V_{CC}$ | | V |
| | Input and output timing reference levels | $0.3V_{CC}$ to $0.7V_{CC}$ | | V |

**Figure 12. AC measurement I/O waveform**

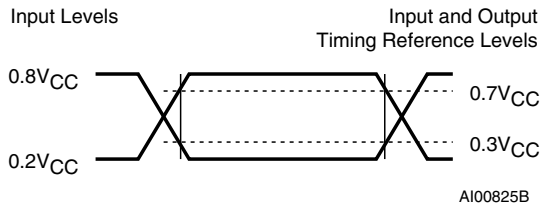


**Table 11. Input parameters**

| Symbol | Parameter[1] | Test condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance (SDA) | | | 8 | pF |
| $C_{IN}$ | Input capacitance (other pins) | | | 6 | pF |
| $Z_{EiL}$ | Ei (E0, E1, E2) input impedance | $V_{IN} < 0.3V_{CC}$ | 30 | | kΩ |
| $Z_{EiH}$ | Ei (E0, E1, E2) input impedance | $V_{IN} > 0.7V_{CC}$ | 800 | | kΩ |
| $Z_{WCL}$ | $\overline{WC}$ input impedance | $V_{IN} < 0.3V_{CC}$ | 5 | | kΩ |
| $Z_{WCH}$ | $\overline{WC}$ input impedance | $V_{IN} > 0.7V_{CC}$ | 500 | | kΩ |
| $t_{NS}$ | Pulse width ignored (input filter on SCL and SDA) | | | 100 | ns |

1. Characterized, not tested in production.

**Table 12. DC characteristics (for temperature range 1 devices)**

| Symbol | Parameter | Test condition (in addition to those in *Table 8*) | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current (SCL, SDA) | $V_{IN} = V_{SS}$ or $V_{CC}$ | | ± 2 | µA |
| $I_{LO}$ | Output leakage current | SDA in Hi-Z, external voltage applied on SDA: $V_{SS}$ or $V_{CC}$ | | ± 2 | µA |
| $I_{CC}$ | Supply current (read) | $V_{CC}$ = 1.7 V, $f_c$ = 100 kHz | | 1 | mA |
| | | $V_{CC}$ = 3.6 V, $f_c$ = 100 kHz | | 2 | mA |
| $I_{CC1}$ | Standby supply current | Device not selected[1], $V_{IN} = V_{SS}$ or $V_{CC}$, $V_{CC}$ = 3.6 V | | 2 | µA |
| | | Device not selected[1], $V_{IN} = V_{SS}$ or $V_{CC}$, $V_{CC}$ = 1.7 V | | 1 | µA |
| $V_{IL}$ | Input low voltage (SCL, SDA, $\overline{WC}$) | 2.5 ≤ $V_{CC}$ | –0.45 | 0.3 $V_{CC}$ | V |
| | | 1.7 V ≤ $V_{CC}$ < 2.5 V | –0.45 | 0.25$V_{CC}$ | V |
| $V_{IH}$ | Input high voltage (SCL, SDA, $\overline{WC}$) | | 0.7$V_{CC}$ | $V_{CC}$+1 | V |
| $V_{HV}$ | E0 high voltage | $V_{HV} - V_{CC} \geq 4.8$ V | 7 | 10 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 2.1 mA, 2.2 V ≤ $V_{CC}$ ≤ 3.6 V | | 0.4 | V |
| | | $I_{OL}$ = 0.7 mA, $V_{CC}$ = 1.7 V | | 0.2 | V |

1. The device is not selected after a power-up, after a read command (after the Stop condition), or after the completion of the internal write cycle $t_W$ ($t_W$ is triggered by the correct decoding of a write command).

**Table 13. DC characteristics (for temperature range 6 devices)**

| Symbol | Parameter | Test condition (in addition to those in *Table 9*) | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current (SCL, SDA) | $V_{IN} = V_{SS}$ or $V_{CC}$ | | ± 2 | µA |
| $I_{LO}$ | Output leakage current | SDA in Hi-Z, external voltage applied on SDA: $V_{SS}$ or $V_{CC}$ | | ± 2 | µA |
| $I_{CC}$ | Supply current (read) | $V_{CC} < 2.5$ V, $f_c = 400$ kHz | | 1 | mA |
| | | $V_{CC} \geq 2.5$ V, $f_c = 400$ kHz | | 3 | mA |
| $I_{CC1}$ | Standby supply current | Device not selected(1), $V_{IN} = V_{SS}$ or $V_{CC}$, $V_{CC} \geq 2.5$ V | | 2 | µA |
| | | Device not selected(1), $V_{IN} = V_{SS}$ or $V_{CC}$, $V_{CC} < 2.5$ V | | 1 | µA |
| $V_{IL}$ | Input low voltage (SCL, SDA, $\overline{WC}$) | $2.5 \leq V_{CC}$ | –0.45 | $0.3\ V_{CC}$ | V |
| | | $1.8\ V \leq V_{CC} < 2.5$ V | –0.45 | $0.25 V_{CC}$ | V |
| $V_{IH}$ | Input high voltage (SCL, SDA, $\overline{WC}$) | | $0.7 V_{CC}$ | $V_{CC}+1$ | V |
| $V_{HV}$ | E0 high voltage | $V_{HV} - V_{CC} \geq 4.8$ V | 7 | 10 | V |
| $V_{OL}$ | Output low voltage | $I_{OL} = 3.0$ mA, $V_{CC} = 5.5$ V | | 0.4 | V |
| | | $I_{OL} = 2.1$ mA, $V_{CC} = 2.5$ V | | 0.4 | V |
| | | $I_{OL} = 0.7$ mA, $V_{CC} = 1.7$ V | | 0.2 | V |

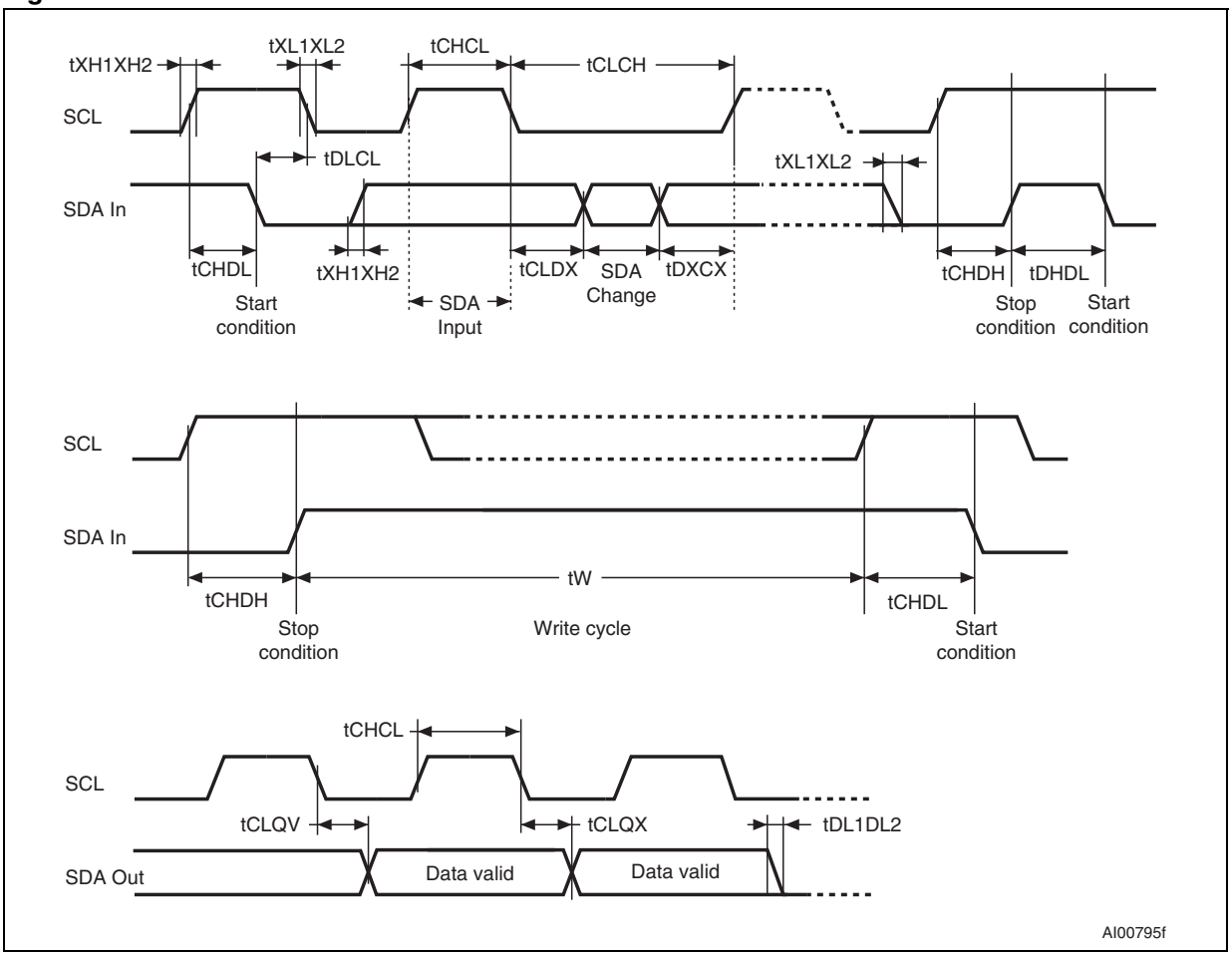
1. The device is not selected after a power-up, after a read command (after the Stop condition), or after the completion of the internal write cycle $t_W$ ($t_W$ is triggered by the correct decoding of a write command).

**Table 14. AC characteristics**

| Test conditions specified in *Table 10*, *Table 8* and *Table 9* | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Alt.** | **Parameter** | **Min.** | **Max.** | **Unit** |
| $f_C$ | $f_{SCL}$ | Clock frequency | | 400 | kHz |
| $t_{CHCL}$ | $t_{HIGH}$ | Clock pulse width high | 600 | | ns |
| $t_{CLCH}$ | $t_{LOW}$ | Clock pulse width low | 1300 | | ns |
| $t_{DL1DL2}$(1) | $t_F$ | SDA (out) fall time | 20 | 100 | ns |
| $t_{XH1XH2}$(2) | $t_R$ | Input signal rise time | 20 | 300 | ns |
| $t_{XL1XL2}$(2) | $t_F$ | Input signal fall time | 20 | 300 | ns |
| $t_{DXCX}$ | $t_{SU:DAT}$ | Data in set up time | 100 | | ns |
| $t_{CLDX}$ | $t_{HD:DAT}$ | Data in hold time | 0 | | ns |
| $t_{CLQX}$ | $t_{DH}$ | Data out hold time | 200 | | ns |
| $t_{CLQV}$(3)(4) | $t_{AA}$ | Clock low to next data valid (access time) | 200 | 900 | ns |
| $t_{CHDL}$(5) | $t_{SU:STA}$ | Start condition setup time | 600 | | ns |
| $t_{DLCL}$ | $t_{HD:STA}$ | Start condition hold time | 600 | | ns |
| $t_{CHDH}$ | $t_{SU:STO}$ | Stop condition setup time | 600 | | ns |
| $t_{DHDL}$ | $t_{BUF}$ | Time between Stop condition and next Start condition | 1300 | | ns |
| $t_W$ | $t_{WR}$ | Write time | | 5 | ms |

1. Sampled only, not 100% tested.
2. Values recommended by I²C-bus/Fast-Mode specification.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. $t_{CLQV}$ is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that the $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 4)*.
5. For a re-Start condition, or following a Write cycle.

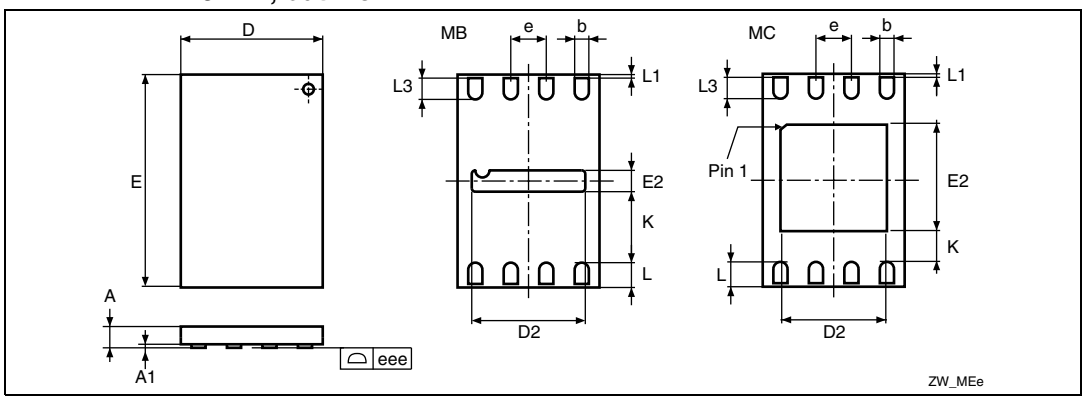
**Figure 13. AC waveforms**



# 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Figure 14. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, outline**



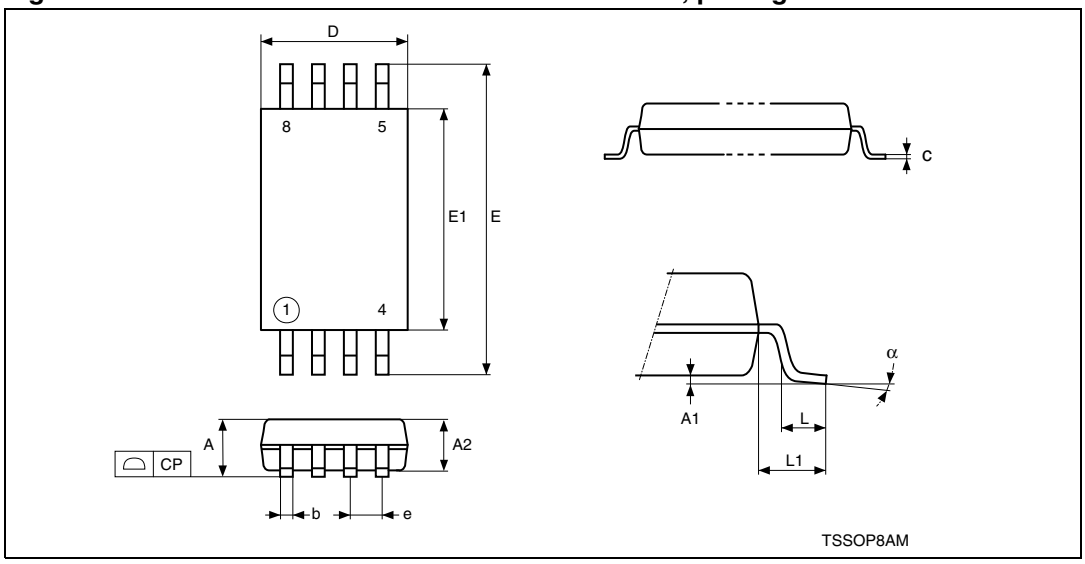

1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is pulled, internally, to $V_{SS}$. It must not be allowed to be connected to any other voltage or signal line on the PCB, for example during the soldering process.
3. The circle in the top view of the package indicates the position of pin 1.

**Table 15. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | 0.550 | 0.450 | 0.600 | 0.0217 | 0.0177 | 0.0236 |
| A1 | 0.020 | 0.000 | 0.050 | 0.0008 | 0.0000 | 0.0020 |
| b | 0.250 | 0.200 | 0.300 | 0.0098 | 0.0079 | 0.0118 |
| D | 2.000 | 1.900 | 2.100 | 0.0787 | 0.0748 | 0.0827 |
| D2 (rev MB) | 1.600 | 1.500 | 1.700 | 0.0630 | 0.0591 | 0.0669 |
| D2 (rev MC) | | 1.200 | 1.600 | | 0.0472 | 0.0630 |
| E | 3.000 | 2.900 | 3.100 | 0.1181 | 0.1142 | 0.1220 |
| E2 (rev MB) | 0.200 | 0.100 | 0.300 | 0.0079 | 0.0039 | 0.0118 |
| E2 (rev MC) | | 1.200 | 1.600 | | 0.0472 | 0.0630 |
| e | 0.500 | | | 0.0197 | | |
| K (rev MB) | | 0.800 | | | 0.0315 | |
| K (rev MC) | | 0.300 | | | 0.0118 | |
| L (rev MB) | 0.450 | 0.400 | 0.500 | 0.0177 | 0.0157 | 0.0197 |
| L (rev MC) | | 0.300 | 0.500 | | 0.0118 | 0.0197 |
| L1 | | | 0.150 | | | 0.0059 |
| L3 | | 0.300 | | | 0.0118 | |
| eee[2] | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

**Figure 15. TSSOP8 – 8-lead thin shrink small outline, package outline**




1. Drawing is not to scale.
2. The circle around the number 1 in the top view of the package indicates the position of pin 1. The numbers 4, 5 and 8 indicate the positions of pins 4, 5 and 8, respectively.

**Table 16. TSSOP8 – 8-lead thin shrink small outline, package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | | | 1.200 | | | 0.0472 |
| A1 | | 0.050 | 0.150 | | 0.0020 | 0.0059 |
| A2 | 1.000 | 0.800 | 1.050 | 0.0394 | 0.0315 | 0.0413 |
| b | | 0.190 | 0.300 | | 0.0075 | 0.0118 |
| c | | 0.090 | 0.200 | | 0.0035 | 0.0079 |
| CP | | | 0.100 | | | 0.0039 |
| D | 3.000 | 2.900 | 3.100 | 0.1181 | 0.1142 | 0.1220 |
| e | 0.650 | – | – | 0.0256 | – | – |
| E | 6.400 | 6.200 | 6.600 | 0.2520 | 0.2441 | 0.2598 |
| E1 | 4.400 | 4.300 | 4.500 | 0.1732 | 0.1693 | 0.1772 |
| L | 0.600 | 0.450 | 0.750 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.000 | | | 0.0394 | | |
| α | | 0° | 8° | | 0° | 8° |
| N | 8 | | | 8 | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

# 9 Part numbering

**Table 17. Ordering information scheme**

Example: M34E02 – F DW 1 T P

**Device type**

M34 = ASSP $I^2C$ serial access EEPROM

**Device function**

E02 = 2 Kbit (256 × 8) SPD (serial presence detect) for DDR1 and DDR2

**Operating voltage**

F = $V_{CC}$ = 1.7 to 3.6 V over 0°C to 70 °C(1) or

F = $V_{CC}$ = 1.7 to 5.5 V over –40 °C to 85 °C(2)

**Package**

MB or MC= UDFDFPN8 (MLP8)

DW = TSSOP8 (4.4 × 3 mm body size)

**Temperature range**

1 = 0 to 70 °C

6 = –40 to 85 °C

**Option**

blank = Standard packing

T = Tape & reel packing

**Plating technology**

P or G = ECOPACK (RoHS compliant)

1. The 1.7 to 3.6 V operating voltage range is available only on temperature range 1 devices.
2. The 1.7 to 5.5 V operating voltage range is available only on temperature range 6 devices.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

# 10 Revision history

**Table 18. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 13-Nov-2003 | 1.0 | First release |
| 01-Dec-2003 | 1.1 | TSSOP8 4.4x3 package replaces TSSOP8 3x3 (MSOP8) package. Correction to sentence in “Setting the Write Protection”. Correction to specification of $t_{NS}$ values. |
| 29-Mar-2004 | 1.2 | Always NoACK after Address and Data bytes in *Table 6*. Improvement in $V_{IO}$ and $V_{CC}$ (min) in Absolute Maximum Ratings table. $I_{OL}$ changed for test condition of $V_{OL}$. MLP package mechanical data respecified. Soldering temperature information clarified for RoHS compliant devices. |
| 14-Apr-2004 | 2.0 | First public release |
| 24-Nov-2004 | 3.0 | Direct connection of E0, E1, E2 to $V_{SS}$ and $V_{CC}$ (see *Chip Enable (E0, E1, E2)* and *Use within a DDR1/DDR2 DRAM module* paragraphs). $Z_{EiL}$ and $Z_{EiH}$ parameters added to *Table 11: Input parameters*. E0, E1, E2 removed from the Parameter descriptions of $V_{IL}$ and $V_{IH}$ in *Table 13: DC characteristics (for temperature range 6 devices)*.<br>Document status promoted from Product Preview to full Datasheet. |
| 11-Mar-2005 | 4.0 | Datasheet title changed. *Features* revised.<br>Plating Technology options updated in *Table 17: Ordering information scheme*.<br>Resistance and capacitance renamed in *Figure 4: Maximum RP value versus bus parasitic capacitance (C) for an I2C bus*. |
| 28 -Apr-2005 | 5.0 | Text in Power On Reset changed. Noise filter value in *Table 11: Input parameters* modified. $I_{CC}$ value 2mA, when Vcc=3/6V, added to *Table 13: DC characteristics (for temperature range 6 devices)*. |
| 10-Apr-2006 | 6 | In *Table 14: AC characteristics*: Frequency $f_C$ changed from 100kHz to 400kHz, related AC timings ($t_{CHCL}$, $t_{CLCH}$, $t_{DXCX}$, $t_{CLQV}$ max, $t_{CHDX}$, $t_{DLCL}$, $t_{CHDH}$, $t_{DHDL}$) also modified.<br>Power On Reset paragraph removed replaced by *Internal device reset*.<br>*Figure 3: Device select code* inserted. $I_{CC1}$ modified in *Table 13: DC characteristics (for temperature range 6 devices)*.<br>Note *3* added to *Figure 14* and Note *2* added to *Figure 15*<br>All packages are ECOPACK® (see text added under *Description* and *Part numbering*, $T_{LEAD}$ removed from *Table 7: Absolute maximum ratings*). |

**Table 18. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 18-Mar-2009 | 7 | Datasheet title and *Features on page 1* modified: the device can be used with DDR1 and DDR2 DRAM configurations.<br>Temperature range 6 added, operating voltage range $V_{CC}$ extended in device temperature range 6. $I_{OL}$ added to and $T_A$ modified in *Table 7: Absolute maximum ratings*.<br>$I_{LO}$, $I_{CC}$ and $V_{IL}$ modified in *Table 13: DC characteristics (for temperature range 6 devices)*. *Table 14: AC characteristics* added. *Table 13: DC characteristics (for temperature range 6 devices)* modified. *Figure 13: AC waveforms* modified.<br>*Figure 4: Maximum RP value versus bus parasitic capacitance (C) for an I2C bus* updated. Note removed below *Figure 11: Serial presence detect block diagram*.<br>UFDFPN8 package specifications updated (see *Table 15: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data*).<br>Blank option removed under plating technology in *Table 17: Ordering information scheme*. Small text changes. |
| 25-Sep-2009 | 8 | *Section 2.5.2: Power-up conditions* and *Section 2.5.3: Device reset* updated. *Figure 4: Maximum RP value versus bus parasitic capacitance (C) for an I2C bus* modified.<br>$t_{NS}$ modified in *Table 11: Input parameters*.<br>$I_{CC}$ and $V_{IL}$ test conditions extended in *Table 12: DC characteristics (for temperature range 1 devices)*. |
| 01-Apr-2010 | 9 | Test condition updated in *Table 12: DC characteristics (for temperature range 1 devices)* and *Table 13: DC characteristics (for temperature range 6 devices)*<br>Updated *Figure 14: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, outline* and *Table 15: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data* |
| 23-Jul-2010 | 10 | Added M34E02-F part number.<br>Added ambient temperature with power applied in *Table 7: Absolute maximum ratings*.<br>Updated $I_{CC1}$ conditions in *Table 12: DC characteristics (for temperature range 1 devices)*.<br>Added *Note 4* for $t_{CLQV}$ in *Table 14: AC characteristics*. Updated *Figure 13: AC waveforms*.<br>$t_{CHDX}$ replaced by $t_{CHDL}$ in *Figure 13: AC waveforms*.<br>Modified MC package outline in *Figure 14: UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, outline*. |
| 27-May-2011 | 11 | Updated MLP8 package data. |

# Public Products List

PCN Title : M34E02 2-Kbit I2C Bus EEPROM Redesign and upgrade to the CMOSF8H+ process technology
PCN Reference : MMS-MMY/13/7720
PCN Created on : 28-FEB-2013

Subject : Public Products List

Dear Customer,

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## ST COMMERCIAL PRODUCT

M34E02-FDW6TP M34E02-FMC6TG

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